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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	25MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f2520-e-so

Pin Diagrams (Cont.'d) - RC2/CCP1/P1A - RC1/T10SI/CCP2⁽¹⁾ NC 44-pin TQFP RC6/TX/CK RC5/SDO RC4/SDI/SDA RD3/PSP3 RD2/PSP2 RD1/PSP1 RD0/PSP0 NC RC7/RX/DT 32 RC0/T10SO/T13CKI RD4/PSP4 RD5/PSP5/P1B -□ 31 OSC2/CLKO/RA6 OSC1/CLKI/RA7 RD6/PSP6/P1C 29 PIC18F4420 Vss RD7/PSP7/P1D 28 VDD Vss PIC18F4520 27 RE2/CS/AN7 V_{DD} 26 RE1/WR/AN6 RB0/INT0/FLT0/AN12 **>** □□□ RE0/RD/AN5 RB1/INT1/AN10 **→**□□ RA5/AN4/SS/HLVDIN/C2OUT RB2/INT2/AN8 →□□ 10 RB3/AN9/CCP2⁽¹⁾ NC RB4/KB10/AN11 + RB5/KB11/PGM + RB6/KB12/PGC + RB7/KB13/PGD + RB7/KB13/PGD -MCLR/VPP/RE3 -RA0/AN0 -RA1/AN1 -RA2/AN2/VREF -/CVREF + RC4/SDI/SDA RC3/SCK/SC RD3/PSP3 RD2/PSP2 RD1/PSP1 RD0/PSP0 RC5/SDO 44-pin QFN OSC2/CLKO/RA6 RC7/RX/DT RD4/PSP4 32 OSC1/CLKI/RA7 2 RD5/PSP5/P1B 31 Vss 3 RD6/PSP6/P1C 30 Vss RD7/PSP7/P1D PIC18F4420 29 Vdd 5 Vss 28 V_{DD} 6 PIC18F4520 27 RE2/CS/AN7 V_{DD} 26 RE1/WR/AN6 8 RB0/INT0/FLT0/AN12 RE0/RD/AN5 25 24 23 9 RB1/INT1/AN10 RA5/AN4/SS/HLVDIN/C2OUT 10 RA4/T0CKI/C1OUT RB2/INT2/AN8 RB4/KBI0/AN11 - RB5/KBI1/PGM - RB6/KBI2/PGC - RB7/KBI3/PGD - MCLR/PP/KE3 - MCLR/PP/KE3 - RA0/AN1 - RA1/AN1 -RB3/AN9/CCP2(1) RA2/AN2/VREF-/CVREF RA3/AN3/VREF+ Note 1: RB3 is the alternate pin for CCP2 multiplexing.

TABLE 1-2: PIC18F2420/2520 PINOUT I/O DESCRIPTIONS (CONTINUED)

	Pin Nu	ımber	Pin	Buffer	
Pin Name	SPDIP, SOIC	QFN	Туре		Description
					PORTC is a bidirectional I/O port.
RC0/T10SO/T13CKI RC0 T10SO T13CKI	11	8	I/O O I	ST — ST	Digital I/O. Timer1 oscillator output. Timer1/Timer3 external clock input.
RC1/T1OSI/CCP2 RC1 T1OSI CCP2 ⁽²⁾	12	9	I/O I I/O	ST Analog ST	Digital I/O. Timer1 oscillator input. Capture 2 input/Compare 2 output/PWM2 output.
RC2/CCP1 RC2 CCP1	13	10	I/O I/O	ST ST	Digital I/O. Capture 1 input/Compare 1 output/PWM1 output.
RC3/SCK/SCL RC3 SCK SCL	14	11	I/O I/O I/O	ST ST ST	Digital I/O. Synchronous serial clock input/output for SPI mode. Synchronous serial clock input/output for I ² C™ mode.
RC4/SDI/SDA RC4 SDI SDA	15	12	I/O I I/O	ST ST ST	Digital I/O. SPI data in. I ² C data I/O.
RC5/SDO RC5 SDO	16	13	I/O O	ST —	Digital I/O. SPI data out.
RC6/TX/CK RC6 TX CK	17	14	I/O O I/O	ST — ST	Digital I/O. EUSART asynchronous transmit. EUSART synchronous clock (see related RX/DT).
RC7/RX/DT RC7 RX DT	18	15	I/O I I/O	ST ST ST	Digital I/O. EUSART asynchronous receive. EUSART synchronous data (see related TX/CK).
RE3		_	_	_	See MCLR/VPP/RE3 pin.
Vss	8, 19	5, 16	Р	_	Ground reference for logic and I/O pins.
VDD	20	17	Р	_	Positive supply for logic and I/O pins.

Legend: TTL = TTL compatible input

CMOS = CMOS compatible input or output

ST = Schmitt Trigger input with CMOS levels
O = Output

I = Input P = Power

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

TABLE 1-3: PIC18F4420/4520 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Piı	n Numb	er	Pin	Buffer	Description
Pili Name	PDIP	QFN	TQFP	Туре	Туре	Description
RA0/AN0 RA0 AN0	2	19	19	I/O I	TTL Analog	PORTA is a bidirectional I/O port. Digital I/O. Analog input 0.
RA1/AN1 RA1 AN1	3	20	20	I/O I	TTL Analog	Digital I/O. Analog input 1.
RA2/AN2/VREF-/CVREF RA2 AN2 VREF- CVREF	4	21	21	I/O I I O	TTL Analog Analog Analog	Digital I/O. Analog input 2. A/D reference voltage (low) input. Comparator reference voltage output.
RA3/AN3/VREF+ RA3 AN3 VREF+	5	22	22	I/O I I	TTL Analog Analog	Digital I/O. Analog input 3. A/D reference voltage (high) input.
RA4/T0CKI/C1OUT RA4 T0CKI C1OUT	6	23	23	I/O I O	ST ST —	Digital I/O. Timer0 external clock input. Comparator 1 output.
RA5/AN4/SS/HLVDIN/ C2OUT RA5 AN4 SS HLVDIN C2OUT	7	24	24	I/O 	TTL Analog TTL Analog —	Digital I/O. Analog input 4. SPI slave select input. High/Low-Voltage Detect input. Comparator 2 output.
RA6						See the OSC2/CLKO/RA6 pin.
RA7						See the OSC1/CLKI/RA7 pin.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output

ST = Schmitt Trigger input with CMOS levels I = Input
O = Output P = Power

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

7.6 Operation During Code-Protect

Data EEPROM memory has its own code-protect bits in Configuration Words. External read and write operations are disabled if code protection is enabled.

The microcontroller itself can both read and write to the internal data EEPROM, regardless of the state of the code-protect Configuration bit. Refer to **Section 23.0** "**Special Features of the CPU**" for additional information.

7.7 Protection Against Spurious Write

There are conditions when the user may not want to write to the data EEPROM memory. To protect against spurious EEPROM writes, various mechanisms have been implemented. On power-up, the WREN bit is cleared. In addition, writes to the EEPROM are blocked during the Power-up Timer period (TPWRT, parameter 33).

The write initiate sequence and the WREN bit together help prevent an accidental write during brown-out, power glitch or software malfunction.

7.8 Using the Data EEPROM

The data EEPROM is a high-endurance, byte addressable array that has been optimized for the storage of frequently changing information (e.g., program variables or other data that are updated often). Frequently changing values will typically be updated more often than specification D124. If this is not the case, an array refresh must be performed. For this reason, variables that change infrequently (such as constants, IDs, calibration, etc.) should be stored in Flash program memory.

A simple data EEPROM refresh routine is shown in Example 7-3.

Note: If data EEPROM is only used to store constants and/or data that changes rarely, an array refresh is likely not required. See specification D124.

EXAMPLE 7-3: DATA EEPROM REFRESH ROUTINE

```
CLRF
             EEADR
                              ; Start at address 0
      BCF
             EECON1, CFGS
                              ; Set for memory
                             ; Set for Data EEPROM
             EECON1, EEPGD
      BCF
                              ; Disable interrupts
      BCF
             INTCON, GIE
      BSF
             EECON1, WREN
                               ; Enable writes
                              ; Loop to refresh array
gool
             EECON1, RD
                               ; Read current address
      BSF
      MOVLW
             55h
      MOVWF EECON2
                               ; Write 55h
      MOVLW 0AAh
                              ;
      MOVWF EECON2
                             ; Write OAAh
      BSF EECON1, WR
BTFSC EECON1, WR
                             ; Set WR bit to begin write
                              ; Wait for write to complete
      BRA
             $-2
      INCFSZ EEADR, F
                               ; Increment address
      BRA
             LOOP
                               ; Not zero, do it again
      BCF
             EECON1, WREN
                               ; Disable writes
      BSF
             INTCON, GIE
                               ; Enable interrupts
```

NOTES:

12.1 **Timer1 Operation**

Timer1 can operate in one of these modes:

- Timer
- · Synchronous Counter
- · Asynchronous Counter

The operating mode is determined by the clock select bit, TMR1CS (T1CON<1>). When TMR1CS is cleared (= 0), Timer1 increments on every internal instruction

cycle (Fosc/4). When the bit is set, Timer1 increments on every rising edge of the Timer1 external clock input or the Timer1 oscillator, if enabled.

When Timer1 is enabled, the RC1/T1OSI and RC0/ T1OSO/T13CKI pins become inputs. This means the values of TRISC<1:0> are ignored and the pins are read as '0'.

FIGURE 12-1: TIMER1 BLOCK DIAGRAM

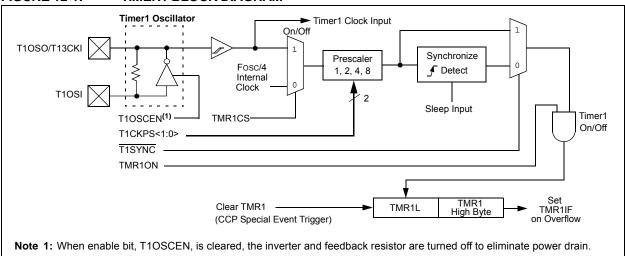
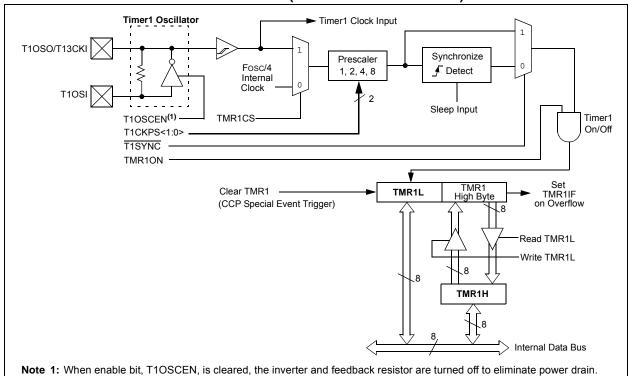


FIGURE 12-2: TIMER1 BLOCK DIAGRAM (16-BIT READ/WRITE MODE)



REGISTER 17-5: SSPCON2: MSSP CONTROL REGISTER 2 (I²C™ MODE)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GCEN	ACKSTAT	ACKDT ⁽²⁾	ACKEN ⁽¹⁾	RCEN ⁽¹⁾	PEN ⁽¹⁾	RSEN ⁽¹⁾	SEN ⁽¹⁾
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7 GCEN: General Call Enable bit (Slave mode only)

1 = Enables interrupt when a general call address (0000h) is received in the SSPSR

0 = General call address disabled.

bit 6 ACKSTAT: Acknowledge Status bit (Master Transmit mode only)

1 = Acknowledge was not received from slave

0 = Acknowledge was received from slave

bit 5 ACKDT: Acknowledge Data bit (Master Receive mode only)(2)

1 = Not Acknowledge

0 = Acknowledge

bit 4 **ACKEN:** Acknowledge Sequence Enable bit (Master Receive mode only)⁽¹⁾

1 = Initiates Acknowledge sequence on SDA and SCL pins and transmit ACKDT data bit. Automatically cleared by hardware.

0 = Acknowledge sequence Idle

bit 3 RCEN: Receive Enable bit (Master mode only)⁽¹⁾

1 = Enables Receive mode for I²C

0 = Receive Idle

bit 2 **PEN:** Stop Condition Enable bit (Master mode only)⁽¹⁾

1 = Initiates Stop condition on SDA and SCL pins. Automatically cleared by hardware.

0 = Stop condition Idle

bit 1 RSEN: Repeated Start Condition Enable bit (Master mode only)⁽¹⁾

1 = Initiates Repeated Start condition on SDA and SCL pins. Automatically cleared by hardware.

0 = Repeated Start condition Idle

bit 0 SEN: Start Condition Enable/Stretch Enable bit(1)

In Master mode:

1 = Initiates Start condition on SDA and SCL pins. Automatically cleared by hardware.

0 = Start condition Idle

In Slave mode:

1 = Clock stretching is enabled for both slave transmit and slave receive (stretch enabled)

o = Clock stretching is disabled

Note 1: For bits ACKEN, RCEN, PEN, RSEN, SEN: If the I²C module is not in the Idle mode, these bits may not be set (no spooling) and the SSPBUF may not be written (or writes to the SSPBUF are disabled).

2: Value that will be transmitted when the user initiates an Acknowledge sequence at the end of a receive.

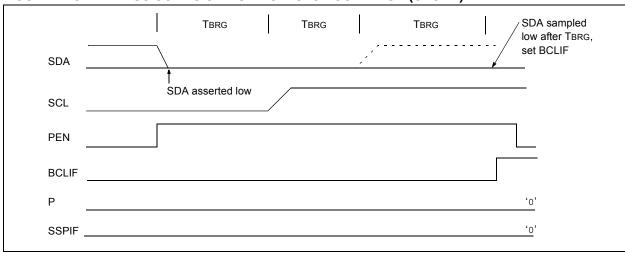
17.4.17.3 Bus Collision During a Stop Condition

Bus collision occurs during a Stop condition if:

- After the SDA pin has been deasserted and allowed to float high, SDA is sampled low after the BRG has timed out.
- After the SCL pin is deasserted, SCL is sampled low before SDA goes high.

The Stop condition begins with SDA asserted low. When SDA is sampled low, the SCL pin is allowed to float. When the pin is sampled high (clock arbitration), the Baud Rate Generator is loaded with SSPADD<6:0> and counts down to 0. After the BRG times out, SDA is sampled. If SDA is sampled low, a bus collision has occurred. This is due to another master attempting to drive a data '0' (Figure 17-31). If the SCL pin is sampled low before SDA is allowed to float high, a bus collision occurs. This is another case of another master attempting to drive a data '0' (Figure 17-32).

FIGURE 17-31: BUS COLLISION DURING A STOP CONDITION (CASE 1)





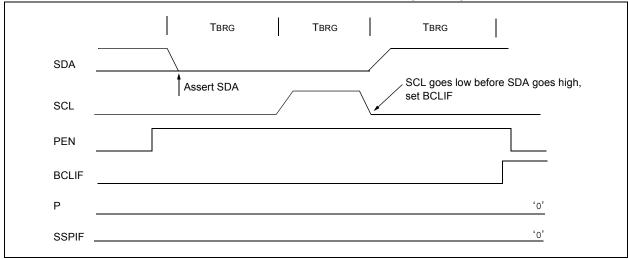


FIGURE 18-12: SYNCHRONOUS TRANSMISSION (THROUGH TXEN)

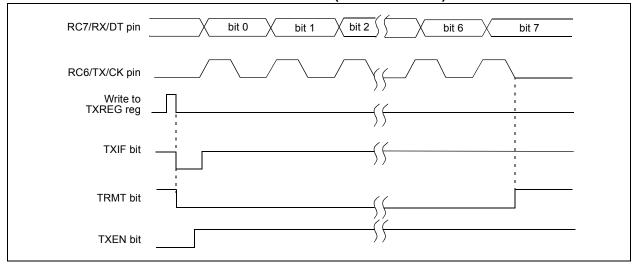


TABLE 18-7: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	49
PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	52
PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	52
IPR1	PSPIP ⁽¹⁾	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	52
RCSTA	SPEN RX9 SREN CREN ADDEN FERR OERR RX9D								
TXREG	EUSART Transmit Register								
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	51
BAUDCON	ABDOVF	RCIDL	RXDTP	TXCKP	BRG16	_	WUE	ABDEN	51
SPBRGH	BRGH EUSART Baud Rate Generator Register High Byte								
SPBRG	EUSART E	Baud Rate G	enerator Re	gister Low	Byte		•		51

Legend: — = unimplemented, read as '0'. Shaded cells are not used for synchronous master transmission.

Note 1: Reserved in 28-pin devices; always maintain these bits clear.

19.0 10-BIT ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The Analog-to-Digital (A/D) Converter module has 10 inputs for the 28-pin devices and 13 for the 40/44-pin devices. This module allows conversion of an analog input signal to a corresponding 10-bit digital number.

The module has five registers:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)
- A/D Control Register 2 (ADCON2)

The ADCON0 register, shown in Register 19-1, controls the operation of the A/D module. The ADCON1 register, shown in Register 19-2, configures the functions of the port pins. The ADCON2 register, shown in Register 19-3, configures the A/D clock source, programmed acquisition time and justification.

REGISTER 19-1: ADCON0: A/D CONTROL REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-6 Unimplemented: Read as '0'

bit 5-2 CHS<3:0>: Analog Channel Select bits

0000 = Channel 0 (AN0)

0001 = Channel 1 (AN1)

0010 = Channel 2 (AN2)

0011 = Channel 3 (AN3)

0100 = Channel 4 (AN4)

0101 = Channel 5 (AN5) $^{(1,2)}$

0110 = Channel 6 $(AN6)^{(1,2)}$

0111 = Channel 7 (AN7) $^{(1,2)}$

1000 = Channel 8 (AN8) 1001 = Channel 9 (AN9)

1010 = Channel 10 (AN10)

1011 = Channel 11 (AN11)

1100 = Channel 12 (AN12)

1101 = Unimplemented)(2)

1110 = Unimplemented)(2)

1111 = Unimplemented)(2)

bit 1 GO/DONE: A/D Conversion Status bit

When ADON = 1:

1 = A/D conversion in progress

0 = A/D Idle

bit 0 ADON: A/D On bit

1 = A/D Converter module is enabled

0 = A/D Converter module is disabled

Note 1: These channels are not implemented on 28-pin devices.

2: Performing a conversion on unimplemented channels will return a floating input measurement.

22.2 HLVD Setup

The following steps are needed to set up the HLVD module:

- 1. Write the value to the HLVDL<3:0> bits that selects the desired HLVD trip point.
- 2. Set the VDIRMAG bit to detect high voltage (VDIRMAG = 1) or low voltage (VDIRMAG = 0).
- 3. Enable the HLVD module by setting the HLVDEN bit.
- 4. Clear the HLVD interrupt flag (PIR2<2>), which may have been set from a previous interrupt.
- 5. Enable the HLVD interrupt, if interrupts are desired, by setting the HLVDIE and GIE bits (PIE2<2> and INTCON<7>). An interrupt will not be generated until the IRVST bit is set.

22.3 **Current Consumption**

When the module is enabled, the HLVD comparator and voltage divider are enabled and will consume static current. The total current consumption, when enabled, is specified in electrical specification parameter D022B.

Depending on the application, the HLVD module does not need to be operating constantly. To decrease the current requirements, the HLVD circuitry may only need to be enabled for short periods where the voltage is checked. After doing the check, the HLVD module may be disabled.

22.4 **HLVD Start-up Time**

The internal reference voltage of the HLVD module, specified in electrical specification parameter D420, may be used by other internal circuitry, such as the programmable Brown-out Reset. If the HLVD or other circuits using the voltage reference are disabled to lower the device's current consumption, the reference voltage circuit will require time to become stable before a low or high-voltage condition can be reliably detected. This start-up time, TIRVST, is an interval that is independent of device clock speed. It is specified in electrical specification parameter 36.

The HLVD interrupt flag is not enabled until TIRVST has expired and a stable reference voltage is reached. For this reason, brief excursions beyond the set point may not be detected during this interval (refer to Figure 22-2 or Figure 22-3).

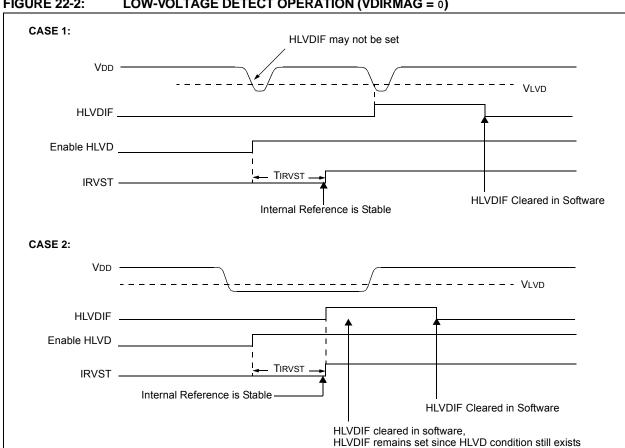


FIGURE 22-2: LOW-VOLTAGE DETECT OPERATION (VDIRMAG = 0)

REGISTER 23-4: CONFIG3H: CONFIGURATION REGISTER 3 HIGH (BYTE ADDRESS 300005h)

R/P-1	U-0	U-0	U-0	U-0	R/P-0	R/P-1	R/P-1
MCLRE	_	_	_	_	LPT1OSC	PBADEN	CCP2MX
bit 7							bit 0

Legend:

R = Readable bit P = Programmable bit U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed u = Unchanged from programmed state

bit 7 MCLRE: MCLR Pin Enable bit

1 = MCLR pin enabled; RE3 input pin disabled 0 = RE3 input pin enabled; MCLR disabled

bit 6-3 **Unimplemented:** Read as '0'

bit 2 LPT10SC: Low-Power Timer1 Oscillator Enable bit

1 = Timer1 configured for low-power operation0 = Timer1 configured for higher power operation

bit 1 PBADEN: PORTB A/D Enable bit

(Affects ADCON1 Reset state. ADCON1 controls PORTB<4:0> pin configuration.)

1 = PORTB<4:0> pins are configured as analog input channels on Reset

0 = PORTB<4:0> pins are configured as digital I/O on Reset

bit 0 CCP2MX: CCP2 MUX bit

1 = CCP2 input/output is multiplexed with RC10 = CCP2 input/output is multiplexed with RB3

REGISTER 23-5: CONFIG4L: CONFIGURATION REGISTER 4 LOW (BYTE ADDRESS 300006h)

R/P-1	R/P-0	U-0	U-0	U-0	R/P-1	U-0	R/P-1
DEBUG	XINST	_	_	_	LVP	_	STVREN
bit 7							bit 0

Legend:

R = Readable bit P = Programmable bit U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed u = Unchanged from programmed state

bit 7 **DEBUG:** Background Debugger Enable bit

1 = Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

0 = Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug

bit 6 XINST: Extended Instruction Set Enable bit

1 = Instruction set extension and Indexed Addressing mode enabled

0 = Instruction set extension and Indexed Addressing mode disabled (Legacy mode)

bit 5-3 **Unimplemented:** Read as '0'

bit 2 LVP: Single-Supply ICSP™ Enable bit

1 = Single-Supply ICSP enabled 0 = Single-Supply ICSP disabled

bit 1 **Unimplemented:** Read as '0'

bit 0 STVREN: Stack Full/Underflow Reset Enable bit

1 = Stack full/underflow will cause Reset 0 = Stack full/underflow will not cause Reset

BRA Unconditional Branch

Syntax: BRA n

Operands: $-1024 \le n \le 1023$ Operation: (PC) + 2 + $2n \rightarrow PC$

Status Affected: None

Encoding: 1101

Description: Add the 2's complement number, '2n', to the PC. Since the PC will have incremented to fetch the next instruction, the

new address will be PC + 2 + 2n. This instruction is a two-cycle instruction.

0nnn

nnnn

nnnn

Words: 1 Cycles: 2 Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal	Process Data	Write to PC
No	No	No	No
operation	operation	operation	operation

Example: HERE BRA Jump

Before Instruction

PC address (HERE)

After Instruction

PC address (Jump) **BSF** Bit Set f

Syntax: BSF f, b {,a} Operands: $0 \le f \le 255$

 $0 \le b \le 7$

 $a\in \left[0,1\right]$

Operation: $1 \rightarrow f < b >$

Status Affected: None

Encoding: ffff 1000 ffff bbba

Description: Bit 'b' in register 'f' is set.

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the

GPR bank (default).

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See Section 24.2.3 "Byte-Oriented and

Bit-Oriented Instructions in Indexed

Literal Offset Mode" for details.

Words: Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write
	register 'f'	Data	register 'f'

Example: BSF FLAG_REG, 7, 1

Before Instruction

FLAG_REG 0Ah

After Instruction

FLAG_REG 8Ah

Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity: Q1 Decode If skip: Q1 No	decremented placed in Williams placed in Williams placed back of the result which is alread a NOP in it a two-cyc of 'a' is 'o', to off 'a' is 'o', to off 'a' is 'o' a set is enable in Indexed off mode when section 24 Bit-Oriented Literal Offs of 1 (2) Note: 3 cycles and williams placed in the section 24 bit-Oriented Literal Offs of 1 (2)	est, t = 0 11da ffff ts of register 'f ed. If 'd' is '0', 'f. If 'd' is '1', th k in register 'f' is '0', the nex eady fetched, s executed ins le instruction. he Access Bar he BSR is use (default). nd the extendo	r' are the result is the result is (default). t instruction, is discarded stead, making the is selected. d to select the ed instruction ction operates Addressing Fh). See iented and is in Indexed details.	Oper Statu Enco Desc Word Cycle	rands: ration: us Affected: oding: cription:	decremented placed in Williams placed back instruction, discarded a instruction. If 'a' is 'o', till 'a' is 'o', till 'a' is 'o' at set is enabli in Indexed mode where Section 24 Bit-Oriented Literal Offs 1 1(2) Note: 3 c	est, t ≠ 0	the result is e result is (default). next dy fetched, is kecuted ycle ak is selected. d to select the ed instruction operates addressing [-h]. See iented and s in Indexed details.
Operation: Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity: Q1 Decode If skip: Q1 No operation If skip and followed b	d ∈ [0,1] a ∈ [0,1] a ∈ [0,1] (f) − 1 → de skip if result None 0010 The content decremente placed in We placed back if the result which is almand a NoP if it a two-cyc. If 'a' is '0', the set is enable in Indexed in I	t = 0 11da ffff ts of register 'f ed. If 'd' is '0', /. If 'd' is '1', th k in register 'f is '0', the nex eady fetched, s executed ins le instruction. he Access Ban he BSR is use (default). nd the extend ed, this instruct Literal Offset / lever f ≤ 95 (5 2.3 "Byte-Or ed Instruction set Mode" for color of the skip and a 2-word instruction	f' are the result is ne result is (default). t instruction, is discarded stead, making nk is selected. d to select the ed instruction ction operates Addressing Fh). See iented and us in Indexed details. d followed action.	Oper Statu Enco Desc Word Cycle	ration: us Affected: oding: cription: ds: es:	$d \in [0,1]$ $a \in [0,1]$ $a \in [0,1]$ $a \in [0,1]$ $(f) - 1 \rightarrow de$ skip if result None 0100 The content decremented placed in White placed back instruction, discarded a placed in the result instruction. If 'a' is '0', the second of the result instruction in the second in the seco	est, It ≠ 0 11da ffff ats of register 'f ed. If 'd' is '0', the ed. If 'd' is '1', the k in register 'f' t is not '0', the which is alrea aking it a two-c aking it a two-c the Access Bar he BSR is used (default). und the extende led, this instruct Literal Offset A never f ≤ 95 (5l 1.2.3 "Byte-Ori ed Instruction set Mode" for	the result is e result is (default). next dy fetched, is kecuted ycle ak is selected. d to select the ed instruction operates addressing [-h]. See iented and s in Indexed details.
Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity: Q1 Decode If skip: Q1 No operation If skip and followed b	None 0010 The content decrements placed in W placed back If the result which is almand a NOP i it a two-cyc If 'a' is '0', tl If 'a' is '1', tl GPR bank (If 'a' is '0' a set is enabl in Indexed I mode when Section 24 Bit-Oriente Literal Offs 1 1(2) Note: 3 cy by a	t = 0 11da ffff ts of register 'f ed. If 'd' is '0', /. If 'd' is '1', th k in register 'f is '0', the nex eady fetched, s executed ins le instruction. he Access Ban he BSR is use (default). nd the extend ed, this instruct Literal Offset / lever f ≤ 95 (5 2.3 "Byte-Or ed Instruction set Mode" for color of the skip and a 2-word instruction	f' are the result is ne result is (default). t instruction, is discarded stead, making nk is selected. d to select the ed instruction ction operates Addressing Fh). See iented and us in Indexed details. d followed action.	Statu Enco Desc Word Cycle	us Affected: oding: cription: ds: es:	None 0100 The content decrements placed in William placed back instruction, discarded a instruction. If 'a' is 'o', till 'a' is 'o', till 'a' is 'o' at set is enabli in Indexed mode wher Section 24 Bit-Orients Literal Offs 1 1(2) Note: 3 0	ats of register 'f ed. If 'd' is '0', 't v. If 'd' is '1', the k in register 'f' t is not '0', the which is alread and a NOP is exaking it a two-che Access Barche BSR is used (default). Inde the extended the ext	the result is e result is (default). next dy fetched, is kecuted ycle ak is selected. d to select the ed instruction operates addressing [-h]. See iented and s in Indexed details.
Encoding: Description: Words: Cycles: Q Cycle Activity: Q1 Decode If skip: Q1 No operation If skip and followed b	The content decrements placed in W placed back If the result which is almand a NOP i it a two-cyc If 'a' is '0', tl If 'a' is '1', tl GPR bank (If 'a' is '0' a set is enabl in Indexed I mode when Section 24 Bit-Oriente Literal Offs 1 1(2) Note: 3 cy by a	ts of register 'f' ed. If 'd' is '1', the ed. If 'd' is '1', the ed. If 'd' is '1', the in register 'f' is '0', the nex eady fetched, s executed ins le instruction. The Access Bar The BSR is use (default). The extended, this instruct Literal Offset A The ever f ≤ 95 (5) 2.3 "Byte-Or The distriction The extended of	f' are the result is ne result is (default). t instruction, is discarded stead, making nk is selected. d to select the ed instruction ction operates Addressing Fh). See iented and us in Indexed details. d followed action.	Enco Desc Word Cycle	ds:	The content decrements placed in W placed back instruction, discarded a instruction. If 'a' is '0', ti f' a' is '1', ti GPR bank If 'a' is '0' a set is enabl in Indexed mode wher Section 24 Bit-Oriente Literal Offs 1 1(2) Note: 3 0	this of register 'f' ed. If 'd' is '0', '1 ed. If 'd' is '1', th k in register 'f' is not '0', the which is alrea and a NOP is ex aking it a two-c the Access Bar he BSR is used (default). und the extende led, this instruct Literal Offset A never f ≤ 95 (5l 3.2.3 "Byte-Ori ed Instruction set Mode" for	the result is e result is (default). next dy fetched, is kecuted ycle ak is selected. d to select the ed instruction operates addressing [-h]. See iented and s in Indexed details.
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Cycles: Q Cycle Activity: Q1 Decode If skip: Q1 No operation If skip and followed b	1(2) Note: 3 cy by a	a 2-word instru	iction.	Cycle	es:	1 1(2) Note: 3 (cycles if skip a	nd followed
Q Cycle Activity: Q1 Decode If skip: Q1 No operation If skip and followed b	Note: 3 cy by a	a 2-word instru	iction.	Cycle	es:	1(2) Note: 3 (
Q1 Decode If skip: Q1 No operation If skip and followed b		Q3	Q4	QC		Бу	a 2-word iristi	uction.
Decode r If skip: Q1 No operation of skip and followed b		Q3	Q4	QU	'v colo A otiv (itv /:			
If skip: Q1 No operation If skip and followed b	Rear		347.1		cycle Activity: Q1	Q2	Q3	Q4
If skip: Q1 No operation If skip and followed b	register 'f'	Process Data	Write to destination		Decode	Read	Process	Write to
Q1 No operation of skip and followed by	regione i	2010	40044		200040	register 'f'	Data	destination
operation of	Q2	Q3	Q4	lf sk	kip:			
If skip and followed b	No	No	No		Q1	Q2	Q3	Q4
	operation	operation	operation		No	No	No	No
Q1	by 2-word in	struction:		16 1	operation	operation	operation	operation
	Q2	Q3	Q4	IT SK	kip and followe	•		0.4
No	No	No	No		Q1	Q2 No	Q3 No	Q4
operation o	operation No	operation No	operation No		No operation	operation	operation	No operation
	operation	operation	operation		No	No	No	No
·	HERE CONTINUE	DECFSZ GOTO	CNT, 1, 1 LOOP	Exar	operation		operation DCFSNZ TEM	operation
Before Instruction							:	
PC = After Instruction CNT =	= Address = CNT - 1	S (HERE)			TEMP After Instruction	= on	?	
If CNT = PC = If CNT ≠ PC =	= 0; = Addrood	(CONTINUE	!)		TEMP If TEMP	=	TEMP – 1, 0;	ZERO)

25.0 DEVELOPMENT SUPPORT

The PIC[®] microcontrollers are supported with a full range of hardware and software development tools:

- · Integrated Development Environment
 - MPLAB® IDE Software
- · Assemblers/Compilers/Linkers
 - MPASM™ Assembler
 - MPLAB C18 and MPLAB C30 C Compilers
 - MPLINK™ Object Linker/ MPLIB™ Object Librarian
 - MPLAB ASM30 Assembler/Linker/Library
- Simulators
 - MPLAB SIM Software Simulator
- Emulators
 - MPLAB ICE 2000 In-Circuit Emulator
 - MPLAB REAL ICE™ In-Circuit Emulator
- · In-Circuit Debugger
 - MPLAB ICD 2
- · Device Programmers
 - PICSTART® Plus Development Programmer
 - MPLAB PM3 Device Programmer
 - PICkit™ 2 Development Programmer
- Low-Cost Demonstration and Development Boards and Evaluation Kits

25.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16-bit microcontroller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- · A single graphical interface to all debugging tools
 - Simulator
 - Programmer (sold separately)
 - Emulator (sold separately)
 - In-Circuit Debugger (sold separately)
- · A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- · High-level source code debugging
- Visual device initializer for easy register initialization
- · Mouse over variable inspection
- Drag and drop variables from source to watch windows
- · Extensive on-line help
- Integration of select third party tools, such as HI-TECH Software C Compilers and IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either assembly or C)
- One touch assemble (or compile) and download to PIC MCU emulator and simulator tools (automatically updates all project information)
- · Debug using:
 - Source files (assembly or C)
 - Mixed assembly and C
 - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

26.3 DC Characteristics: PIC18F2420/2520/4420/4520 (Industrial) PIC18LF2420/2520/4420/4520 (Industrial)

DC CHA	ARACTE	RISTICS				unless otherwise stated) ≤ +85°C for industrial
Param No.	Symbol	Characteristic	Min	Max	Units	Conditions
	VIL	Input Low Voltage				
		I/O Ports:				
D030		with TTL Buffer	Vss	0.15 VDD	V	VDD < 4.5V
D030A			_	0.8	V	$4.5V \le VDD \le 5.5V$
D031		with Schmitt Trigger Buffer	Vss	0.2 VDD	V	
D031A		RC3 and RC4	Vss	0.3 VDD	V	I ² C™ enabled
D031B			Vss	0.8	V	SMBus enabled
D032		MCLR	Vss	0.2 VDD	V	
D033		OSC1	Vss	0.3 VDD	V	HS, HSPLL modes
D033A		OSC1	Vss	0.2 VDD	V	RC, EC modes ⁽¹⁾
D033B		OSC1	Vss	0.3	V	XT, LP modes
D034	\ /	T13CKI	Vss	0.3	V	
	VIH	Input High Voltage I/O Ports:				
D040		with TTL Buffer	0.25 VDD + 0.8V	VDD	V	VDD < 4.5V
D040A		with FTE Buller	2.0	VDD	V	4.5V ≤ VDD ≤ 5.5V
D040A		with Schmitt Trigger Buffer	0.8 VDD	VDD	V	4.50 \(\) \(
D041A		RC3 and RC4	0.7 VDD	VDD	V	I ² C enabled
D041R		100 and 104	2.1	VDD	V	SMBus enabled
D041B		MCLR	0.8 VDD	VDD	V	CIVIDUS CHADICA
D042		OSC1	0.7 VDD	VDD	V	HS, HSPLL modes
D043A		OSC1	0.7 VDD 0.8 VDD	VDD	V	EC mode
D043A		OSC1	0.9 VDD	VDD	V	RC mode ⁽¹⁾
D043C		OSC1	1.6	VDD	V	XT, LP modes
D044		T13CKI	1.6	VDD	V	
	lı∟	Input Leakage Current ^(2,3)				
D060		I/O Ports	_	±200	nA	VDD < 5.5V, VSS ≤ VPIN ≤ VDD,
				±50	nA	Pin at high-impedance VDD < 3V, VSS ≤ VPIN ≤ VDD, Pin at high-impedance
D061		MCLR	_	±1	μΑ	$Vss \le VPIN \le VDD$
D063		OSC1	–	±1	μΑ	$Vss \le VPIN \le VDD$
	IPU	Weak Pull-up Current				
D070	IPURB	PORTB Weak Pull-up Current	50	400	μΑ	VDD = 5V, VPIN = VSS

Note 1: In RC oscillator configuration, the OSC1/CLKI pin is a Schmitt Trigger input. It is not recommended that the PIC[®] device be driven with an external clock while in RC mode.

^{2:} The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

^{3:} Negative current is defined as current sourced by the pin.

26.4 AC (Timing) Characteristics

26.4.1 TIMING PARAMETER SYMBOLOGY

The timing parameter symbols have been created using one of the following formats:

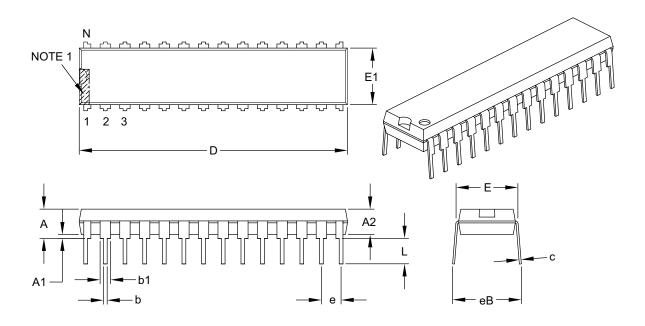
1. TppS2ppS		3. Tcc:st	(I ² C specifications only)
2. TppS		4. Ts	(I ² C specifications only)
Т			
F	Frequency	Т	Time
Lowercase letters (pp) and their meanings:			
рр			
СС	CCP1	osc	OSC1
ck	CLKO	rd	RD
cs	CS	rw	RD or WR
di	SDI	sc	SCK
do	SDO	ss	SS
dt	Data in	tO	T0CKI
io	I/O port	t1	T13CKI
mc	MCLR	wr	WR
Uppercase	letters and their meanings:		
S			
F	Fall	Р	Period
Н	High	R	Rise
I	Invalid (High-impedance)	V	Valid
L	Low	Z	High-impedance
I ² C only			
AA	output access	High	High
BUF	Bus free	Low	Low
Tcc:st (I ² C	specifications only)		
CC			
HD	Hold	SU	Setup
ST			
DAT	DATA input hold	STO	Stop condition
STA	Start condition		

28.2 Package Details

The following sections give the technical details of the packages.

28-Lead Skinny Plastic Dual In-Line (SP) - 300 mil Body [SPDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		INCHES	
Dimension	n Limits	MIN	NOM	MAX
Number of Pins	N		28	
Pitch	е	.100 BSC		
Top to Seating Plane	Α	1	-	.200
Molded Package Thickness	A2	.120	.135	.150
Base to Seating Plane	A1	.015	-	_
Shoulder to Shoulder Width	Е	.290	.310	.335
Molded Package Width	E1	.240	.285	.295
Overall Length	D	1.345	1.365	1.400
Tip to Seating Plane	L	.110	.130	.150
Lead Thickness	С	.008	.010	.015
Upper Lead Width	b1	.040	.050	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eВ	-	_	.430

Notes

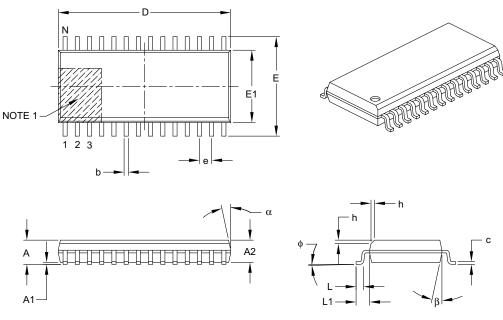
- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic.
- 3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B

28-Lead Plastic Small Outline (SO) – Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		MILLIMETERS	3
Dimension	n Limits	MIN	NOM	MAX
Number of Pins	N		28	
Pitch	е		1.27 BSC	
Overall Height	Α	_	_	2.65
Molded Package Thickness	A2	2.05	_	_
Standoff §	A1	0.10	_	0.30
Overall Width	Е		10.30 BSC	
Molded Package Width	E1	7.50 BSC		
Overall Length	D	17.90 BSC		
Chamfer (optional)	h	0.25	_	0.75
Foot Length	L	0.40	_	1.27
Footprint	L1	1.40 REF		
Foot Angle Top	ф	0°	_	8°
Lead Thickness	С	0.18	_	0.33
Lead Width	b	0.31	_	0.51
Mold Draft Angle Top	α	5°	_	15°
Mold Draft Angle Bottom	β	5°	_	15°

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic.
- 3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-052B

RA4/T0CKI/C1OUT	13, 17	PORTE	
RA5/AN4/SS/HLVDIN/C2OUT	13, 17	Associated Registers	119
RB0/INT0/FLT0/AN12	14, 18	LATE Register	117
RB1/INT1/AN10	14, 18	PORTE Register	
RB2/INT2/AN8	14, 18	PSP Mode Select (PSPMODE Bit)	
RB3/AN9/CCP2	14, 18	TRISE Register	
RB4/KBI0/AN11		Power-Managed Modes	
RB5/KBI1/PGM		and A/D Operation	
RB6/KBI2/PGC	•	and EUSART Operation	
RB7/KBI3/PGD		and Multiple Sleep Commands	
RC0/T10S0/T13CKI		and PWM Operation	
RC1/T10SI/CCP2	•	and SPI Operation	
RC2/CCP1	•	Clock Transitions and Status Indicators	
		Effects on Clock Sources	
RC2/CCP1/P1A			
RC3/SCK/SCL	*	Entering	
RC4/SDI/SDA	•	Exiting Idle and Sleep Modes	
RC5/SDO	•	by Interrupt	
RC6/TX/CK	•	by Reset	39
RC7/RX/DT	•	by WDT Time-out	
RD0/PSP0		Without a Start-up Delay	
RD1/PSP1	20	Idle Modes	
RD2/PSP2	20	PRI_IDLE	38
RD3/PSP3	20	RC_IDLE	39
RD4/PSP4	20	SEC_IDLE	38
RD5/PSP5/P1B	20	Run Modes	
RD6/PSP6/P1C	20	PRI_RUN	
RD7/PSP7/P1D		RC_RUN	
RE0/RD/AN5		SEC RUN	
RE1/WR/AN6		Selecting	
RE2/CS/AN7		Sleep Mode	
VDD		Summary (table)	
Vss	•	Power-on Reset (POR)	
	15, 21	Power-up Timer (PWRT)	
Pinout I/O Descriptions PIC18F2420/2520	10		
		Time-out Sequence	
PIC18F4420/4520		Power-up Delays	
PIR Registers		Power-up Timer (PWRT)	31
PLL Frequency Multiplier		Prescaler	4=0
HSPLL Oscillator Mode		Timer2	
Use with INTOSC		Prescaler, Timer0	
POP	296	Prescaler, Timer2	
POR. See Power-on Reset.		PRI_IDLE Mode	
PORTA		PRI_RUN Mode	
Associated Registers		Program Counter	54
LATA Register	105	PCL, PCH and PCU Registers	54
PORTA Register	105	PCLATH and PCLATU Registers	54
TRISA Register	105	Program Memory	
PORTB		and Extended Instruction Set	72
Associated Registers	110	Code Protection	264
LATB Register		Instructions	58
PORTB Register		Two-Word	
RB7:RB4 Interrupt-on-Change Flag		Interrupt Vector	
(RBIF Bit)	108	Look-up Tables	
TRISB Register		Map and Stack (diagram)	
PORTC	100	Reset Vector	
	110		
Associated Registers		Program Verification and Code Protection	
LATC Register		Associated Registers	
PORTC Register		Programming, Device Instructions	267
RC3/SCK/SCL Pin		PSP. See Parallel Slave Port.	
TRISC Register	111	Pulse-Width Modulation. See PWM (CCP Module)	
PORTD		and PWM (ECCP Module).	
Associated Registers	116	PUSH	
LATD Register	114	PUSH and POP Instructions	55
Parallel Slave Port (PSP) Function		PUSHL	312
PORTD Register			
TRISD Register			