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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	25MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (16K × 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f2520-e-sp

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Din Nomo	Pin Number			Pin Buffer		Description		
	PDIP	QFN	TQFP	Туре	Туре	Description		
						PORTA is a bidirectional I/O port.		
RA0/AN0 RA0 AN0	2	19	19	I/O I	TTL Analog	Digital I/O. Analog input 0.		
RA1/AN1 RA1 AN1	3	20	20	I/O I	TTL Analog	Digital I/O. Analog input 1.		
RA2/AN2/VREF-/CVREF RA2 AN2 VREF- CVREF	4	21	21	I/O I I O	TTL Analog Analog Analog	Digital I/O. Analog input 2. A/D reference voltage (low) input. Comparator reference voltage output.		
RA3/AN3/VREF+ RA3 AN3 VREF+	5	22	22	I/O I I	TTL Analog Analog	Digital I/O. Analog input 3. A/D reference voltage (high) input.		
RA4/T0CKI/C1OUT RA4 T0CKI C1OUT	6	23	23	I/O I O	ST ST	Digital I/O. Timer0 external clock input. Comparator 1 output.		
RA5/AN4/SS/HLVDIN/ C2OUT RA5 AN4 SS HLVDIN C2OUT	7	24	24	I/O I I O	TTL Analog TTL Analog —	Digital I/O. Analog input 4. SPI slave select input. High/Low-Voltage Detect input. Comparator 2 output.		
RA6						See the OSC2/CLKO/RA6 pin.		
RA7						See the OSC1/CLKI/RA7 pin.		
Legend: TTL = TTL co	mpatibl	e input		001	(CMOS = CMOS compatible input or output		
SI = Schmit O = Output	tt Trigge	r input v	with CM	US lev	eis I F	= input P = Power		

TABLE 1-3:	PIC18F4420/4520 PINOUT I/O DESCRIPTIONS ((CONTINUED)	

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

3.5.4 EXIT WITHOUT AN OSCILLATOR START-UP DELAY

Certain exits from power-managed modes do not invoke the OST at all. There are two cases:

- PRI_IDLE mode, where the primary clock source is not stopped and
- the primary clock source is not any of the LP, XT, HS or HSPLL modes.

In these instances, the primary clock source either does not require an oscillator start-up delay, since it is already running (PRI_IDLE), or normally does not require an oscillator start-up delay (RC, EC and INTIO Oscillator modes). However, a fixed delay of interval TCSD following the wake event is still required when leaving Sleep and Idle modes to allow the CPU to prepare for execution. Instruction execution resumes on the first clock cycle following this delay.

TABLE 3-2:EXIT DELAY ON WAKE-UP BY RESET FROM SLEEP MODE OR ANY IDLE MODE
(BY CLOCK SOURCES)

Clock Source Before Wake-up	Clock Source After Wake-up	Exit Delay	Clock Ready Status Bit (OSCCON)
	LP, XT, HS		
Primary Device Clock	HSPLL	теер(1)	OSTS
(PRI_IDLE mode)	EC, RC		
	INTOSC ⁽²⁾		IOFS
	LP, XT, HS	Tost ⁽³⁾	
	HSPLL	Tost + t _{rc} ⁽³⁾	OSTS
TIOSE OF INTRE	EC, RC	TCSD ⁽¹⁾	
	INTOSC ⁽²⁾	TCSD ⁽¹⁾	IOFS
	LP, XT, HS	Tost ⁽³⁾	
	HSPLL	Tost + t _{rc} (3)	OSTS
	EC, RC	TCSD ⁽¹⁾	
	INTOSC ⁽²⁾	TCSD ⁽¹⁾	IOFS
	LP, XT, HS	Tost ⁽³⁾	
None	HSPLL	Tost + t _{rc} (3)	OSTS
(Sleep mode)	EC, RC	Tcsd ⁽¹⁾	
	INTOSC ⁽²⁾	TCSD ⁽¹⁾	IOFS

Note 1: TCSD (parameter 38) is a required delay when waking from Sleep and all Idle modes and runs concurrently with any other required delays (see Section 3.4 "Idle Modes"). On Reset, INTOSC defaults to 1 MHz.

2: Includes both the INTOSC 8 MHz source and postscaler derived frequencies.

3: TOST is the Oscillator Start-up Timer (parameter 32). t_{rc} is the PLL lock-out timer (parameter F12); it is also designated as TPLL.

4.0 RESET

The PIC18F2420/2520/4420/4520 devices differentiate between various kinds of Reset:

- a) Power-on Reset (POR)
- b) MCLR Reset during normal operation
- c) MCLR Reset during power-managed modes
- d) Watchdog Timer (WDT) Reset (during execution)
- e) Programmable Brown-out Reset (BOR)
- f) RESET Instruction
- g) Stack Full Reset
- h) Stack Underflow Reset

This section discusses Resets generated by MCLR, POR and BOR and covers the operation of the various start-up timers. Stack Reset events are covered in Section 5.1.2.4 "Stack Full and Underflow Resets". WDT Resets are covered in Section 23.2 "Watchdog Timer (WDT)". A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 4-1.

4.1 RCON Register

Device Reset events are tracked through the RCON register (Register 4-1). The lower five bits of the register indicate that a specific Reset event has occurred. In most cases, these bits can only be cleared by the event and must be set by the application after the event. The state of these flag bits, taken together, can be read to indicate the type of Reset that just occurred. This is described in more detail in **Section 4.6 "Reset State of Registers"**.

The RCON register also has control bits for setting interrupt priority (IPEN) and software control of the BOR (SBOREN). Interrupt priority is discussed in Section 9.0 "Interrupts". BOR is covered in Section 4.4 "Brown-out Reset (BOR)".





6.3 Reading the Flash Program Memory

The TBLRD instruction is used to retrieve data from program memory and places it into data RAM. Table reads from program memory are performed one byte at a time.

TBLPTR points to a byte address in program space. Executing TBLRD places the byte pointed to into TABLAT. In addition, TBLPTR can be modified automatically for the next table read operation.

The internal program memory is typically organized by words. The Least Significant bit of the address selects between the high and low bytes of the word. Figure 6-4 shows the interface between the internal program memory and the TABLAT.

FIGURE 6-4: READS FROM FLASH PROGRAM MEMORY



EXAMPLE 6-1: READING A FLASH PROGRAM MEMORY WORD

	MOVLW MOVWF MOVLW MOVUF MOVLW MOVWF	CODE_ADDR_UPPER TBLPTRU CODE_ADDR_HIGH TBLPTRH CODE_ADDR_LOW TBLPTRL	;;	: Load TBLPTR with the base : address of the word
READ_WORD				
	TBLRD*+ MOVF TABLAT, W		;	; read into TABLAT and increment
			;	; get data
	MOVWF	WORD_EVEN		
	TBLRD*-	+	;	; read into TABLAT and increment
	MOVFW	TABLAT, W	;	; get data
	MOVF	WORD_ODD		

10.0 I/O PORTS

Depending on the device selected and features enabled, there are up to five ports available. Some pins of the I/O ports are multiplexed with an alternate function from the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

Each port has three registers for its operation. These registers are:

- TRIS register (Data Direction register)
- PORT register (reads the levels on the pins of the device)
- LAT register (Data Latch register)

The Data Latch (LAT register) is useful for read-modifywrite operations on the value that the I/O pins are driving.

A simplified model of a generic I/O port, without the interfaces to other peripherals, is shown in Figure 10-1.



10.1 PORTA, TRISA and LATA Registers

PORTA is an 8-bit wide, bidirectional port. The corresponding Data Direction register is TRISA. Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a high-impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin). Reading the PORTA register reads the status of the pins, whereas writing to it, will write to the port latch.

The Data Latch (LATA) register is also memory mapped. Read-modify-write operations on the LATA register read and write the latched output value for PORTA.

The RA4 pin is multiplexed with the Timer0 module clock input and one of the comparator outputs to become the RA4/T0CKI/C1OUT pin. Pins RA6 and RA7 are multiplexed with the main oscillator pins; they are enabled as oscillator or I/O pins by the selection of the main oscillator in the Configuration register (see **Section 23.1 "Configuration Bits**" for details). When they are not used as port pins, RA6 and RA7 and their associated TRIS and LAT bits are read as 'o'.

The other PORTA pins are multiplexed with analog inputs, the analog VREF+ and VREF- inputs and the comparator voltage reference output. The operation of pins RA<3:0> and RA5 as A/D Converter inputs is selected by clearing or setting the control bits in the ADCON1 register (A/D Control Register 1).

Pins RA0 through RA5 may also be used as comparator inputs or outputs by setting the appropriate bits in the CMCON register. To use RA<3:0> as digital inputs, it is also necessary to turn off the comparators.

Note:	On a Power-on Reset, RA5 and RA<3:0>
	are configured as analog inputs and read
	as '0'. RA4 is configured as a digital input.

The RA4/T0CKI/C1OUT pin is a Schmitt Trigger input. All other PORTA pins have TTL input levels and full CMOS output drivers.

The TRISA register controls the direction of the PORTA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs.

EXAMPLE 10-1: INITIALIZING PORTA

CLRF	PORTA	;	Initialize PORTA by
		;	clearing output
		;	data latches
CLRF	LATA	;	Alternate method
		;	to clear output
		;	data latches
MOVLW	07h	;	Configure A/D
MOVWF	ADCON1	;	for digital inputs
MOVWF	07h	;	Configure comparators
MOVWF	CMCON	;	for digital input
MOVLW	0CFh	;	Value used to
		;	initialize data
		;	direction
MOVWF	TRISA	;	Set RA<3:0> as inputs
		;	RA<5:4> as outputs

	TORIDI				
Pin	Function	TRIS Setting	I/O	I/O Type	Description
RD0/PSP0	RD0	0	0	DIG	LATD<0> data output.
		1	I	ST	PORTD<0> data input.
	PSP0	x	0	DIG	PSP read data output (LATD<0>); takes priority over port data.
		x	I	TTL	PSP write data input.
RD1/PSP1	RD1	0	0	DIG	LATD<1> data output.
		1	I	ST	PORTD<1> data input.
	PSP1	x	0	DIG	PSP read data output (LATD<1>); takes priority over port data.
		x	I	TTL	PSP write data input.
RD2/PSP2 RD2 0 O DIG LATD<2> data output.				LATD<2> data output.	
		1	I	ST	PORTD<2> data input.
	PSP2	x	0	DIG	PSP read data output (LATD<2>); takes priority over port data.
		x	I	TTL	PSP write data input.
RD3/PSP3	RD3	0	0	DIG	LATD<3> data output.
		1	I	ST	PORTD<3> data input.
	PSP3	x	0	DIG	PSP read data output (LATD<3>); takes priority over port data.
		x	I	TTL	PSP write data input.
RD4/PSP4	RD4	0	0	DIG	LATD<4> data output.
		1	I	ST	PORTD<4> data input.
	PSP4	x	0	DIG	PSP read data output (LATD<4>); takes priority over port data.
		x	I	TTL	PSP write data input.
RD5/PSP5/P1B	RD5	0	0	DIG	LATD<5> data output.
		1	I	ST	PORTD<5> data input.
	PSP5	x	0	DIG	PSP read data output (LATD<5>); takes priority over port data.
		x	I	TTL	PSP write data input.
	P1B	0	0	DIG	ECCP1 Enhanced PWM output, channel B; takes priority over port and PSP data. May be configured for tri-state during Enhanced PWM shutdown events.
RD6/PSP6/P1C	RD6	0	0	DIG	LATD<6> data output.
		1	I	ST	PORTD<6> data input.
	PSP6	x	0	DIG	PSP read data output (LATD<6>); takes priority over port data.
		х	Ι	TTL	PSP write data input.
	P1C	0	0	DIG	ECCP1 Enhanced PWM output, channel C; takes priority over port and PSP data. May be configured for tri-state during Enhanced PWM shutdown events.
RD7/PSP7/P1D	RD7	0	0	DIG	LATD<7> data output.
		1	I	ST	PORTD<7> data input.
	PSP7	x	0	DIG	PSP read data output (LATD<7>); takes priority over port data.
		x	I	TTL	PSP write data input.
	P1D	0	0	DIG	ECCP1 Enhanced PWM output, channel D; takes priority over port and PSP data. May be configured for tri-state during Enhanced PWM shutdown events.

TABLE 10-7: PORTD	I/O	SUMMARY
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Legend: DIG = Digital level output; TTL = TTL input buffer; ST = Schmitt Trigger input buffer; x = Don't care (TRIS bit does not affect port direction or is overridden for this option).

R-0	R-0	R/W-0	R/W-0	U-0	R/W-1	R/W-1	R/W-1
IBF	OBF	IBOV	PSPMODE		TRISE2	TRISE1	TRISE0
bit 7			•				bit 0
Legend:							
R = Readabl	e bit	W = Writable	bit	U = Unimplen	nented bit, read	d as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown
bit /	IBF: Input Bu	ffer Full Status	bit				
	1 = A word ha	as been receiv has been recei	ed and waiting t	to be read by th	ne CPU		
bit 6	OBF: Output	Buffer Full Sta	tus bit				
	1 = The outpu	ut buffer still ho	lds a previously	y written word			
	0 = The outpu	ut buffer has be	een read				
bit 5	IBOV: Input B	Buffer Overflow	Detect bit (in N	/licroprocessor	mode)		
	1 = A write oc	curred when a	previously input	word has not b	een read (must	be cleared in se	oftware)
	0 = No overflo	ow occurred					
bit 4	PSPMODE: F	Parallel Slave F	Port Mode Sele	ct bit			
	1 = Parallel S 0 = General p	lave Port mode	e ide				
bit 3		ted: Read as '	0'				
bit 2	TRISE2: RE2	Direction Con	trol bit				
	1 = Input						
	0 = Output						
bit 1	TRISE1: RE1	Direction Con	trol bit				
	1 = Input						
	0 = Output						
bit 0	TRISE0: RE0	Direction Con	trol bit				
	1 = Input						
	0 = Output						

REGISTER 10-1: TRISE REGISTER (40/44-PIN DEVICES ONLY)



17.4.17.1 Bus Collision During a Start Condition

During a Start condition, a bus collision occurs if:

- a) SDA or SCL is sampled low at the beginning of the Start condition (Figure 17-26).
- b) SCL is sampled low before SDA is asserted low (Figure 17-27).

During a Start condition, both the SDA and the SCL pins are monitored.

If the SDA pin is already low, or the SCL pin is already low, then all of the following occur:

- the Start condition is aborted,
- · the BCLIF flag is set and
- the MSSP module is reset to its Idle state (Figure 17-26).

The Start condition begins with the SDA and SCL pins deasserted. When the SDA pin is sampled high, the Baud Rate Generator is loaded from SSPADD<6:0> and counts down to 0. If the SCL pin is sampled low while SDA is high, a bus collision occurs because it is assumed that another master is attempting to drive a data '1' during the Start condition.

If the SDA pin is sampled low during this count, the BRG is reset and the SDA line is asserted early (Figure 17-28). If, however, a '1' is sampled on the SDA pin, the SDA pin is asserted low at the end of the BRG count. The Baud Rate Generator is then reloaded and counts down to 0; if the SCL pin is sampled as '0' during this time, a bus collision does not occur. At the end of the BRG count, the SCL pin is asserted low.

Note: The reason that bus collision is not a factor during a Start condition is that no two bus masters can assert a Start condition at the exact same time. Therefore, one master will always assert SDA before the other. This condition does not cause a bus collision because the two masters must be allowed to arbitrate the first address following the Start condition. If the address is the same, arbitration must be allowed to continue into the data portion, Repeated Start or Stop conditions.



FIGURE 17-26: BUS COLLISION DURING START CONDITION (SDA ONLY)

NOTES:

EXAMPLE 18-1: CALCULATING BAUD RATE ERROR

For a device with FOSC of 16 MHz, desired baud rate of 9600, Asynchronous mode, 8-bit BRG:								
Desired Baud Rate	=	Fosc/(64 ([SPBRGH:SPBRG] + 1))						
Solving for SPBRGH:SPBRG:								
Х	=	((FOSC/Desired Baud Rate)/64) - 1						
	=	((1600000/9600)/64) – 1						
	=	[25.042] = 25						
Calculated Baud Rate	=	1600000/(64 (25 + 1))						
	=	9615						
Error	=	(Calculated Baud Rate - Desired Baud Rate)/Desired Baud Rate						
	=	(9615 - 9600)/9600 = 0.16%						

TABLE 18-2: REGISTERS ASSOCIATED WITH BAUD RATE GENERATOR

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page	
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	51	
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	51	
BAUDCON	ABDOVF	RCIDL	RXDTP	TXCKP	BRG16	—	WUE	ABDEN	51	
SPBRGH	EUSART E	EUSART Baud Rate Generator Register High Byte								
SPBRG	EUSART E	Baud Rate G	Generator R	egister Low	[,] Byte				51	

Legend: — = unimplemented, read as '0'. Shaded cells are not used by the BRG.

18.1.3 AUTO-BAUD RATE DETECT

The Enhanced USART module supports the automatic detection and calibration of baud rate. This feature is active only in Asynchronous mode and while the WUE bit is clear.

The automatic baud rate measurement sequence (Figure 18-1) begins whenever a Start bit is received and the ABDEN bit is set. The calculation is self-averaging.

In the Auto-Baud Rate Detect (ABD) mode, the clock to the BRG is reversed. Rather than the BRG clocking the incoming RX signal, the RX signal is timing the BRG. In ABD mode, the internal Baud Rate Generator is used as a counter to time the bit period of the incoming serial byte stream.

Once the ABDEN bit is set, the state machine will clear the BRG and look for a Start bit. The Auto-Baud Rate Detect must receive a byte with the value 55h (ASCII "U", which is also the LIN bus Sync character) in order to calculate the proper bit rate. The measurement is taken over both a low and a high bit time in order to minimize any effects caused by asymmetry of the incoming signal. After a Start bit, the SPBRG begins counting up, using the preselected clock source on the first rising edge of RX. After eight bits on the RX pin or the fifth rising edge, an accumulated value totalling the proper BRG period is left in the SPBRGH:SPBRG register pair. Once the 5th edge is seen (this should correspond to the Stop bit), the ABDEN bit is automatically cleared.

If a rollover of the BRG occurs (an overflow from FFFFh to 0000h), the event is trapped by the ABDOVF status bit (BAUDCON<7>). It is set in hardware by BRG rollovers and can be set or cleared by the user in software. ABD mode remains active after rollover events and the ABDEN bit remains set (Figure 18-2).

While calibrating the baud rate period, the BRG registers are clocked at 1/8th the preconfigured clock rate. Note that the BRG clock will be configured by the BRG16 and BRGH bits. Independent of the BRG16 bit setting, both the SPBRG and SPBRGH will be used as a 16-bit counter. This allows the user to verify that no carry occurred for 8-bit modes by checking for 00h in the SPBRGH register. Refer to Table 18-4 for counter clock rates to the BRG.

While the ABD sequence takes place, the EUSART state machine is held in Idle. The RCIF interrupt is set once the fifth rising edge on RX is detected. The value in the RCREG needs to be read to clear the RCIF interrupt. The contents of RCREG should be discarded.

- Note 1: If the WUE bit is set with the ABDEN bit, Auto-Baud Rate Detection will occur on the byte *following* the Break character.
 - 2: It is up to the user to determine that the incoming character baud rate is within the range of the selected BRG clock source. Some combinations of oscillator frequency and EUSART baud rates are not possible due to bit error rates. Overall system timing and communication baud rates must be taken into consideration when using the Auto-Baud Rate Detection feature.

TABLE 18-4:BRG COUNTERCLOCK RATES

BRG16	BRGH	BRG Counter Clock		
0	0	Fosc/512		
0	1	Fosc/128		
1	0	Fosc/128		
1	1	Fosc/32		

Note: During the ABD sequence, SPBRG and SPBRGH are both used as a 16-bit counter, independent of BRG16 setting.

18.1.3.1 ABD and EUSART Transmission

Since the BRG clock is reversed during ABD acquisition, the EUSART transmitter cannot be used during ABD. This means that whenever the ABDEN bit is set, TXREG cannot be written to. Users should also ensure that ABDEN does not become set during a transmit sequence. Failing to do this may result in unpredictable EUSART operation.

EUSART ASYNCHRONOUS 18.2.2 RECEIVER

The receiver block diagram is shown in Figure 18-6. The data is received on the RX pin and drives the data recovery block. The data recovery block is actually a high-speed shifter operating at x16 times the baud rate, whereas the main receive serial shifter operates at the bit rate or at Fosc. This mode would typically be used in RS-232 systems.

To set up an Asynchronous Reception:

- Initialize the SPBRGH:SPBRG registers for the 1. appropriate baud rate. Set or clear the BRGH and BRG16 bits, as required, to achieve the desired baud rate.
- 2. Enable the asynchronous serial port by clearing bit, SYNC, and setting bit, SPEN.
- 3. If interrupts are desired, set enable bit, RCIE.
- If 9-bit reception is desired, set bit, RX9. 4
- 5. Enable the reception by setting bit, CREN.
- 6. Flag bit, RCIF, will be set when reception is complete and an interrupt will be generated if enable bit, RCIE, was set.
- 7. Read the RCSTA register to get the 9th bit (if enabled) and determine if any error occurred during reception.
- 8. Read the 8-bit received data by reading the RCREG register.
- 9. If any error occurred, clear the error by clearing enable bit, CREN.
- 10. If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

FIGURE 18-6:

SETTING UP 9-BIT MODE WITH 18.2.3 ADDRESS DETECT

This mode would typically be used in RS-485 systems. To set up an Asynchronous Reception with Address Detect Enable:

- Initialize the SPBRGH:SPBRG registers for the 1. appropriate baud rate. Set or clear the BRGH and BRG16 bits, as required, to achieve the desired baud rate.
- 2. Enable the asynchronous serial port by clearing the SYNC bit and setting the SPEN bit.
- If interrupts are required, set the RCEN bit and 3. select the desired priority level with the RCIP bit.
- Set the RX9 bit to enable 9-bit reception. 4.
- 5. Set the ADDEN bit to enable address detect.
- Enable reception by setting the CREN bit. 6.
- 7. The RCIF bit will be set when reception is complete. The interrupt will be Acknowledged if the RCIE and GIE bits are set.
- Read the RCSTA register to determine if any 8. error occurred during reception, as well as read bit 9 of data (if applicable).
- Read RCREG to determine if the device is being addressed.
- 10. If any error occurred, clear the CREN bit.
- 11. If the device has been addressed, clear the ADDEN bit to allow all received data into the receive buffer and interrupt the CPU.



NOTES:

20.9 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 20-4. Since the analog pins are connected to a digital output, they have reverse biased diodes to VDD and Vss. The analog input, therefore, must be between Vss and VDD. If the input voltage deviates from this

range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up condition may occur. A maximum source impedance of 10 k Ω is recommended for the analog sources. Any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current.





TABLE 20-1: REGISTERS ASSOCIATED WITH COMPARATOR MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
CMCON	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	51
CVRCON	CVREN	CVROE	CVRR	CVRSS	CVR3	CVR2	CVR1	CVR0	51
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	52
PIR2	OSCFIF	CMIF	_	EEIF	BCLIF	HLVDIF	TMR3IF	CCP2IF	52
PIE2	OSCFIE	CMIE	_	EEIE	BCLIE	HLVDIE	TMR3IE	CCP2IE	52
IPR2	OSCFIP	CMIP	—	EEIP	BCLIP	HLVDIP	TMR3IP	CCP2IP	52
PORTA	RA7 ⁽¹⁾	RA6 ⁽¹⁾	RA5	RA4	RA3	RA2	RA1	RA0	52
LATA	LATA7 ⁽¹⁾	LATA6 ⁽¹⁾	PORTA Data Latch Register (Read and Write to Data Latch)				52		
TRISA	TRISA7 ⁽¹⁾	TRISA6 ⁽¹⁾	PORTA Data Direction Register					52	

Legend: — = unimplemented, read as '0'. Shaded cells are unused by the comparator module.

Note 1: PORTA<7:6> and their direction and latch bits are individually configured as port pins based on various primary oscillator modes. When disabled, these bits are read as '0'.

CPFSGT	Compare f with W, Skip if f > W					
Syntax:	CPFSGT	CPFSGT f {,a}				
Operands:	$0 \leq f \leq 255$					
	a ∈ [0,1]					
Operation:	(f) – (W), skip if (f) > ((unsigned c	(f) – (W), skip if (f) > (W) (unsigned comparison)				
Status Affected:	None	None				
Encoding:	0110	0110 010a ffff ffff				
Description:	Compares t location 'f t performing If the content contents of instruction i executed in two-cycle in If 'a' is '0', tl If 'a' is '0', tl If 'a' is '0', at set is enabl in Indexed I mode when Section 24. Bit-Oriente Literal Offs 1	Compares the contents of data memory location 'f' to the contents of the W by performing an unsigned subtraction. If the contents of 'f' are greater than the contents of WREG, then the fetched instruction is discarded and a NOP is executed instead, making this a two-cycle instruction. If 'a' is '0', the Access Bank is selected. If 'a' is '0', the Access Bank is selected. If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See Section 24.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode" for details. 1				
Cycles:	1(2)	1(2)				
-	Note: 3 cy	Note: 3 cycles if skip and followed				
	by a	2-word instruc	ction.			
Q Cycle Activity:			0.4			
Q1 Docodo	Q2 Road	Q3 Process	Q4 No			
Decode	register 'f'	Data	operation			
lf skip:						
Q1	Q2	Q3	Q4			
No	No	No	No			
operation	operation	operation	operation			
	a by 2-word in:		04			
No	No	No	No			
operation	operation	operation	operation			
No	No	No	No			
operation	operation	operation	operation			
Example:	HERE NGREATER	HERE CPFSGT REG, 0 NGREATER :				
Defens lestruction						
PC.	uon = Ad	on = Address (HERE) = ?				
Ŵ	= ?					
After Instruction	n.					
If REG	> W;					
PC	= Ad	dress (GREAT	TER)			
If REG	≤ W;	≤ W;				
PC	= A0	uiess (NGREA	ATEK)			

CPFSLT		Compare	Compare f with W, Skip if f < W					
Syntax:		CPFSLT f	CPFSLT f {,a}					
Operands:		0 ≤ f ≤ 255 a ∈ [0,1]	$\begin{array}{l} 0 \leq f \leq 255 \\ a \in \ [0,1] \end{array}$					
Operation:		(f) – (W), skip if (f) < ((unsigned c	(f) – (W), skip if (f) < (W) (unsigned comparison)					
Statu	s Affected:	None	None					
Enco	ding:	0110	000a ff	ff	ffff			
Description:		Compares t location 'f' tu performing J If the conten contents of instruction is executed in two-cycle in If 'a' is '0', tu If 'a' is '1', tu GPR bank (Compares the contents of data memory location 'f' to the contents of W by performing an unsigned subtraction. If the contents of 'f' are less than the contents of W, then the fetched instruction is discarded and a NOP is executed instead, making this a two-cycle instruction. If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default)					
Word	ls:	1	1					
Cycles:		1(2) Note: 3 c by a	1(2) Note: 3 cycles if skip and followed by a 2-word instruction.					
		02	03		04			
1	Decode	Read	Process		No			
		register 'f'	Data	ор	operation			
lf sk	ip:							
1	Q1	Q2	Q3		Q4			
	operation	operation	operation	op	NO operation			
lf sk	ip and followed	d by 2-word ins	struction:					
	Q1	Q2	Q3		Q4			
	No	No	No		No			
	operation	operation	operation	ор	operation			
	operation	operation	operation	ор	operation			
Example:		HERE C NLESS : LESS :	HERE CPFSLT REG, 1 NLESS : LESS :					
	Before Instruc PC W After Instructic	tion = Ad = ?	n = Address (HERE) = ?					
If REG PC If REG PC		< W; = Ad	dress (LESS	;)				
		= Ad	= Address (NLESS)					

24.2.5 SPECIAL CONSIDERATIONS WITH MICROCHIP MPLAB[®] IDE TOOLS

The latest versions of Microchip's software tools have been designed to fully support the extended instruction set of the PIC18F2420/2520/4420/4520 family of devices. This includes the MPLAB C18 C compiler, MPASM assembly language and MPLAB Integrated Development Environment (IDE).

When selecting a target device for software development, MPLAB IDE will automatically set default Configuration bits for that device. The default setting for the XINST Configuration bit is '0', disabling the extended instruction set and Indexed Literal Offset Addressing mode. For proper execution of applications developed to take advantage of the extended instruction set, XINST must be set during programming.

To develop software for the extended instruction set, the user must enable support for the instructions and the Indexed Addressing mode in their language tool(s). Depending on the environment being used, this may be done in several ways:

- A menu option, or dialog box within the environment, that allows the user to configure the language tool and its settings for the project
- · A command line option
- · A directive in the source code

These options vary between different compilers, assemblers and development environments. Users are encouraged to review the documentation accompanying their development systems for the appropriate information.

FIGURE 26-1: PIC18F2420/2520/4420/4520 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)







FIGURE 27-17: TYPICAL AND MAXIMUM SEC_RUN CURRENT vs. Vdd ACROSS TEMPERATURE (T10SC IN LOW-POWER MODE)

FIGURE 27-18: TYPICAL AND MAXIMUM SEC_IDLE CURRENT vs. VDD ACROSS TEMPERATURE (T10SC IN LOW-POWER MODE)



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