Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f4420-i-ml

TABLE 2-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

| Osc Type	Crystal Freq	Typical Capacitor Values Tested:	
		C1	C2
LP	32 kHz	30 pF	30 pF
XT	1 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	10 MHz	15 pF	15 pF
	20 MHz	15 pF	15 pF
	25 MHz	0 pF	5 pF
	25 MHz	15 pF	15 pF

Capacitor values are for design guidance only.

These capacitors were tested with the crystals listed below for basic start-up and operation. **These values are not optimized.**

Different capacitor values may be required to produce acceptable oscillator operation. The user should test the performance of the oscillator over the expected V_{DD} and temperature range for the application.

See the notes following this table for additional information.

Crystals Used:	
32 kHz	4 MHz
25 MHz	10 MHz
1 MHz	20 MHz

Note 1: Higher capacitance increases the stability of the oscillator but also increases the start-up time.

2: When operating below 3V V_{DD}, or when using certain ceramic resonators at any voltage, it may be necessary to use the HS mode or switch to a crystal oscillator.

3: Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.

4: Rs may be required to avoid overdriving crystals with low drive level specification.

5: Always verify oscillator performance over the V_{DD} and temperature range that is expected for the application.

An external clock source may also be connected to the OSC1 pin in the HS mode, as shown in Figure 2-2.

FIGURE 2-2: EXTERNAL CLOCK INPUT OPERATION (HS OSC CONFIGURATION)
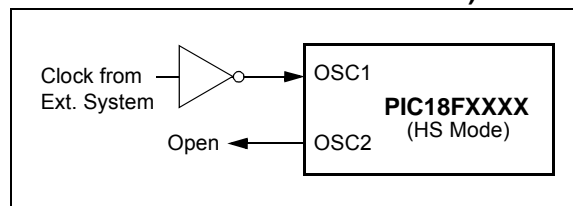

2.3 External Clock Input

The EC and ECIO Oscillator modes require an external clock source to be connected to the OSC1 pin. There is no oscillator start-up time required after a Power-on Reset or after an exit from Sleep mode.

In the EC Oscillator mode, the oscillator frequency divided by 4 is available on the OSC2 pin. This signal may be used for test purposes or to synchronize other logic. Figure 2-3 shows the pin connections for the EC Oscillator mode.

FIGURE 2-3: EXTERNAL CLOCK INPUT OPERATION (EC CONFIGURATION)
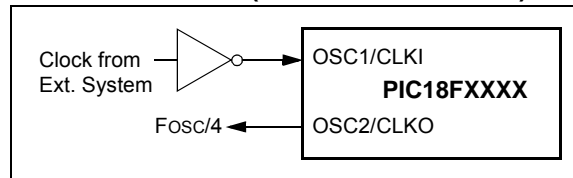
The ECIO Oscillator mode functions like the EC mode, except that the OSC2 pin becomes an additional general purpose I/O pin. The I/O pin becomes bit 6 of PORTA (RA6). Figure 2-4 shows the pin connections for the ECIO Oscillator mode.

FIGURE 2-4: EXTERNAL CLOCK INPUT OPERATION (ECIO CONFIGURATION)
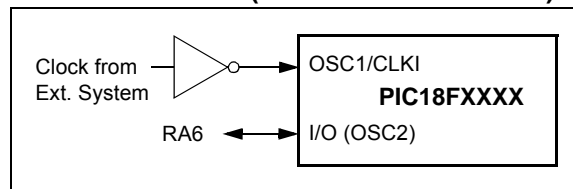
2.8 Effects of Power-Managed Modes on the Various Clock Sources

When PRI_IDLE mode is selected, the designated primary oscillator continues to run without interruption. For all other power-managed modes, the oscillator using the OSC1 pin is disabled. The OSC1 pin (and OSC2 pin, if used by the oscillator) will stop oscillating.

In secondary clock modes (SEC_RUN and SEC_IDLE), the Timer1 oscillator is operating and providing the device clock. The Timer1 oscillator may also run in all power-managed modes if required to clock Timer1 or Timer3.

In internal oscillator modes (RC_RUN and RC_IDLE), the internal oscillator block provides the device clock source. The 31 kHz INTRC output can be used directly to provide the clock and may be enabled to support various special features, regardless of the power-managed mode (see **Section 23.2 "Watchdog Timer (WDT)"**, **Section 23.3 "Two-Speed Start-up"** and **Section 23.4 "Fail-Safe Clock Monitor"** for more information on WDT, Fail-Safe Clock Monitor and Two-Speed Start-up). The INTOSC output at 8 MHz may be used directly to clock the device or may be divided down by the postscaler. The INTOSC output is disabled if the clock is provided directly from the INTRC output.

If Sleep mode is selected, all clock sources are stopped. Since all the transistor switching currents have been stopped, Sleep mode achieves the lowest current consumption of the device (only leakage currents).

Enabling any on-chip feature that will operate during Sleep will increase the current consumed during Sleep. The INTRC is required to support WDT operation. The Timer1 oscillator may be operating to support a Real-Time Clock. Other features may be operating that do not require a device clock source (i.e., MSSP slave, PSP, INTx pins and others). Peripherals that may add significant current consumption are listed in **Section 26.2 "DC Characteristics".**

2.9 Power-up Delays

Power-up delays are controlled by two timers so that no external Reset circuitry is required for most applications. The delays ensure that the device is kept in Reset until the device power supply is stable under normal circumstances and the primary clock is operating and stable. For additional information on power-up delays, see **Section 4.5 "Device Reset Timers"**.

The first timer is the Power-up Timer (PWRT), which provides a fixed delay on power-up (parameter 33, Table 26-10). It is enabled by clearing (= 0) the PWRTEN Configuration bit.

The second timer is the Oscillator Start-up Timer (OST), intended to keep the chip in Reset until the crystal oscillator is stable (LP, XT and HS modes). The OST does this by counting 1024 oscillator cycles before allowing the oscillator to clock the device.

When the HSPLL Oscillator mode is selected, the device is kept in Reset for an additional 2 ms, following the HS mode OST delay, so the PLL can lock to the incoming clock frequency.

There is a delay of interval, T$_{CSD}$ (parameter 38, Table 26-10), following POR, while the controller becomes ready to execute instructions. This delay runs concurrently with any other delays. This may be the only delay that occurs when any of the EC, RC or INTIO modes are used as the primary clock source.

TABLE 2-3:   OSC1 AND OSC2 PIN STATES IN SLEEP MODE

OSC Mode	OSC1 Pin	OSC2 Pin
RC, INTIO1	Floating, external resistor should pull high	At logic low (clock/4 output)
RCIO	Floating, external resistor should pull high	Configured as PORTA, bit 6
INTIO2	Configured as PORTA, bit 7	Configured as PORTA, bit 6
ECIO	Floating, pulled by external clock	Configured as PORTA, bit 6
EC	Floating, pulled by external clock	At logic low (clock/4 output)
LP, XT and HS	Feedback inverter disabled at quiescent voltage level	Feedback inverter disabled at quiescent voltage level

Note: See Table 4-2 in **Section 4.0 "Reset"** for time-outs due to Sleep and $\overline{MCLR}$ Reset.

TABLE 4-4: **INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)**

Register	Applicable Devices				Power-on Reset, Brown-out Reset	MCLR Resets, WDT Reset, RESET Instruction, Stack Resets	Wake-up via WDT or Interrupt
FSR1H	2420	2520	4420	4520	---- 0000	---- 0000	---- uuuu
FSR1L	2420	2520	4420	4520	xxxx xxxx	uuuu uuuu	uuuu uuuu
BSR	2420	2520	4420	4520	---- 0000	---- 0000	---- uuuu
INDF2	2420	2520	4420	4520	N/A	N/A	N/A
POSTINC2	2420	2520	4420	4520	N/A	N/A	N/A
POSTDEC2	2420	2520	4420	4520	N/A	N/A	N/A
PREINC2	2420	2520	4420	4520	N/A	N/A	N/A
PLUSW2	2420	2520	4420	4520	N/A	N/A	N/A
FSR2H	2420	2520	4420	4520	---- 0000	---- 0000	---- uuuu
FSR2L	2420	2520	4420	4520	xxxx xxxx	uuuu uuuu	uuuu uuuu
STATUS	2420	2520	4420	4520	---x xxxx	---u uuuu	---u uuuu
TMR0H	2420	2520	4420	4520	0000 0000	0000 0000	uuuu uuuu
TMR0L	2420	2520	4420	4520	xxxx xxxx	uuuu uuuu	uuuu uuuu
T0CON	2420	2520	4420	4520	1111 1111	1111 1111	uuuu uuuu
OSCCON	2420	2520	4420	4520	0100 q000	0100 q000	uuuu quuu
HLVDCON	2420	2520	4420	4520	0-00 0101	0-00 0101	u-uu uuuu
WDTCON	2420	2520	4420	4520	---- ---0	---- ---0	---- ---u
RCON[4]	2420	2520	4420	4520	0q-1 11q0	0q-q qquu	uq-u qquu
TMR1H	2420	2520	4420	4520	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1L	2420	2520	4420	4520	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	2420	2520	4420	4520	0000 0000	u0uu uuuu	uuuu uuuu
TMR2	2420	2520	4420	4520	0000 0000	0000 0000	uuuu uuuu
PR2	2420	2520	4420	4520	1111 1111	1111 1111	1111 1111
T2CON	2420	2520	4420	4520	-000 0000	-000 0000	-uuu uuuu
SSPBUF	2420	2520	4420	4520	xxxx xxxx	uuuu uuuu	uuuu uuuu
SSPADD	2420	2520	4420	4520	0000 0000	0000 0000	uuuu uuuu
SSPSTAT	2420	2520	4420	4520	0000 0000	0000 0000	uuuu uuuu
SSPCON1	2420	2520	4420	4520	0000 0000	0000 0000	uuuu uuuu
SSPCON2	2420	2520	4420	4520	0000 0000	0000 0000	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition.
Shaded cells indicate conditions do not apply for the designated device.

Note 1: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

3: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.

4: See Table 4-3 for Reset value for specific condition.

5: Bits 6 and 7 of PORTA, LATA and TRISA are enabled depending on the oscillator mode selected. When not enabled as PORTA pins, they are disabled and read '0'.

6: The Reset value of the PCFG bits depends on the value of the PBADEN Configuration bit (CONFIG3H<1>). When PBADEN = 1, PCFG<2:0> = 000; when PBADEN = 0, PCFG<2:0> = 111.

7.0 DATA EEPROM MEMORY

The data EEPROM is a nonvolatile memory array, separate from the data RAM and program memory, that is used for long-term storage of program data. It is not directly mapped in either the register file or program memory space but is indirectly addressed through the Special Function Registers (SFRs). The EEPROM is readable and writable during normal operation over the entire VDD range.

Five SFRs are used to read and write to the data EEPROM as well as the program memory. They are:

• EECON1
• EECON2
• EEDATA
• EEADR

The data EEPROM allows byte read and write. When interfacing to the data memory block, EEDATA holds the 8-bit data for read/write and the EEADR register holds the address of the EEPROM location being accessed.

The EEPROM data memory is rated for high erase/write cycle endurance. A byte write automatically erases the location and writes the new data (erase-before-write). The write time is controlled by an on-chip timer; it will vary with voltage and temperature as well as from chip to chip. Please refer to parameter D122 (Table 26-1 in **Section 26.0 "Electrical Characteristics"**) for exact limits.

7.1 EEADR Register

The EEADR register is used to address the data EEPROM for read and write operations. The 8-bit range of the register can address a memory range of 256 bytes (00h to FFh).

7.2 EECON1 and EECON2 Registers

Access to the data EEPROM is controlled by two registers: EECON1 and EECON2. These are the same registers which control access to the program memory and are used in a similar manner for the data EEPROM.

The EECON1 register (Register 7-1) is the control register for data and program memory access. Control bit EEPGD determines if the access will be to program or data EEPROM memory. When clear, operations will access the data EEPROM memory. When set, program memory is accessed.

Control bit, CFGS, determines if the access will be to the Configuration registers or to program memory/data EEPROM memory. When set, subsequent operations access Configuration registers. When CFGS is clear, the EEPGD bit selects either program Flash or data EEPROM memory.

The WREN bit, when set, will allow a write operation. On power-up, the WREN bit is clear. The WRERR bit is set in hardware when the WR bit is set and cleared when the internal programming timer expires and the write operation is complete.

Note:	During normal operation, the WRERR may read as '1'. This can indicate that a write operation was prematurely terminated by a Reset, or a write operation was attempted improperly.

The WR control bit initiates write operations. The bit can be set but not cleared in software. It is only cleared in hardware at the completion of the write operation.

Note:	The EEIF interrupt flag bit (PIR2<4>) is set when the write is complete. It must be cleared in software.

Control bits, RD and WR, start read and erase/write operations, respectively. These bits are set by firmware and cleared by hardware at the completion of the operation.

The RD bit cannot be set when accessing program memory (EEPGD = 1). Program memory is read using table read instructions. See **Section 6.1 "Table Reads and Table Writes"** regarding table reads.

The EECON2 register is not a physical register. It is used exclusively in the memory write and erase sequences. Reading EECON2 will read all '0's.

REGISTER 9-7:   PIE2: PERIPHERAL INTERRUPT ENABLE REGISTER 2

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OSCFIE	CMIE	—	EEIE	BCLIE	HLVDIE	TMR3IE	CCP2IE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 7   **OSCFIE:** Oscillator Fail Interrupt Enable bit

   1 = Enabled
   0 = Disabled

bit 6   **CMIE:** Comparator Interrupt Enable bit

   1 = Enabled
   0 = Disabled

bit 5   **Unimplemented:** Read as '0'

bit 4   **EEIE:** Data EEPROM/Flash Write Operation Interrupt Enable bit

   1 = Enabled
   0 = Disabled

bit 3   **BCLIE:** Bus Collision Interrupt Enable bit

   1 = Enabled
   0 = Disabled

bit 2   **HLVDIE:** High/Low-Voltage Detect Interrupt Enable bit

   1 = Enabled
   0 = Disabled

bit 1   **TMR3IE:** TMR3 Overflow Interrupt Enable bit

   1 = Enabled
   0 = Disabled

bit 0   **CCP2IE:** CCP2 Interrupt Enable bit

   1 = Enabled
   0 = Disabled

15.3 Compare Mode

In Compare mode, the 16-bit CCPRx register value is constantly compared against either the TMR1 or TMR3 register pair value. When a match occurs, the CCPx pin can be:

• driven high
• driven low
• toggled (high-to-low or low-to-high)
• remain unchanged (that is, reflects the state of the I/O latch)

The action on the pin is based on the value of the mode select bits (CCPxM<3:0>). At the same time, the interrupt flag bit, CCPxIF, is set.

15.3.1 CCP PIN CONFIGURATION

The user must configure the CCPx pin as an output by clearing the appropriate TRIS bit.

Note:	Clearing the CCP2CON register will force the RB3 or RC1 compare output latch (depending on device configuration) to the default low level. This is not the PORTB or PORTC I/O data latch.

15.3.2 TIMER1/TIMER3 MODE SELECTION

Timer1 and/or Timer3 must be running in Timer mode or Synchronized Counter mode if the CCP module is using the compare feature. In Asynchronous Counter mode, the compare operation may not work.

15.3.3 SOFTWARE INTERRUPT MODE

When the Generate Software Interrupt mode is chosen (CCPxM<3:0> = 1010), the corresponding CCPx pin is not affected. A CCP interrupt is generated when the CCPxIF interrupt flag is set while the CCPxIE bit is set.

15.3.4 SPECIAL EVENT TRIGGER

Both CCP modules are equipped with a Special Event Trigger. This is an internal hardware signal generated in Compare mode to trigger actions by other modules. The Special Event Trigger is enabled by selecting the Compare Special Event Trigger mode (CCPxM<3:0> = 1011).

For either CCP module, the Special Event Trigger resets the Timer register pair for whichever timer resource is currently assigned as the module's time base. This allows the CCPRx registers to serve as a programmable Period register for either timer.

The Special Event Trigger for CCP2 can also start an A/D conversion. In order to do this, the A/D Converter must already be enabled.

FIGURE 15-2: COMPARE MODE OPERATION BLOCK DIAGRAM
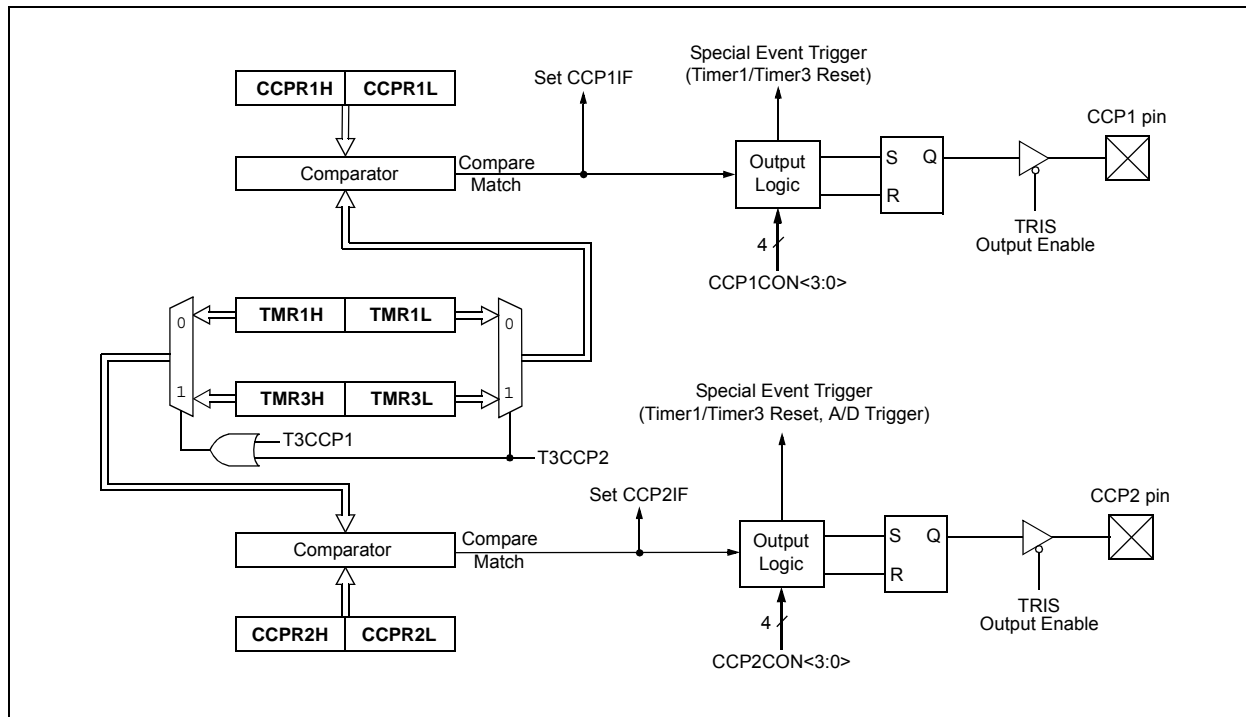
17.3.2 OPERATION

When initializing the SPI, several options need to be specified. This is done by programming the appropriate control bits (SSPCON1<5:0> and SSPSTAT<7:6>). These control bits allow the following to be specified:

- Master mode (SCK is the clock output)
- Slave mode (SCK is the clock input)
- Clock Polarity (Idle state of SCK)
- Data Input Sample Phase (middle or end of data output time)
- Clock Edge (output data on rising/falling edge of SCK)
- Clock Rate (Master mode only)
- Slave Select mode (Slave mode only)

The MSSP consists of a transmit/receive shift register (SSPSR) and a buffer register (SSPBUF). The SSPSR shifts the data in and out of the device, MSb first. The SSPBUF holds the data that was written to the SSPSR until the received data is ready. Once the 8 bits of data have been received, that byte is moved to the SSPBUF register. Then, the Buffer Full detect bit, BF (SSPSTAT<0>) and the interrupt flag bit, SSPIF, are set. This double-buffering of the received data (SSPBUF) allows the next byte to start reception before reading the data that was just received. Any write to the SSPBUF register during transmission/reception of data will be ignored and the write collision detect bit, WCOL (SSPCON1<7>), will be set. User software must clear the WCOL bit so that it can be determined if the following write(s) to the SSPBUF register completed successfully.

When the application software is expecting to receive valid data, the SSPBUF should be read before the next byte of data to transfer is written to the SSPBUF. The Buffer Full bit, BF (SSPSTAT<0>), indicates when SSPBUF has been loaded with the received data (transmission is complete). When the SSPBUF is read, the BF bit is cleared. This data may be irrelevant if the SPI is only a transmitter. Generally, the MSSP interrupt is used to determine when the transmission/reception has completed. The SSPBUF must be read and/or written. If the interrupt method is not going to be used, then software polling can be done to ensure that a write collision does not occur. Example 17-1 shows the loading of the SSPBUF (SSPSR) for data transmission.

The SSPSR is not directly readable or writable and can only be accessed by addressing the SSPBUF register. Additionally, the MSSP Status register (SSPSTAT) indicates the various status conditions.

> **Note:** The SSPBUF register cannot be used with read-modify-write instructions such as BCF, BTFSC and COMF, etc.

EXAMPLE 17-1:   LOADING THE SSPBUF (SSPSR) REGISTER

```
LOOP    BTFSS   SSPSTAT, BF     ;Has data been received (transmit complete)?
        BRA     LOOP            ;No
        MOVF    SSPBUF, W       ;WREG reg = contents of SSPBUF

        MOVWF   RXDATA          ;Save in user RAM, if data is meaningful

        MOVF    TXDATA, W       ;W reg = contents of TXDATA
        MOVWF   SSPBUF          ;New data to xmit
```

> **Note:** To avoid lost data in Master mode, a read of the SSPBUF must be performed to clear the Buffer Full (BF) detect bit (SSPSTAT<0>) between each transmission.

REGISTER 17-4:   SSPCON1: MSSP CONTROL REGISTER 1 (I2C™ MODE)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WCOL	SSPOV	SSPEN[1]	CKP	SSPM3	SSPM2	SSPM1	SSPM0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 7   **WCOL:** Write Collision Detect bit

In Master Transmit mode:
1 = A write to the SSPBUF register was attempted while the I2C conditions were not valid for a transmission to be started (must be cleared in software)
0 = No collision

In Slave Transmit mode:
1 = The SSPBUF register is written while it is still transmitting the previous word (must be cleared in software)
0 = No collision

In Receive mode (Master or Slave modes):
This is a "don't care" bit.

bit 6   **SSPOV:** Receive Overflow Indicator bit

In Receive mode:
1 = A byte is received while the SSPBUF register is still holding the previous byte (must be cleared in software)
0 = No overflow

In Transmit mode:
This is a "don't care" bit in Transmit mode.

bit 5   **SSPEN:** Master Synchronous Serial Port Enable bit[1]

1 = Enables the serial port and configures the SDA and SCL pins as the serial port pins
0 = Disables serial port and configures these pins as I/O port pins

bit 4   **CKP:** SCK Release Control bit

In Slave mode:
1 = Releases clock
0 = Holds clock low (clock stretch), used to ensure data setup time

In Master mode:
Unused in this mode.

bit 3-0   **SSPM<3:0>:** Master Synchronous Serial Port Mode Select bits[2]

1111 = I2C Slave mode, 10-bit address with Start and Stop bit interrupts enabled
1110 = I2C Slave mode, 7-bit address with Start and Stop bit interrupts enabled
1011 = I2C Firmware Controlled Master mode (Slave Idle)
1000 = I2C Master mode, clock = FOSC/(4 * (SSPADD + 1))
0111 = I2C Slave mode, 10-bit address
0110 = I2C Slave mode, 7-bit address
Bit combinations not specifically listed here are either reserved or implemented in SPI mode only.

Note 1:   When enabled, the SDA and SCL pins must be properly configured as inputs or outputs.

17.4.2   OPERATION

The MSSP module functions are enabled by setting the MSSP Enable bit, SSPEN (SSPCON1<5>).

The SSPCON1 register allows control of the I^{2}C operation. Four mode selection bits (SSPCON1<3:0>) allow one of the following I^{2}C modes to be selected:

- I^{2}C Master mode, clock = (F$_{OSC}$/4) x (SSPADD + 1)
- I^{2}C Slave mode (7-bit addressing)
- I^{2}C Slave mode (10-bit addressing)
- I^{2}C Slave mode (7-bit addressing) with Start and Stop bit interrupts enabled
- I^{2}C Slave mode (10-bit addressing) with Start and Stop bit interrupts enabled
- I^{2}C Firmware Controlled Master mode, slave is Idle

Selection of any I^{2}C mode, with the SSPEN bit set, forces the SCL and SDA pins to be open-drain, provided these pins are programmed to inputs by setting the appropriate TRISC bits. To ensure proper operation of the module, pull-up resistors must be provided externally to the SCL and SDA pins.

17.4.3   SLAVE MODE

In Slave mode, the SCL and SDA pins must be config-ured as inputs (TRISC<4:3> set). The MSSP module will override the input state with the output data when required (slave-transmitter).

The I^{2}C Slave mode hardware will always generate an interrupt on an address match. Through the mode select bits, the user can also choose to interrupt on Start and Stop bits

When an address is matched, or the data transfer after an address match is received, the hardware automati-cally will generate the Acknowledge ($\overline{ACK}$) pulse and load the SSPBUF register with the received value currently in the SSPSR register.

Any combination of the following conditions will cause the MSSP module not to give this $\overline{ACK}$ pulse:

- The Buffer Full bit, BF (SSPSTAT<0>), was set before the transfer was received.
- The overflow bit, SSPOV (SSPCON2<6>), was set before the transfer was received.

In this case, the SSPSR register value is not loaded into the SSPBUF, but bit, SSPIF (PIR1<3>), is set. The BF bit is cleared by reading the SSPBUF register, while bit SSPOV is cleared through software.

The SCL clock input must have a minimum high and low for proper operation. The high and low times of the I^{2}C specification, as well as the requirement of the MSSP module, are shown in timing parameter 100 and parameter 101.

17.4.3.1   Addressing

Once the MSSP module has been enabled, it waits for a Start condition to occur. Following the Start condition, the 8 bits are shifted into the SSPSR register. All incoming bits are sampled with the rising edge of the clock (SCL) line. The value of register SSPSR<7:1> is compared to the value of the SSPADD register. The address is compared on the falling edge of the eighth clock (SCL) pulse. If the addresses match and the BF and SSPOV bits are clear, the following events occur:

1. The SSPSR register value is loaded into the SSPBUF register.
2. The Buffer Full bit, BF, is set.
3. An $\overline{ACK}$ pulse is generated.
4. MSSP Interrupt Flag bit, SSPIF (PIR1<3>), is set (interrupt is generated, if enabled) on the falling edge of the ninth SCL pulse.

In 10-Bit Addressing mode, two address bytes need to be received by the slave. The five Most Significant bits (MSbs) of the first address byte specify if this is a 10-bit address. Bit, R/$\overline{W}$ (SSPSTAT<2>), must specify a write so the slave device will receive the second address byte. For a 10-bit address, the first byte would equal '11110 A9 A8 0', where 'A9' and 'A8' are the two MSbs of the address. The sequence of events for 10-Bit Addressing mode is as follows, with steps 7 through 9 for the slave-transmitter:

1. Receive first (high) byte of address (bits, SSPIF, BF and UA (SSPSTAT<1>), are set).
2. Update the SSPADD register with second (low) byte of address (clears UA bit and releases the SCL line).
3. Read the SSPBUF register (clears BF bit) and clear flag bit, SSPIF.
4. Receive second (low) byte of address (bits, SSPIF, BF and UA, are set).
5. Update the SSPADD register with the first (high) byte of address. If match releases SCL line, this will clear bit, UA.
6. Read the SSPBUF register (clears BF bit) and clear flag bit, SSPIF.
7. Receive Repeated Start condition.
8. Receive first (high) byte of address (bits, SSPIF and BF, are set).
9. Read the SSPBUF register (clears BF bit) and clear flag bit, SSPIF.
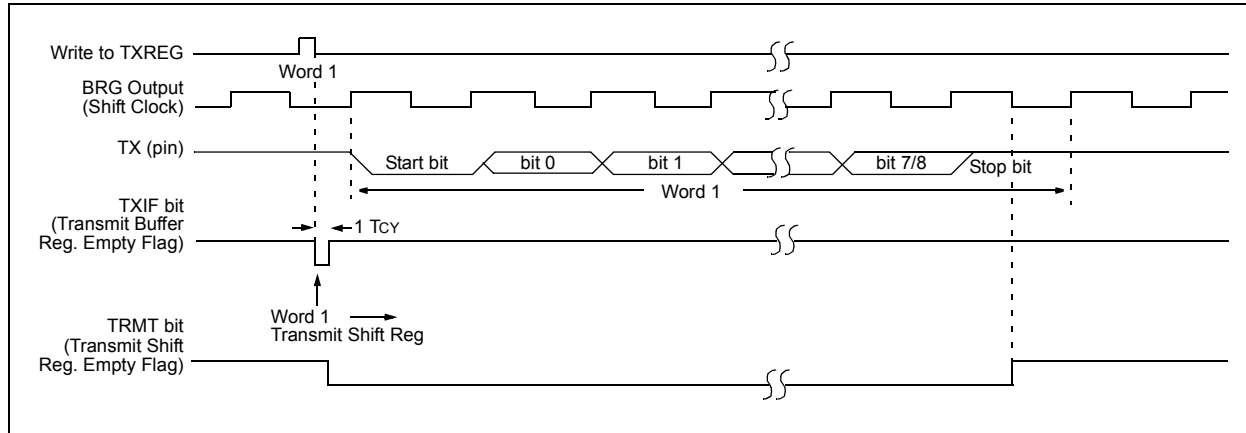
FIGURE 18-4: **ASYNCHRONOUS TRANSMISSION**

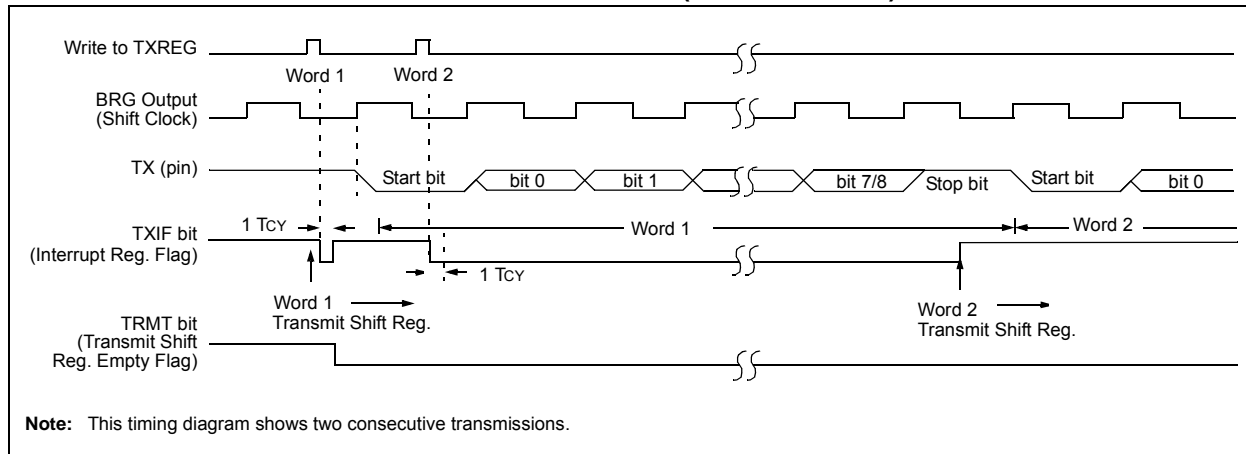**FIGURE 18-5:** **ASYNCHRONOUS TRANSMISSION (BACK TO BACK)**

Note: This timing diagram shows two consecutive transmissions.

TABLE 18-5: **REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	49
PIR1	PSPIF[1]	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	52
PIE1	PSPIE[1]	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	52
IPR1	PSPIP[1]	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	52
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	51
TXREG	EUSART Transmit Register								51
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	51
BAUDCON	ABDOVF	RCIDL	RXDTP	TXCKP	BRG16	—	WUE	ABDEN	51
SPBRGH	EUSART Baud Rate Generator Register High Byte								51
SPBRG	EUSART Baud Rate Generator Register Low Byte								51

Legend: — = unimplemented locations read as '0'. Shaded cells are not used for asynchronous transmission.

Note 1: Reserved in 28-pin devices; always maintain these bits clear.

FIGURE 20-3: **COMPARATOR OUTPUT BLOCK DIAGRAM**
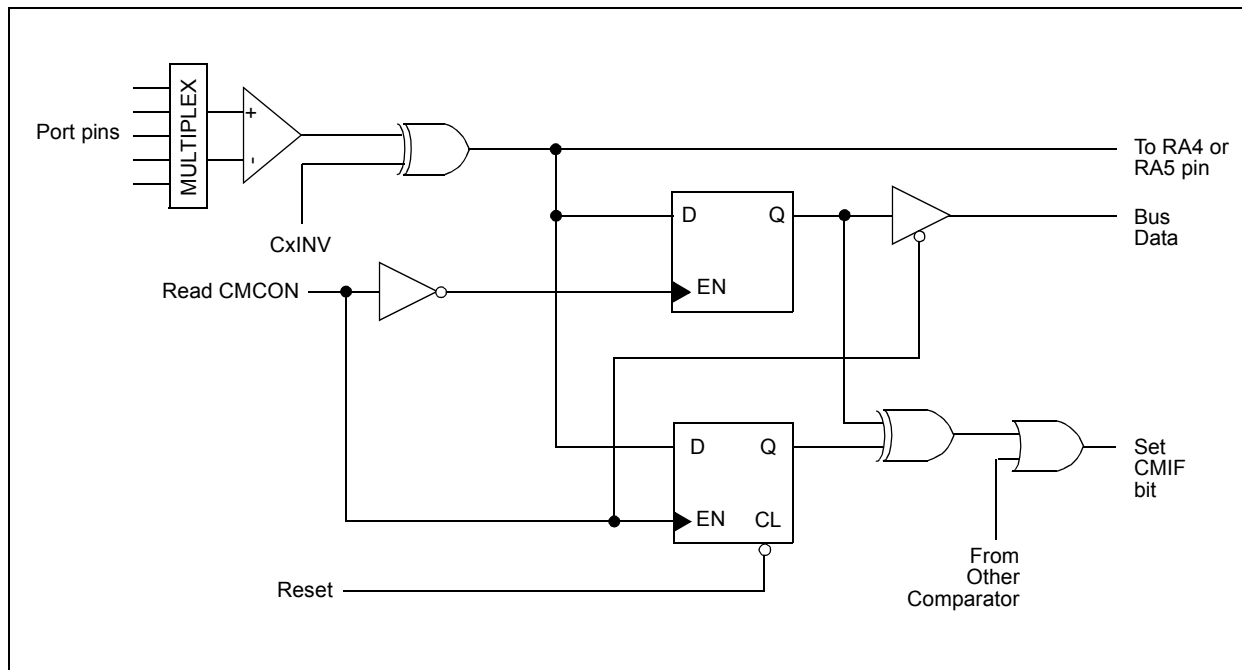
20.6 Comparator Interrupts

The comparator interrupt flag is set whenever there is a change in the output value of either comparator. Software will need to maintain information about the status of the output bits, as read from CMCON<7:6>, to determine the actual change that occurred. The CMIF bit (PIR2<6>) is the Comparator Interrupt Flag. The CMIF bit must be reset by clearing it. Since it is also possible to write a '1' to this register, a simulated interrupt may be initiated.

Both the CMIE bit (PIE2<6>) and the PEIE bit (INTCON<6>) must be set to enable the interrupt. In addition, the GIE bit (INTCON<7>) must also be set. If any of these bits are clear, the interrupt is not enabled, though the CMIF bit will still be set if an interrupt condition occurs.

Note: If a change in the CMCON register (C1OUT or C2OUT) should occur when a read operation is being executed (start of the Q2 cycle), then the CMIF (PIR2<6>) interrupt flag may not get set.

The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

a) Any read or write of CMCON will end the mismatch condition.

b) Clear flag bit, CMIF.

A mismatch condition will continue to set flag bit, CMIF. Reading CMCON will end the mismatch condition and allow flag bit, CMIF, to be cleared.

20.7 Comparator Operation During Sleep

When a comparator is active and the device is placed in Sleep mode, the comparator remains active and the interrupt is functional if enabled. This interrupt will wake-up the device from Sleep mode when enabled. Each operational comparator will consume additional current, as shown in the comparator specifications. To minimize power consumption while in Sleep mode, turn off the comparators (CM<2:0> = 111) before entering Sleep. If the device wakes up from Sleep, the contents of the CMCON register are not affected.

20.8 Effects of a Reset

A device Reset forces the CMCON register to its Reset state, causing the comparator modules to be turned off (CM<2:0> = 111). However, the input pins (RA0 through RA3) are configured as analog inputs by default on device Reset. The I/O configuration for these pins is determined by the setting of the PCFG<3:0> bits (ADCON1<3:0>). Therefore, device current is minimized when analog inputs are present at Reset time.

24.0 INSTRUCTION SET SUMMARY

PIC18F2420/2520/4420/4520 devices incorporate the standard set of 75 PIC18 core instructions, as well as an extended set of 8 new instructions, for the optimization of code that is recursive or that utilizes a software stack. The extended set is discussed later in this section.

24.1 Standard Instruction Set

The standard PIC18 instruction set adds many enhancements to the previous PIC® MCU instruction sets, while maintaining an easy migration from these PIC MCU instruction sets. Most instructions are a single program memory word (16 bits), but there are four instructions that require two program memory locations.

Each single-word instruction is a 16-bit word divided into an opcode, which specifies the instruction type and one or more operands, which further specify the operation of the instruction.

The instruction set is highly orthogonal and is grouped into four basic categories:

• **Byte-oriented** operations
• **Bit-oriented** operations
• **Literal** operations
• **Control** operations

The PIC18 instruction set summary in Table 24-2 lists **byte-oriented**, **bit-oriented**, **literal** and **control** operations. Table 24-1 shows the opcode field descriptions.

Most **byte-oriented** instructions have three operands:

1. The file register (specified by 'f')
2. The destination of the result (specified by 'd')
3. The accessed memory (specified by 'a')

The file register designator 'f' specifies which file register is to be used by the instruction. The destination designator 'd' specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the WREG register. If 'd' is one, the result is placed in the file register specified in the instruction.

All **bit-oriented** instructions have three operands:

1. The file register (specified by 'f')
2. The bit in the file register (specified by 'b')
3. The accessed memory (specified by 'a')

The bit field designator 'b' selects the number of the bit affected by the operation, while the file register designator 'f' represents the number of the file in which the bit is located.

The **literal** instructions may use some of the following operands:

• A literal value to be loaded into a file register (specified by 'k')
• The desired FSR register to load the literal value into (specified by 'f')
• No operand required (specified by '—')

The **control** instructions may use some of the following operands:

• A program memory address (specified by 'n')
• The mode of the CALL or RETURN instructions (specified by 's')
• The mode of the table read and table write instructions (specified by 'm')
• No operand required (specified by '—')

All instructions are a single word, except for four double-word instructions. These instructions were made double-word to contain the required information in 32 bits. In the second word, the 4 MSbs are '1's. If this second word is executed as an instruction (by itself), it will execute as a NOP.

All single-word instructions are executed in a single instruction cycle, unless a conditional test is true or the program counter is changed as a result of the instruction. In these cases, the execution takes two instruction cycles, with the additional instruction cycle(s) executed as a NOP.

The double-word instructions execute in two instruction cycles.

One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μs. If a conditional test is true, or the program counter is changed as a result of an instruction, the instruction execution time is 2 μs. Two-word branch instructions (if true) would take 3 μs.

Figure 24-1 shows the general formats that the instructions can have. All examples use the convention 'nnh' to represent a hexadecimal number.

The Instruction Set Summary, shown in Table 24-2, lists the standard instructions recognized by the Microchip Assembler (MPASM™).

Section 24.1.1 "Standard Instruction Set" provides a description of each instruction.

PIC18F2420/2520/4420/4520

<table>
<tr><td>POP</td><td colspan="2">Pop Top of Return Stack</td></tr>
<tr><td>Syntax:</td><td colspan="2">POP</td></tr>
<tr><td>Operands:</td><td colspan="2">None</td></tr>
<tr><td>Operation:</td><td colspan="2">(TOS) → bit bucket</td></tr>
<tr><td>Status Affected:</td><td colspan="2">None</td></tr>
<tr><td>Encoding:</td><td colspan="2">0000   0000   0000   0110</td></tr>
<tr><td>Description:</td><td colspan="2">The TOS value is pulled off the return stack and is discarded. The TOS value then becomes the previous value that was pushed onto the return stack. This instruction is provided to enable the user to properly manage the return stack to incorporate a software stack.</td></tr>
<tr><td>Words:</td><td colspan="2">1</td></tr>
<tr><td>Cycles:</td><td colspan="2">1</td></tr>
</table>

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	No operation	POP TOS value	No operation

Example:
```
        POP
        GOTO    NEW
```
Before Instruction
  TOS   =   0031A2h
  Stack (1 level down)   =   014332h

After Instruction
  TOS   =   014332h
  PC   =   NEW

<table>
<tr><td>PUSH</td><td colspan="2">Push Top of Return Stack</td></tr>
<tr><td>Syntax:</td><td colspan="2">PUSH</td></tr>
<tr><td>Operands:</td><td colspan="2">None</td></tr>
<tr><td>Operation:</td><td colspan="2">(PC + 2) → TOS</td></tr>
<tr><td>Status Affected:</td><td colspan="2">None</td></tr>
<tr><td>Encoding:</td><td colspan="2">0000   0000   0000   0101</td></tr>
<tr><td>Description:</td><td colspan="2">The PC + 2 is pushed onto the top of the return stack. The previous TOS value is pushed down on the stack. This instruction allows implementing a software stack by modifying TOS and then pushing it onto the return stack.</td></tr>
<tr><td>Words:</td><td colspan="2">1</td></tr>
<tr><td>Cycles:</td><td colspan="2">1</td></tr>
</table>

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	PUSH PC + 2 onto return stack	No operation	No operation

Example:
```
        PUSH
```
Before Instruction
  TOS   =   345Ah
  PC   =   0124h

After Instruction
  PC   =   0126h
  TOS   =   0126h
  Stack (1 level down)   =   345Ah

26.2   DC Characteristics: Power-Down and Supply Current
PIC18F2420/2520/4420/4520 (Industrial)
PIC18LF2420/2520/4420/4520 (Industrial) (Continued)

PIC18LF2420/2520/4420/4520 (Industrial)	Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
PIC18F2420/2520/4420/4520 (Industrial, Extended)	**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				

Param No.	Device	Typ	Max	Units	Conditions	
	Module Differential Currents (ΔIWDT, ΔIBOR, ΔILVD, ΔIOSCB, ΔIAD)					
D026 (ΔIAD)	**A/D Converter**	0.2	1.0	µA	-40°C to +85°C	VDD = 2.0V	A/D on, not converting
		0.2	1.0	µA	-40°C to +85°C	VDD = 3.0V	
		0.2	1.0	µA	-40°C to +85°C	VDD = 5.0V	
		0.5	4.0	µA	-40°C to +125°C		
D022 (ΔIWDT)	**Watchdog Timer**	1.3	2.2	µA	-40°C	VDD = 2.0V	
		1.4	2.2	µA	+25°C		
		1.6	2.3	µA	+85°C		
		1.9	3.5	µA	-40°C	VDD = 3.0V	
		2.0	3.5	µA	+25°C		
		2.2	3.5	µA	+85°C		
		3.0	7.5	µA	-40°C	VDD = 5.0V	
		3.5	7.5	µA	+25°C		
		3.5	7.8	µA	+85°C		
		4.0	10	µA	+125°C		
D022A (ΔIBOR)	**Brown-out Reset**[4]	35	50	µA	-40°C to +85°C	VDD = 3.0V	
		40	55	µA	-40°C to +85°C	VDD = 5.0V	
		55	65	µA	-40°C to +125°C		
		0	2	µA	-40°C to +85°C		Sleep mode, BOREN<1:0> = 10
		0	5	µA	-40°C to +125°C		
D022B (ΔILVD)	**High/Low-Voltage Detect**[4]	22	38	µA	-40°C to +85°C	VDD = 2.0V	
		25	40	µA	-40°C to +85°C	VDD = 3.0V	
		29	45	µA	-40°C to +85°C	VDD = 5.0V	
		30	45	µA	-40°C to +125°C		

Legend: Shading of rows is to assist in readability of the table.

Note   1:   The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2:   The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:
   OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD or VSS;
   MCLR = VDD; WDT enabled/disabled as specified.

3:   When operation below -10°C is expected, use T1OSC High-Power mode, where LPT1OSC (CONFIG3H<2>) = 0. When operation will always be above -10°C, then the low-power Timer1 oscillator may be selected.

4:   BOR and HLVD enable internal band gap reference. With both modules enabled, current consumption will be less than the sum of both specifications.

26.4 AC (Timing) Characteristics

26.4.1 TIMING PARAMETER SYMBOLOGY

The timing parameter symbols have been created using one of the following formats:

1. TppS2ppS			3. T$_{CC:ST}$	(I^{2}C specifications only)
2. TppS			4. Ts	(I^{2}C specifications only)

T				
	F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

pp				
	cc	CCP1	osc	OSC1
	ck	CLKO	rd	$\overline{RD}$
	cs	$\overline{CS}$	rw	$\overline{RD}$ or $\overline{WR}$
	di	SDI	sc	SCK
	do	SDO	ss	$\overline{SS}$
	dt	Data in	t0	T0CKI
	io	I/O port	t1	T13CKI
	mc	$\overline{MCLR}$	wr	$\overline{WR}$

Uppercase letters and their meanings:

S				
	F	Fall	P	Period
	H	High	R	Rise
	I	Invalid (High-impedance)	V	Valid
	L	Low	Z	High-impedance
I^{2}C only				
	AA	output access	High	High
	BUF	Bus free	Low	Low

T$_{CC:ST}$ (I^{2}C specifications only)

CC				
	HD	Hold	SU	Setup
ST				
	DAT	DATA input hold	STO	Stop condition
	STA	Start condition		

FIGURE 26-12: **PARALLEL SLAVE PORT TIMING (PIC18F4420/4520)**

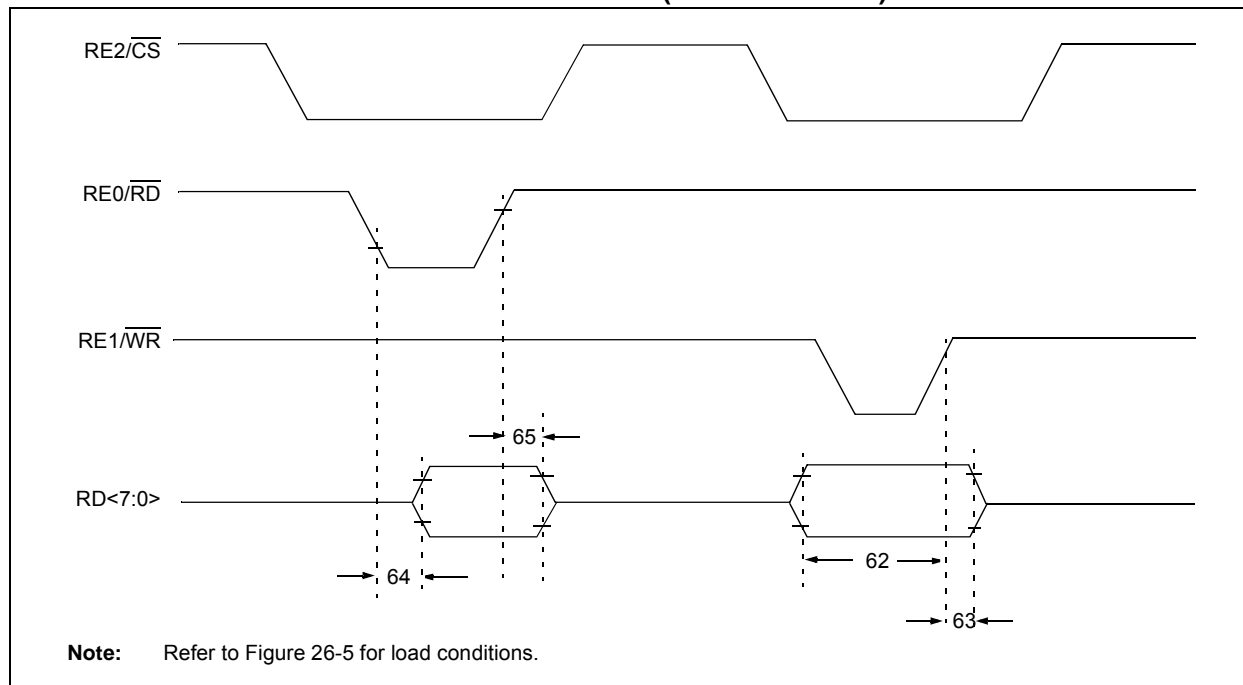**Note:** Refer to Figure 26-5 for load conditions.

TABLE 26-13: PARALLEL SLAVE PORT REQUIREMENTS (PIC18F4420, PIC18F4520)

Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
62	TdtV2wrH	Data In Valid before $\overline{WR}$ ↑ or $\overline{CS}$ ↑ (setup time)		20	—	ns	
63	TwrH2dtI	$\overline{WR}$ ↑ or $\overline{CS}$ ↑ to Data–In Invalid (hold time)	PIC18**F**XXXX	20	—	ns	
			PIC18**LF**XXXX	35	—	ns	VDD = 2.0V
64	TrdL2dtV	$\overline{RD}$ ↓ and $\overline{CS}$ ↓ to Data–Out Valid		—	80	ns	
65	TrdH2dtI	$\overline{RD}$ ↑ or $\overline{CS}$ ↓ to Data–Out Invalid		10	30	ns	
66	TibfINH	Inhibit of the IBF Flag bit being Cleared from $\overline{WR}$ ↑ or $\overline{CS}$ ↑		—	3 TCY		

FIGURE 26-13: **EXAMPLE SPI MASTER MODE TIMING (CKE = 0)**

Note: Refer to Figure 26-5 for load conditions.
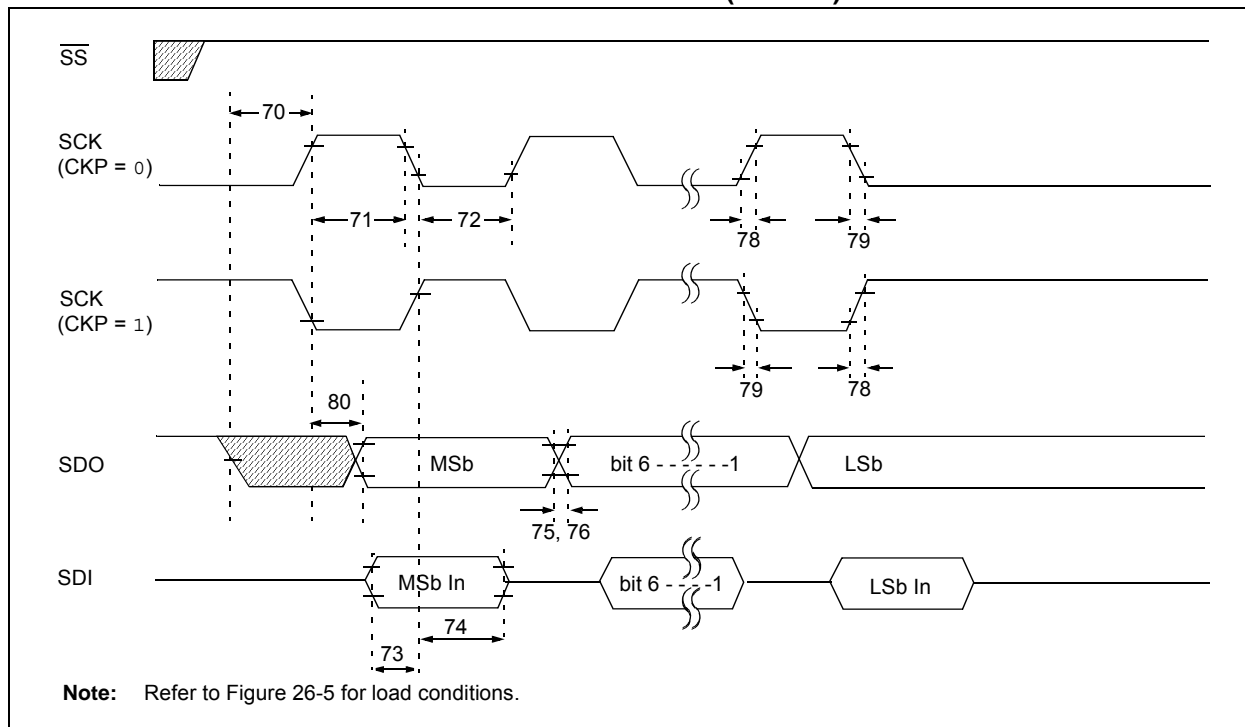
TABLE 26-14: **EXAMPLE SPI MODE REQUIREMENTS (MASTER MODE, CKE = 0)**

Param No.	Symbol	Characteristic		Min	Max	Units	Conditions
70	TssL2scH, TssL2scL	$\overline{SS} \downarrow$ to SCK $\downarrow$ or SCK $\uparrow$ Input		T$_{CY}$	—	ns	
73	TdiV2scH, TdiV2scL	Setup Time of SDI Data Input to SCK Edge		20	—	ns	
73A	Tb2b	Last Clock Edge of Byte 1 to the 1st Clock Edge of Byte 2		1.5 T$_{CY}$ + 40	—	ns	**(Note 2)**
74	TscH2diL, TscL2diL	Hold Time of SDI Data Input to SCK Edge		40	—	ns	
75	TdoR	SDO Data Output Rise Time	PIC18**F**XXXX	—	25	ns	
			PIC18**LF**XXXX	—	45	ns	V$_{DD}$ = 2.0V
76	TdoF	SDO Data Output Fall Time		—	25	ns	
78	TscR	SCK Output Rise Time (Master mode)	PIC18**F**XXXX	—	25	ns	
			PIC18**LF**XXXX	—	45	ns	V$_{DD}$ = 2.0V
79	TscF	SCK Output Fall Time (Master mode)		—	25	ns	
80	TscH2doV, TscL2doV	SDO Data Output Valid after SCK Edge	PIC18**F**XXXX	—	50	ns	
			PIC18**LF**XXXX	—	100	ns	V$_{DD}$ = 2.0V

Note 1: Requires the use of Parameter #73A.

2: Only if Parameter #71A and #72A are used.

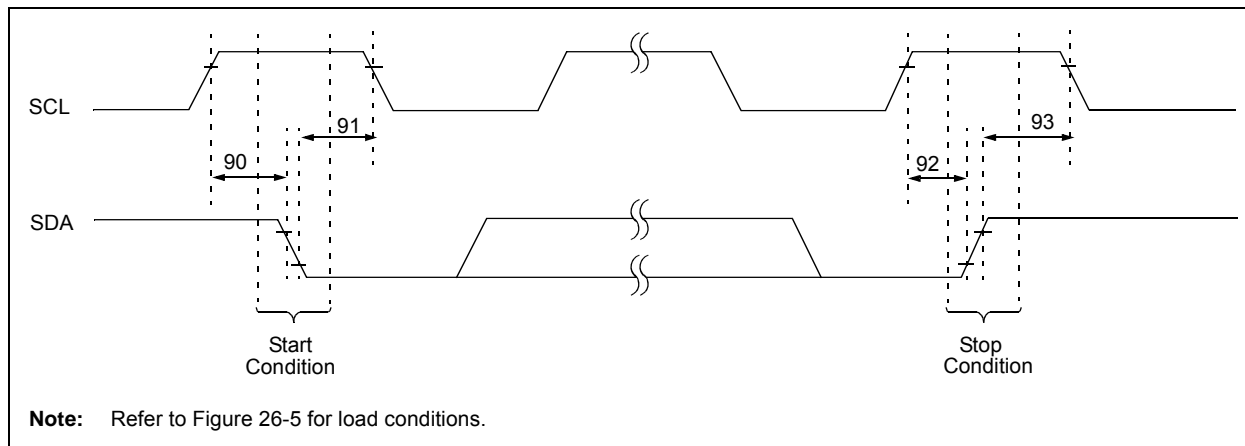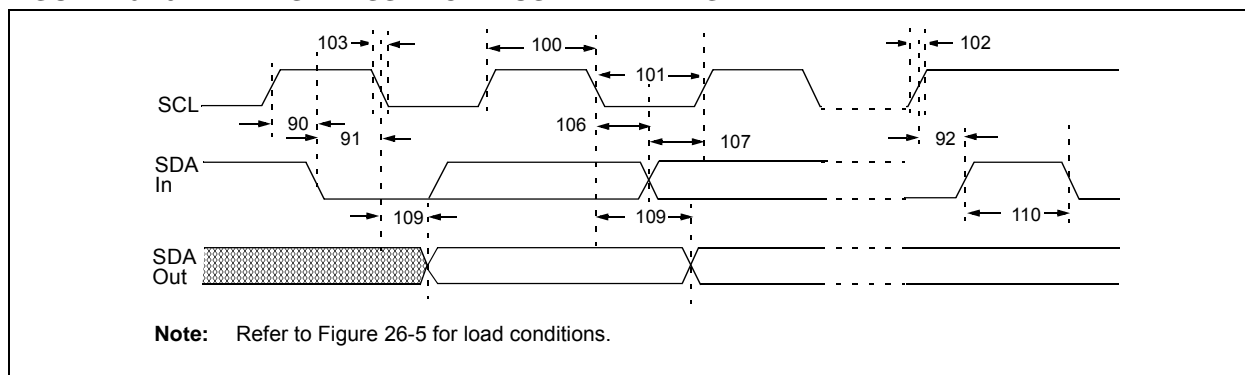**FIGURE 26-19:** **MASTER SSP I²C™ BUS START/STOP BITS TIMING WAVEFORMS**

Note: Refer to Figure 26-5 for load conditions.

TABLE 26-20: **MASTER SSP I²C™ BUS START/STOP BITS REQUIREMENTS**

Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
90	TSU:STA	Start Condition Setup Time	100 kHz mode	2(TOSC)(BRG + 1)	—	ns	Only relevant for Repeated Start condition
			400 kHz mode	2(TOSC)(BRG + 1)	—		
			1 MHz mode[1]	2(TOSC)(BRG + 1)	—		
91	THD:STA	Start Condition Hold Time	100 kHz mode	2(TOSC)(BRG + 1)	—	ns	After this period, the first clock pulse is generated
			400 kHz mode	2(TOSC)(BRG + 1)	—		
			1 MHz mode[1]	2(TOSC)(BRG + 1)	—		
92	TSU:STO	Stop Condition Setup Time	100 kHz mode	2(TOSC)(BRG + 1)	—	ns	
			400 kHz mode	2(TOSC)(BRG + 1)	—		
			1 MHz mode[1]	2(TOSC)(BRG + 1)	—		
93	THD:STO	Stop Condition Hold Time	100 kHz mode	2(TOSC)(BRG + 1)	—	ns	
			400 kHz mode	2(TOSC)(BRG + 1)	—		
			1 MHz mode[1]	2(TOSC)(BRG + 1)	—		

Note 1: Maximum pin capacitance = 10 pF for all I²C pins.

FIGURE 26-20: **MASTER SSP I²C™ BUS DATA TIMING**

Note: Refer to Figure 26-5 for load conditions.

FIGURE 26-23: A/D CONVERSION TIMING

Note 1: If the A/D clock source is selected as RC, a time of T_{CY} is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

2: This is a minimal RC delay (typically 100 ns), which also disconnects the holding capacitor from the analog input.
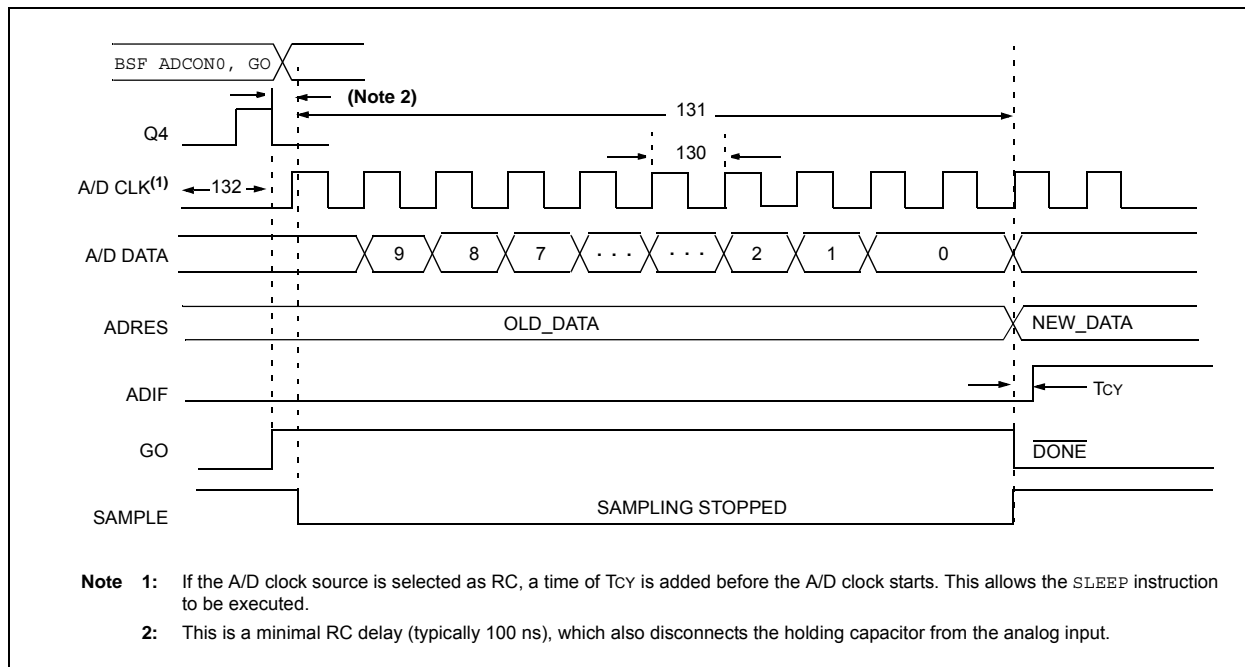
TABLE 26-25: A/D CONVERSION REQUIREMENTS

Param No.	Symbol	Characteristic		Min	Max	Units	Conditions
130	T_{AD}	A/D Clock Period	PIC18**F**XXXX	0.7	25.0[1]	μs	T_{OSC} based, $V_{REF} \geq 3.0V$
			PIC18**LF**XXXX	1.4	25.0[1]	μs	$V_{DD} = 2.0V$; T_{OSC} based, V_{REF} full range
			PIC18**F**XXXX	—	1	μs	A/D RC mode
			PIC18**LF**XXXX	—	3	μs	$V_{DD} = 2.0V$; A/D RC mode
131	T_{CNV}	Conversion Time (not including acquisition time) **(Note 2)**		11	12	T_{AD}	
132	T_{ACQ}	Acquisition Time **(Note 3)**		1.4	—	μs	-40°C to +85°C
135	T_{SWC}	Switching Time from Convert → Sample		—	**(Note 4)**		
TBD	T_{DIS}	Discharge Time		0.2	—	μs	

Note 1: The time of the A/D clock period is dependent on the device frequency and the T_{AD} clock divider.

2: ADRES register may be read on the following T_{CY} cycle.

3: The time for the holding capacitor to acquire the "New" input voltage when the voltage changes full scale after the conversion (V_{DD} to V_{SS} or V_{SS} to V_{DD}). The source impedance (R_S) on the input channels is 50Ω.

4: On the following cycle of the device clock.

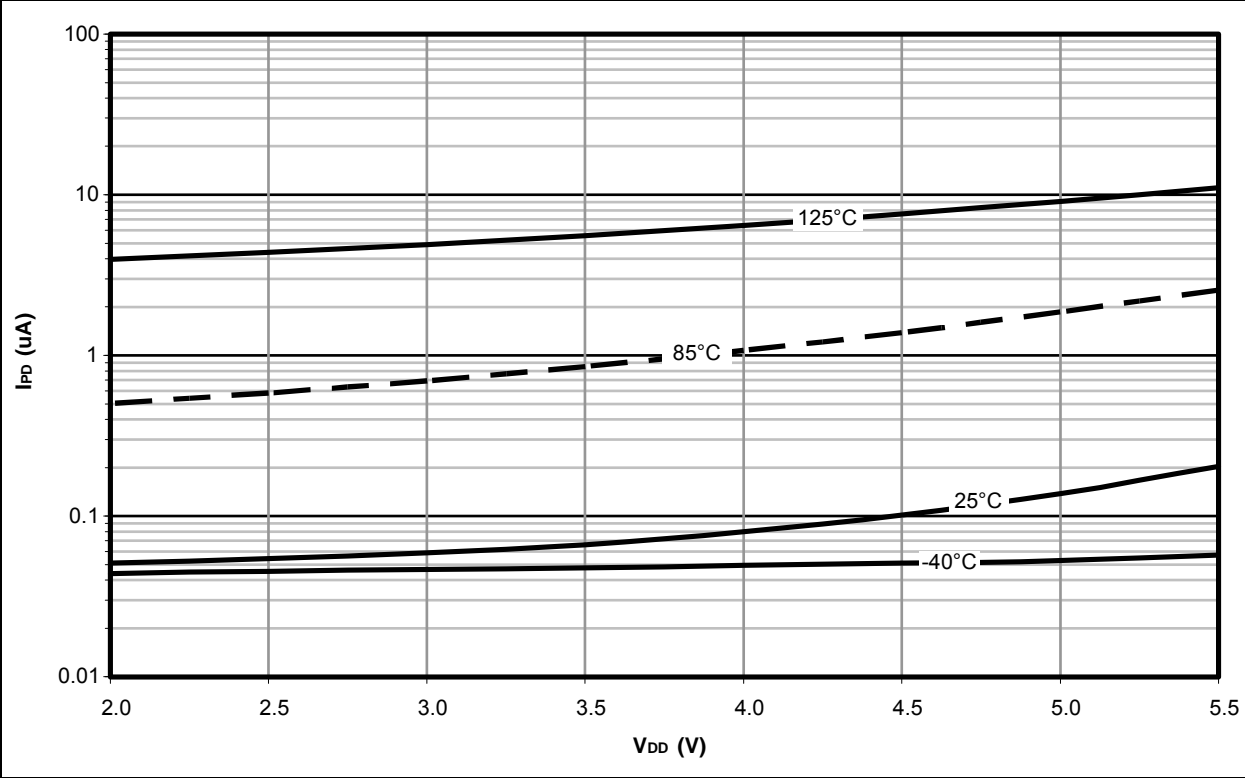**FIGURE 27-2:** **TYPICAL I$_{PD}$ vs. V$_{DD}$ ACROSS TEMPERATURE (SLEEP MODE)**

FIGURE 27-3: **MAXIMUM I$_{PD}$ vs. V$_{DD}$ ACROSS TEMPERATURE (SLEEP MODE)**