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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	32KB (16K × 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f4520t-i-pt

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

3.4.3 RC_IDLE MODE

In RC_IDLE mode, the CPU is disabled but the peripherals continue to be clocked from the internal oscillator block using the INTOSC multiplexer. This mode allows for controllable power conservation during Idle periods.

From RC_RUN, this mode is entered by setting the IDLEN bit and executing a SLEEP instruction. If the device is in another Run mode, first set IDLEN, then set the SCS1 bit and execute SLEEP. Although its value is ignored, it is recommended that SCS0 also be cleared; this is to maintain software compatibility with future devices. The INTOSC multiplexer may be used to select a higher clock frequency by modifying the IRCF bits before executing the SLEEP instruction. When the clock source is switched to the INTOSC multiplexer, the primary oscillator is shut down and the OSTS bit is cleared.

If the IRCF bits are set to any non-zero value, or the INTSRC bit is set, the INTOSC output is enabled. The IOFS bit becomes set, after the INTOSC output becomes stable, after an interval of TIOBST (parameter 39, Table 26-10). Clocks to the peripherals continue while the INTOSC source stabilizes. If the IRCF bits were previously at a non-zero value, or INTSRC was set before the SLEEP instruction was executed and the INTOSC source was already stable, the IOFS bit will remain set. If the IRCF bits and INTSRC are all clear, the INTOSC output will not be enabled, the IOFS bit will remain clear and there will be no indication of the current clock source.

When a wake event occurs, the peripherals continue to be clocked from the INTOSC multiplexer. After a delay of TCSD following the wake event, the CPU begins executing code being clocked by the INTOSC multiplexer. The IDLEN and SCS bits are not affected by the wake-up. The INTRC source will continue to run if either the WDT or the Fail-Safe Clock Monitor is enabled.

3.5 Exiting Idle and Sleep Modes

An exit from Sleep mode or any of the Idle modes is triggered by an interrupt, a Reset or a WDT time-out. This section discusses the triggers that cause exits from power-managed modes. The clocking subsystem actions are discussed in each of the power-managed modes (see Section 3.2 "Run Modes", Section 3.3 "Sleep Mode" and Section 3.4 "Idle Modes").

3.5.1 EXIT BY INTERRUPT

Any of the available interrupt sources can cause the device to exit from an Idle mode or the Sleep mode to a Run mode. To enable this functionality, an interrupt source must be enabled by setting its enable bit in one of the INTCON or PIE registers. The exit sequence is initiated when the corresponding interrupt flag bit is set.

On all exits from Idle or Sleep modes by interrupt, code execution branches to the interrupt vector if the GIE/ GIEH bit (INTCON<7>) is set. Otherwise, code execution continues or resumes without branching (see **Section 9.0 "Interrupts"**).

A fixed delay of interval TCSD following the wake event is required when leaving Sleep and Idle modes. This delay is required for the CPU to prepare for execution. Instruction execution resumes on the first clock cycle following this delay.

3.5.2 EXIT BY WDT TIME-OUT

A WDT time-out will cause different actions depending on which power-managed mode the device is in when the time-out occurs.

If the device is not executing code (all Idle modes and Sleep mode), the time-out will result in an exit from the power-managed mode (see Section 3.2 "Run Modes" and Section 3.3 "Sleep Mode"). If the device is executing code (all Run modes), the time-out will result in a WDT Reset (see Section 23.2 "Watchdog Timer (WDT)").

The WDT timer and postscaler are cleared by executing a SLEEP or CLRWDT instruction, the loss of a currently selected clock source (if the Fail-Safe Clock Monitor is enabled) and modifying the IRCF bits in the OSCCON register if the internal oscillator block is the device clock source.

3.5.3 EXIT BY RESET

Normally, the device is held in Reset by the Oscillator Start-up Timer (OST) until the primary clock becomes ready. At that time, the OSTS bit is set and the device begins executing code. If the internal oscillator block is the new clock source, the IOFS bit is set instead.

The exit delay time from Reset to the start of code execution depends on both the clock sources before and after the wake-up and the type of oscillator if the new clock source is the primary clock. Exit delays are summarized in Table 3-2.

Code execution can begin before the primary clock becomes ready. If either the Two-Speed Start-up (see Section 23.3 "Two-Speed Start-up") or Fail-Safe Clock Monitor (see Section 23.4 "Fail-Safe Clock Monitor") is enabled, the device may begin execution as soon as the Reset source has cleared. Execution is clocked by the INTOSC multiplexer driven by the internal oscillator block. Execution is clocked by the internal oscillator block. Execution is clocked by the internal oscillator block until either the primary clock becomes ready or a power-managed mode is entered before the primary clock becomes ready; the primary clock is then shut down.

4.2 Master Clear (MCLR)

The MCLR pin provides a method for triggering an external Reset of the device. A Reset is generated by holding the pin low. These devices have a noise filter in the MCLR Reset path which detects and ignores small pulses.

The $\overline{\text{MCLR}}$ pin is not driven low by any internal Resets, including the WDT.

In PIC18F2420/2520/4420/4520 devices, the $\overline{\text{MCLR}}$ input can be disabled with the MCLRE Configuration bit. When $\overline{\text{MCLR}}$ is disabled, the pin becomes a digital input. See **Section 10.5** "**PORTE, TRISE and LATE Registers**" for more information.

4.3 Power-on Reset (POR)

A Power-on Reset pulse is generated on-chip whenever VDD rises above a certain threshold. This allows the device to start in the initialized state when VDD is adequate for operation.

To take advantage of the POR circuitry, tie the $\overline{\text{MCLR}}$ pin through a resistor (1 k Ω to 10 k Ω) to VDD. This will eliminate external RC components usually needed to create a Power-on Reset delay. A minimum rise rate for VDD is specified (parameter D004). For a slow rise time, see Figure 4-2.

When the device starts normal operation (i.e., exits the Reset condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

POR events are captured by the \overrightarrow{POR} bit (RCON<1>). The state of the bit is set to '0' whenever a POR occurs; it does not change for any other Reset event. \overrightarrow{POR} is not reset to '1' by any hardware event. To capture multiple events, the user manually resets the bit to '1' in software following any POR.

FIGURE 4-2:

EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



- Note 1: External Power-on Reset circuit is required only if the VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.
 - 2: $R < 40 \ k\Omega$ is recommended to make sure that the voltage drop across R does not violate the device's electrical specification.

4.4 Brown-out Reset (BOR)

PIC18F2420/2520/4420/4520 devices implement a BOR circuit that provides the user with a number of configuration and power-saving options. The BOR is controlled by the BORV<1:0> and BOREN<1:0> Configuration bits. There are a total of four BOR configurations which are summarized in Table 4-1.

The BOR threshold is set by the BORV<1:0> bits. If BOR is enabled (any values of BOREN<1:0>, except '00'), any drop of VDD below VBOR (parameter D005) for greater than TBOR (parameter 35) will reset the device. A Reset may or may not occur if VDD falls below VBOR for less than TBOR. The chip will remain in Brown-out Reset until VDD rises above VBOR.

If the Power-up Timer is enabled, it will be invoked after VDD rises above VBOR; it then will keep the chip in Reset for an additional time delay, TPWRT (parameter 33). If VDD drops below VBOR while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be initialized. Once VDD rises above VBOR, the Power-up Timer will execute the additional time delay.

BOR and the Power-up Timer (PWRT) are independently configured. Enabling the Brown-out Reset does not automatically enable the PWRT.

4.4.1 SOFTWARE ENABLED BOR

When BOREN<1:0> = 01, the BOR can be enabled or disabled by the user in software. This is done with the control bit, SBOREN (RCON<6>). Setting SBOREN enables the BOR to function as previously described. Clearing SBOREN disables the BOR entirely. The SBOREN bit operates only in this mode; otherwise it is read as '0'. Placing the BOR under software control gives the user the additional flexibility of tailoring the application to its environment without having to reprogram the device to change BOR configuration. It also allows the user to tailor device power consumption in software by eliminating the incremental current that the BOR consumes. While the BOR current is typically very small, it may have some impact in low-power applications.

Note:	Even when BOR is under software control,
	the Brown-out Reset voltage level is still
	set by the BORV<1:0> Configuration bits;
	it cannot be changed in software.

4.4.2 DETECTING BOR

When BOR is enabled, the BOR bit always resets to '0' on any BOR or POR event. This makes it difficult to determine if a BOR event has occurred just by reading the state of BOR alone. A more reliable method is to simultaneously check the state of both POR and BOR. This assumes that the POR bit is reset to '1' in software immediately after any POR event. If BOR is '0' while POR is '1', it can be reliably assumed that a BOR event has occurred.

4.4.3 DISABLING BOR IN SLEEP MODE

When BOREN<1:0> = 10, the BOR remains under hardware control and operates as previously described. Whenever the device enters Sleep mode, however, the BOR is automatically disabled. When the device returns to any other operating mode, BOR is automatically re-enabled.

This mode allows for applications to recover from brown-out situations, while actively executing code, when the device requires BOR protection the most. At the same time, it saves additional power in Sleep mode by eliminating the small incremental BOR current.

BOR Con	figuration	Status of	BOD Operation				
BOREN1	BOREN0	(RCON<6>)	BOR Operation				
0	0	Unavailable	BOR disabled; must be enabled by reprogramming the Configuration bits.				
0	1	Available	BOR enabled in software; operation controlled by SBOREN.				
1	0	Unavailable	BOR enabled in hardware in Run and Idle modes, disabled during Sleep mode.				
1	1	Unavailable	BOR enabled in hardware; must be disabled by reprogramming the Configuration bits.				

TABLE 4-1: BOR CONFIGURATIONS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	49
EEADR	EEPROM Address Register								
EEDATA	EEPROM Data Register								
EECON2	EEPROM C	ontrol Registe	er 2 (not a p	hysical reg	ister)				51
EECON1	EEPGD	CFGS	—	FREE	WRERR	WREN	WR	RD	51
IPR2	OSCFIP	CMIP	—	EEIP	BCLIP	HLVDIP	TMR3IP	CCP2IP	52
PIR2	OSCFIF	CMIF	—	EEIF	BCLIF	HLVDIF	TMR3IF	CCP2IF	52
PIE2	OSCFIE	CMIE	_	EEIE	BCLIE	HLVDIE	TMR3IE	CCP2IE	52

TABLE 7-1: REGISTERS ASSOCIATED WITH DATA EEPROM MEMORY

Legend: — = unimplemented, read as '0'. Shaded cells are not used during Flash/EEPROM access.

	TORIDI				
Pin	Function	TRIS Setting	I/O	I/O Type	Description
RD0/PSP0	RD0	0	0	DIG	LATD<0> data output.
		1	I	ST	PORTD<0> data input.
	PSP0	x	0	DIG	PSP read data output (LATD<0>); takes priority over port data.
		x	I	TTL	PSP write data input.
RD1/PSP1	RD1	0	0	DIG	LATD<1> data output.
		1	I	ST	PORTD<1> data input.
	PSP1	x	0	DIG	PSP read data output (LATD<1>); takes priority over port data.
		x	I	TTL	PSP write data input.
RD2/PSP2	RD2	0	0	DIG	LATD<2> data output.
		1	I	ST	PORTD<2> data input.
	PSP2	x	0	DIG	PSP read data output (LATD<2>); takes priority over port data.
		x	I	TTL	PSP write data input.
RD3/PSP3	RD3	0	0	DIG	LATD<3> data output.
		1	I	ST	PORTD<3> data input.
	PSP3	x	0	DIG	PSP read data output (LATD<3>); takes priority over port data.
		x	I	TTL	PSP write data input.
RD4/PSP4	RD4	0	0	DIG	LATD<4> data output.
		1	I	ST	PORTD<4> data input.
	PSP4	x	0	DIG	PSP read data output (LATD<4>); takes priority over port data.
		x	I	TTL	PSP write data input.
RD5/PSP5/P1B	RD5	0	0	DIG	LATD<5> data output.
		1	I	ST	PORTD<5> data input.
	PSP5	x	0	DIG	PSP read data output (LATD<5>); takes priority over port data.
		x	I	TTL	PSP write data input.
	P1B	0	0	DIG	ECCP1 Enhanced PWM output, channel B; takes priority over port and PSP data. May be configured for tri-state during Enhanced PWM shutdown events.
RD6/PSP6/P1C	RD6	0	0	DIG	LATD<6> data output.
		1	I	ST	PORTD<6> data input.
	PSP6	x	0	DIG	PSP read data output (LATD<6>); takes priority over port data.
		х	Ι	TTL	PSP write data input.
	P1C	0	0	DIG	ECCP1 Enhanced PWM output, channel C; takes priority over port and PSP data. May be configured for tri-state during Enhanced PWM shutdown events.
RD7/PSP7/P1D	RD7	0	0	DIG	LATD<7> data output.
		1	I	ST	PORTD<7> data input.
	PSP7	x	0	DIG	PSP read data output (LATD<7>); takes priority over port data.
		x	Ι	TTL	PSP write data input.
	P1D	0	0	DIG	ECCP1 Enhanced PWM output, channel D; takes priority over port and PSP data. May be configured for tri-state during Enhanced PWM shutdown events.

TABLE 10-7: PORTD	I/O	SUMMARY
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Legend: DIG = Digital level output; TTL = TTL input buffer; ST = Schmitt Trigger input buffer; x = Don't care (TRIS bit does not affect port direction or is overridden for this option).

15.2 Capture Mode

In Capture mode, the CCPRxH:CCPRxL register pair captures the 16-bit value of the TMR1 or TMR3 register when an event occurs on the corresponding CCPx pin. An event is defined as one of the following:

- · every falling edge
- · every rising edge
- every 4th rising edge
- · every 16th rising edge

The event is selected by the mode select bits, CCPxM<3:0> (CCPxCON<3:0>). When a capture is made, the interrupt request flag bit, CCPxIF, is set; it must be cleared in software. If another capture occurs before the value in register CCPRx is read, the old captured value is overwritten by the new captured value.

15.2.1 CCP PIN CONFIGURATION

In Capture mode, the appropriate CCPx pin should be configured as an input by setting the corresponding TRIS direction bit.

Note:	If RB3/CCP2 or RC1/CCP2 is configured							
	as an output, a write to the port can cause							
	a capture condition.							

15.2.2 TIMER1/TIMER3 MODE SELECTION

The timers that are to be used with the capture feature (Timer1 and/or Timer3) must be running in Timer mode or Synchronized Counter mode. In Asynchronous Counter mode, the capture operation will not work. The timer to be used with each CCP module is selected in the T3CON register (see Section 15.1.1 "CCP Modules and Timer Resources").

15.2.3 SOFTWARE INTERRUPT

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep the CCPxIE interrupt enable bit clear to avoid false interrupts. The interrupt flag bit, CCPxIF, should also be cleared following any such change in operating mode.

15.2.4 CCP PRESCALER

There are four prescaler settings in Capture mode; they are specified as part of the operating mode selected by the mode select bits (CCPxM<3:0>). Whenever the CCP module is turned off, or Capture mode is disabled, the prescaler counter is cleared. This means that any Reset will clear the prescaler counter.

Switching from one capture prescaler to another may generate an interrupt. Also, the prescaler counter will not be cleared; therefore, the first capture may be from a non-zero prescaler. Example 15-1 shows the recommended method for switching between capture prescalers. This example also clears the prescaler counter and will not generate the "false" interrupt.

EXAMPLE 15-1: CHANGING BETWEEN CAPTURE PRESCALERS (CCP2 SHOWN)

CLRF MOVLW	CCP2CON NEW_CAPT_PS	; ;	Turn CCP module off Load WREG with the
		;	new prescaler mode
		;	value and CCP ON
MOVWF	CCP2CON	;	Load CCP2CON with
		;	this value

FIGURE 15-1: CAPTURE MODE OPERATION BLOCK DIAGRAM



17.4.2 OPERATION

The MSSP module functions are enabled by setting the MSSP Enable bit, SSPEN (SSPCON1<5>).

The SSPCON1 register allows control of the I^2C operation. Four mode selection bits (SSPCON1<3:0>) allow one of the following I^2C modes to be selected:

- I²C Master mode, clock = (Fosc/4) x (SSPADD + 1)
- I²C Slave mode (7-bit addressing)
- I²C Slave mode (10-bit addressing)
- I²C Slave mode (7-bit addressing) with Start and Stop bit interrupts enabled
- I²C Slave mode (10-bit addressing) with Start and Stop bit interrupts enabled
- I²C Firmware Controlled Master mode, slave is Idle

Selection of any I²C mode, with the SSPEN bit set, forces the SCL and SDA pins to be open-drain, provided these pins are programmed to inputs by setting the appropriate TRISC bits. To ensure proper operation of the module, pull-up resistors must be provided externally to the SCL and SDA pins.

17.4.3 SLAVE MODE

In Slave mode, the SCL and SDA pins must be configured as inputs (TRISC<4:3> set). The MSSP module will override the input state with the output data when required (slave-transmitter).

The I²C Slave mode hardware will always generate an interrupt on an address match. Through the mode select bits, the user can also choose to interrupt on Start and Stop bits

When an address is matched, or the data transfer after an address match is received, the hardware automatically will generate the Acknowledge (\overline{ACK}) pulse and load the SSPBUF register with the received value currently in the SSPSR register.

Any combination of the following conditions will cause the MSSP module not to give this ACK pulse:

- The Buffer Full bit, BF (SSPSTAT<0>), was set before the transfer was received.
- The overflow bit, SSPOV (SSPCON2<6>), was set before the transfer was received.

In this case, the SSPSR register value is not loaded into the SSPBUF, but bit, SSPIF (PIR1<3>), is set. The BF bit is cleared by reading the SSPBUF register, while bit SSPOV is cleared through software.

The SCL clock input must have a minimum high and low for proper operation. The high and low times of the I^2C specification, as well as the requirement of the MSSP module, are shown in timing parameter 100 and parameter 101.

17.4.3.1 Addressing

Once the MSSP module has been enabled, it waits for a Start condition to occur. Following the Start condition, the 8 bits are shifted into the SSPSR register. All incoming bits are sampled with the rising edge of the clock (SCL) line. The value of register SSPSR<7:1> is compared to the value of the SSPADD register. The address is compared on the falling edge of the eighth clock (SCL) pulse. If the addresses match and the BF and SSPOV bits are clear, the following events occur:

- 1. The SSPSR register value is loaded into the SSPBUF register.
- 2. The Buffer Full bit, BF, is set.
- 3. An ACK pulse is generated.
- 4. MSSP Interrupt Flag bit, SSPIF (PIR1<3>), is set (interrupt is generated, if enabled) on the falling edge of the ninth SCL pulse.

In 10-Bit Addressing mode, two address bytes need to be received by the slave. The five Most Significant bits (MSbs) of the first address byte specify if this is a 10-bit address. Bit, R/W (SSPSTAT<2>), must specify a write so the slave device will receive the second address byte. For a 10-bit address, the first byte would equal '11110 A9 A8 0', where 'A9' and 'A8' are the two MSbs of the address. The sequence of events for 10-Bit Addressing mode is as follows, with steps 7 through 9 for the slave-transmitter:

- 1. Receive first (high) byte of address (bits, SSPIF, BF and UA (SSPSTAT<1>), are set).
- Update the SSPADD register with second (low) byte of address (clears UA bit and releases the SCL line).
- 3. Read the SSPBUF register (clears BF bit) and clear flag bit, SSPIF.
- 4. Receive second (low) byte of address (bits, SSPIF, BF and UA, are set).
- 5. Update the SSPADD register with the first (high) byte of address. If match releases SCL line, this will clear bit, UA.
- 6. Read the SSPBUF register (clears BF bit) and clear flag bit, SSPIF.
- 7. Receive Repeated Start condition.
- 8. Receive first (high) byte of address (bits, SSPIF and BF, are set).
- 9. Read the SSPBUF register (clears BF bit) and clear flag bit, SSPIF.

PIC18F2420/2520/4420/4520



FIGURE 18-5: ASYNCHRONOUS TRANSMISSION (BACK TO BACK)



TABLE 18-5: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	49
PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	52
PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	52
IPR1	PSPIP ⁽¹⁾	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	52
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	51
TXREG	EUSART T	ransmit Reg	jister						51
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	51
BAUDCON	ABDOVF	RCIDL	RXDTP	TXCKP	BRG16	—	WUE	ABDEN	51
SPBRGH	EUSART Baud Rate Generator Register High Byte								
SPBRG	EUSART E	Baud Rate G	enerator Re	gister Low	Byte				51

Legend: — = unimplemented locations read as '0'. Shaded cells are not used for asynchronous transmission.

Note 1: Reserved in 28-pin devices; always maintain these bits clear.

18.2.4.1 Special Considerations Using Auto-Wake-up

Since auto-wake-up functions by sensing rising edge transitions on RX/DT, information with any state changes before the Stop bit may signal a false End-of-Character (EOC) and cause data or framing errors. To work properly, therefore, the initial character in the transmission must be all '0's. This can be 00h (8 bytes) for standard RS-232 devices or 000h (12 bits) for LIN bus.

Oscillator start-up time must also be considered, especially in applications using oscillators with longer start-up intervals (i.e., XT or HS mode). The Sync Break (or Wake-up Signal) character must be of sufficient length and be followed by a sufficient interval to allow enough time for the selected oscillator to start and provide proper initialization of the EUSART.

18.2.4.2 Special Considerations Using the WUE Bit

The timing of WUE and RCIF events may cause some confusion when it comes to determining the validity of received data. As noted, setting the WUE bit places the EUSART in an Idle mode. The wake-up event causes a receive interrupt by setting the RCIF bit. The WUE bit is cleared after this when a rising edge is seen on RX/DT. The interrupt condition is then cleared by reading the RCREG register. Ordinarily, the data in RCREG will be dummy data and should be discarded.

The fact that the WUE bit has been cleared (or is still set) and the RCIF flag is set should not be used as an indicator of the integrity of the data in RCREG. Users should consider implementing a parallel method in firmware to verify received data integrity.

To assure that no actual data is lost, check the RCIDL bit to verify that a receive operation is not in process. If a receive operation is not occurring, the WUE bit may then be set just prior to entering the Sleep mode.









18.4 EUSART Synchronous Slave Mode

Synchronous Slave mode is entered by clearing bit, CSRC (TXSTA<7>). This mode differs from the Synchronous Master mode in that the shift clock is supplied externally at the CK pin (instead of being supplied internally in Master mode). This allows the device to transfer or receive data while in any low-power mode.

18.4.1 EUSART SYNCHRONOUS SLAVE TRANSMISSION

The operation of the Synchronous Master and Slave modes is identical, except in the case of the Sleep mode.

If two words are written to the TXREG and then the SLEEP instruction is executed, the following will occur:

- a) The first word will immediately transfer to the TSR register and transmit.
- b) The second word will remain in the TXREG register.
- c) Flag bit, TXIF, will not be set.
- d) When the first word has been shifted out of TSR, the TXREG register will transfer the second word to the TSR and flag bit, TXIF, will now be set.
- e) If enable bit, TXIE, is set, the interrupt will wake the chip from Sleep. If the global interrupt is enabled, the program will branch to the interrupt vector.

To set up a Synchronous Slave Transmission:

- 1. Enable the synchronous slave serial port by setting bits, SYNC and SPEN, and clearing bit, CSRC.
- 2. Clear bits, CREN and SREN.
- 3. If interrupts are desired, set enable bit, TXIE.
- 4. If 9-bit transmission is desired, set bit, TX9.
- 5. Enable the transmission by setting enable bit, TXEN.
- 6. If 9-bit transmission is selected, the ninth bit should be loaded in bit, TX9D.
- 7. Start transmission by loading data to the TXREG register.
- If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	49
PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	52
PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	52
IPR1	PSPIP ⁽¹⁾	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	52
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	51
TXREG	EUSART T	ransmit Reg	ister						51
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	51
BAUDCON	ABDOVF	RCIDL	RXDTP	TXCKP	BRG16	—	WUE	ABDEN	51
SPBRGH	EUSART Baud Rate Generator Register High Byte								
SPBRG	EUSART E	aud Rate Ge	enerator Re	gister Low I	Byte				51

TABLE 18-9: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE TRANSMISSION

Legend: — = unimplemented, read as '0'. Shaded cells are not used for synchronous slave transmission.

Note 1: Reserved in 28-pin devices; always maintain these bits clear.

PIC18F2420/2520/4420/4520

FIGURE 20-3: COMPARATOR OUTPUT BLOCK DIAGRAM



20.6 Comparator Interrupts

The comparator interrupt flag is set whenever there is a change in the output value of either comparator. Software will need to maintain information about the status of the output bits, as read from CMCON<7:6>, to determine the actual change that occurred. The CMIF bit (PIR2<6>) is the Comparator Interrupt Flag. The CMIF bit must be reset by clearing it. Since it is also possible to write a '1' to this register, a simulated interrupt may be initiated.

Both the CMIE bit (PIE2<6>) and the PEIE bit (INTCON<6>) must be set to enable the interrupt. In addition, the GIE bit (INTCON<7>) must also be set. If any of these bits are clear, the interrupt is not enabled, though the CMIF bit will still be set if an interrupt condition occurs.

Note:	If a change in the CMCON register										
	(C1OUT or C2OUT) should occur when a										
	read operation is being executed (start of										
	the Q2 cycle), then the CMIF (PIR2<6>)										
	interrupt flag may not get set.										

The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

- a) Any read or write of CMCON will end the mismatch condition.
- b) Clear flag bit, CMIF.

A mismatch condition will continue to set flag bit, CMIF. Reading CMCON will end the mismatch condition and allow flag bit, CMIF, to be cleared.

20.7 Comparator Operation During Sleep

When a comparator is active and the device is placed in Sleep mode, the comparator remains active and the interrupt is functional if enabled. This interrupt will wake-up the device from Sleep mode when enabled. Each operational comparator will consume additional current, as shown in the comparator specifications. To minimize power consumption while in Sleep mode, turn off the comparators (CM<2:0> = 111) before entering Sleep. If the device wakes up from Sleep, the contents of the CMCON register are not affected.

20.8 Effects of a Reset

A device Reset forces the CMCON register to its Reset state, causing the comparator modules to be turned off (CM<2:0> = 111). However, the input pins (RA0 through RA3) are configured as analog inputs by default on device Reset. The I/O configuration for these pins is determined by the setting of the PCFG<3:0> bits (ADCON1<3:0>). Therefore, device current is minimized when analog inputs are present at Reset time.

20.9 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 20-4. Since the analog pins are connected to a digital output, they have reverse biased diodes to VDD and Vss. The analog input, therefore, must be between Vss and VDD. If the input voltage deviates from this

range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up condition may occur. A maximum source impedance of 10 k Ω is recommended for the analog sources. Any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current.





TABLE 20-1: REGISTERS ASSOCIATED WITH COMPARATOR MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page		
CMCON	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	51		
CVRCON	CVREN	CVROE	CVRR	CVRSS	CVR3	CVR2	CVR1	CVR0	51		
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	52		
PIR2	OSCFIF	CMIF	_	EEIF	BCLIF	HLVDIF	TMR3IF	CCP2IF	52		
PIE2	OSCFIE	CMIE	_	EEIE	BCLIE	HLVDIE	TMR3IE	CCP2IE	52		
IPR2	OSCFIP	CMIP	—	EEIP	BCLIP	HLVDIP	TMR3IP	CCP2IP	52		
PORTA	RA7 ⁽¹⁾	RA6 ⁽¹⁾	RA5	RA4	RA3	RA2	RA1	RA0	52		
LATA	LATA7 ⁽¹⁾	LATA6 ⁽¹⁾	PORTA Da	PORTA Data Latch Register (Read and Write to Data Latch)							
TRISA	TRISA7 ⁽¹⁾	TRISA6 ⁽¹⁾	PORTA Da	ta Direction	Register				52		

Legend: — = unimplemented, read as '0'. Shaded cells are unused by the comparator module.

Note 1: PORTA<7:6> and their direction and latch bits are individually configured as port pins based on various primary oscillator modes. When disabled, these bits are read as '0'.





TABLE 21-1: REGISTERS ASSOCIATED WITH COMPARATOR VOLTAGE REFERENCE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
CVRCON	CVREN	CVROE	CVRR	CVRSS	CVR3	CVR2	CVR1	CVR0	51
CMCON	C2OUT	C10UT	C2INV	C1INV	CIS	CM2	CM1	CM0	51
TRISA	TRISA7 ⁽¹⁾	ISA7 ⁽¹⁾ TRISA6 ⁽¹⁾ PORTA Data Direction Register							52

Legend: Shaded cells are not used with the comparator voltage reference.

Note 1: PORTA pins are enabled based on oscillator configuration.

The module is enabled by setting the HLVDEN bit. Each time that the HLVD module is enabled, the circuitry requires some time to stabilize. The IRVST bit is a read-only bit and is used to indicate when the circuit is stable. The module can only generate an interrupt after the circuit is stable and IRVST is set.

The VDIRMAG bit determines the overall operation of the module. When VDIRMAG is cleared, the module monitors for drops in VDD below a predetermined set point. When the bit is set, the module monitors for rises in VDD above the set point.

22.1 Operation

When the HLVD module is enabled, a comparator uses an internally generated reference voltage as the set point. The set point is compared with the trip point, where each node in the resistor divider represents a trip point voltage. The "trip point" voltage is the voltage level at which the device detects a high or low-voltage event, depending on the configuration of the module. When the supply voltage is equal to the trip point, the voltage tapped off of the resistor array is equal to the internal reference voltage generated by the voltage reference module. The comparator then generates an interrupt signal by setting the HLVDIF bit.

The trip point voltage is software programmable to any one of 16 values. The trip point is selected by programming the HLVDL<3:0> bits (HLVDCON<3:0>).

The HLVD module has an additional feature that allows the user to supply the trip voltage to the module from an external source. This mode is enabled when bits, HLVDL<3:0>, are set to '1111'. In this state, the comparator input is multiplexed from the external input pin, HLVDIN. This gives users flexibility because it allows them to configure the High/Low-Voltage Detect interrupt to occur at any voltage in the valid operating range.





PIC18F2420/2520/4420/4520

REGISTER 23-6: CONFIG5L: CONFIGURATION REGISTER 5 LOW (BYTE ADDRESS 300008h)

U-0	U-0	U-0	U-0	R/C-1	R/C-1	R/C-1	R/C-1
	—	_		CP3 ⁽¹⁾	CP2 ⁽¹⁾	CP1	CP0
bit 7							bit 0
Legend:							

Logonan		
R = Readable bit	C = Clearable bit	U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed		u = Unchanged from programmed state

bit 7-4	Unimplemented: Read as '0'
bit 3	CP3: Code Protection bit ⁽¹⁾
	1 = Block 3 (006000-007FFFh) not code-protected 0 = Block 3 (006000-007FFFh) code-protected
bit 2	CP2: Code Protection bit ⁽¹⁾
	1 = Block 2 (004000-005FFFh) not code-protected
	0 = Block 2 (004000-005FFFh) code-protected
bit 1	CP1: Code Protection bit
	1 = Block 1 (002000-003FFFh) not code-protected
	0 = Block 1 (002000-003FFFh) code-protected
bit 0	CP0: Code Protection bit
	1 = Block 0 (000800-001FFFh) not code-protected
	0 = Block 0 (000800-001FFFh) code-protected

Note 1: Unimplemented in PIC18F2420/4420 devices; maintain this bit set.

REGISTER 23-7: CONFIG5H: CONFIGURATION REGISTER 5 HIGH (BYTE ADDRESS 300009h)

R/C-1	R/C-1	U-0	U-0	U-0	U-0	U-0	U-0
CPD	СРВ	—	—	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	C = Clearable bit	U = Unimplemented bit, read as '0'
-n = Value when device is unp	programmed	u = Unchanged from programmed state

bit 7	CPD: Data EEPROM Code Protection bit
	1 = Data EEPROM not code-protected
	0 = Data EEPROM code-protected
bit 6	CPB: Boot Block Code Protection bit
	1 = Boot block (000000-0007FFh) not code-protected
	0 = Boot block (000000-0007FFh) code-protected
bit 5-0	Unimplemented: Read as '0'

23.5.2 DATA EEPROM CODE PROTECTION

The entire data EEPROM is protected from external reads and writes by two bits: CPD and WRTD. CPD inhibits external reads and writes of data EEPROM. WRTD inhibits internal and external writes to data EEPROM. The CPU can always read data EEPROM under normal operation, regardless of the protection bit settings.

23.5.3 CONFIGURATION REGISTER PROTECTION

The Configuration registers can be write-protected. The WRTC bit controls protection of the Configuration registers. In normal execution mode, the WRTC bit is read-only. WRTC can only be written via ICSP or an external programmer.

23.6 ID Locations

Eight memory locations (20000h-200007h) are designated as ID locations, where the user can store checksum or other code identification numbers. These locations are both readable and writable during normal execution through the TBLRD and TBLWT instructions, or during program/verify. The ID locations can be read when the device is code-protected.

23.7 In-Circuit Serial Programming

PIC18F2420/2520/4420/4520 devices can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data and three other lines for power, ground and the programming voltage. This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

23.8 In-Circuit Debugger

When the DEBUG Configuration bit is programmed to a '0', the In-Circuit Debugger functionality is enabled. This function allows simple debugging functions when used with MPLAB[®] IDE. When the microcontroller has this feature enabled, some resources are not available for general use. Table 23-4 shows which resources are required by the background debugger.

TABLE 23-4:	DEBUGGER RESOURCES
	DEBOOCER RECOORCEO

I/O pins:	RB6, RB7
Stack:	2 levels
Program Memory:	512 bytes
Data Memory:	10 bytes

To use the In-Circuit Debugger function of the microcontroller, the design must implement In-Circuit Serial Programming connections to $\overline{\text{MCLR}}/\text{VPP}/\text{RE3}$, VDD, Vss, RB7 and RB6. This will interface to the In-Circuit Debugger module available from Microchip or one of the third party development tool companies.

23.9 Single-Supply ICSP Programming

The LVP Configuration bit enables Single-Supply ICSP Programming (formerly known as Low-Voltage ICSP Programming or LVP). When Single-Supply Programming is enabled, the microcontroller can be programmed without requiring high voltage being applied to the MCLR/VPP/RE3 pin, but the RB5/KBI1/PGM pin is then dedicated to controlling Program mode entry and is not available as a general purpose I/O pin.

While programming, using Single-Supply Programming mode, VDD is applied to the MCLR/VPP/RE3 pin as in normal execution mode. To enter Programming mode, VDD is applied to the PGM pin.

- Note 1: High-voltage programming is always available, regardless of the state of the LVP bit or the PGM pin, by applying VIHH to the MCLR pin.
 - 2: By default, Single-Supply ICSP is enabled in unprogrammed devices (as supplied from Microchip) and erased devices.
 - **3:** When Single-Supply Programming is enabled, the RB5 pin can no longer be used as a general purpose I/O pin.
 - 4: When LVP is enabled, externally pull the PGM pin to Vss to allow normal program execution.

If Single-Supply ICSP Programming mode will not be used, the LVP bit can be cleared. RB5/KBI1/PGM then becomes available as the digital I/O pin, RB5. The LVP bit may be set or cleared only when using standard high-voltage programming (VIHH applied to the MCLR/ VPP/RE3 pin). Once LVP has been disabled, only the standard high-voltage programming is available and must be used to program the device.

Memory that is not code-protected can be erased using either a block erase, or erased row by row, then written at any specified VDD. If code-protected memory is to be erased, a block erase is required. If a block erase is to be performed when using Low-Voltage Programming, the device must be supplied with VDD of 4.5V to 5.5V.

24.2.2 EXTENDED INSTRUCTION SET

ADD	OFSR	Add Lite	Add Literal to FSR					
Synta	ax:	ADDFSR	ADDFSR f, k					
Operands:		0 ≤ k ≤ 63 f ∈ [0 1	$0 \le k \le 63$					
Oper	ation:	FSR(f) + k	$s \rightarrow FSR($	f)				
Statu	s Affected:	None						
Enco	ding:	1110	1000	ffk	k	kkkk		
Description:		The 6-bit l contents c	The 6-bit literal 'k' is added to the contents of the FSR specified by 'f'.					
Word	ls:	1	1					
Cycle	es:	1	1					
Q Cycle Activity:								
	Q1	Q2	Q3			Q4		
	Decode	Read	Proce	SS	٧	Vrite to		
		literal 'k'	Data	a		FSR		

ADDFSR 2, 23h

03FFh

= 0422h

Syntax:	ADDULN	ADDULNK k					
Operands:	$0 \le k \le 6$	$0 \le k \le 63$					
Operation:	FSR2 + I	$s \rightarrow FSR2$,				
	$(TOS) \rightarrow$	PC					
Status Affected:	None						
Encoding:	1110	1000	11kk	kkkk			
	TOS. TOS. The instr execute; the secon This may case of th where f = only on F	The 6-bit literal 'k' is added to the contents of FSR2. A RETURN is then executed by loading the PC with the TOS. The instruction takes two cycles to execute; a NOP is performed during the second cycle. This may be thought of as a special case of the ADDFSR instruction, where f = 3 (binary '11'); it operates only on FSR2.					
Words:	1						
Cycles:	2						

Add Literal to FSR2 and Return

Q Cycle Activity:

ADDULNK

Q1	Q2	Q3	Q4
Decode	Read	Process	Write to
	literal 'k'	Data	FSR
No	No	No	No
Operation	Operation	Operation	Operation

Example: ADDULNK 23h

Before Instruction								
FSR2	=	03FFh						
PC	=	0100h						
After Instruction								
FSR2	=	0422h						
PC	=	(TOS)						

Note: All PIC18 instructions may take an optional label argument preceding the instruction mnemonic for use in symbolic addressing. If a label is used, the instruction syntax then becomes: {label} instruction argument(s).

Example:

Before Instruction FSR2 =

After Instruction

FSR2

26.2 DC Characteristics: Power-Down and Supply Current PIC18F2420/2520/4420/4520 (Industrial) PIC18LF2420/2520/4420/4520 (Industrial) (Continued)

PIC18LF24 (Indust	Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial							
PIC18F242 (Indust	$\begin{array}{llllllllllllllllllllllllllllllllllll$							
Param No.	Device	Тур	Max	Units	Conditions			
	Supply Current (IDD) ⁽²⁾							
	PIC18LF2X2X/4X20	250	350	μΑ	-40°C			
		260	350	μΑ	+25°C	VDD = 2.0V		
		250	350	μA	+85°C			
	PIC18LF2X2X/4X20	550	650	μΑ	-40°C			
		480	640	μΑ	+25°C	VDD = 3.0V	Fosc = 1 MHz	
		460	600	μA	+85°C		EC oscillator)	
	All devices	1.2	1.5	mA	-40°C			
		1.1	1.4	mA	+25°C			
		1.0	1.3	mA	+85°C	VDD = 5.0V		
	Extended devices only	1.0	3.0	mA	+125°C			
	PIC18LF2X2X/4X20	0.72	1.0	mA	-40°C			
		0.74	1.0	mA	+25°C	VDD = 2.0V	Fosc = 4 MHz (PRI_RUN , EC oscillator)	
		0.74	1.0	mA	+85°C			
	PIC18LF2X2X/4X20	1.3	1.8	mA	-40°C			
		1.3	1.8	mA	+25°C	VDD = 3.0V		
		1.3	1.8	mA	+85°C			
	All devices	2.7	4.0	mA	-40°C			
		2.6	4.0	mA	+25°C			
		2.5	4.0	mA	+85°C	VDD = 3.0V		
	Extended devices only	2.6	5.0	mA	+125°C			
	Extended devices only	8.4	13	mA	+125°C	VDD = 4.2V	Fosc = 25 MHz	
		11	16	mA	+125°C	VDD = 5.0V	(PRI_RUN , EC oscillator)	
	All devices	15	20	mA	-40°C			
		15	20	mA	+25°C	VDD = 4.2V		
		15	20	mA	+85°C			
	All devices	20	25	mA	-40°C		EC oscillator)	
		20	25	mA	+25°C	VDD = 5.0V	,	
		20	25	mA	+85°C			

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSs and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD or VSS;

- MCLR = VDD; WDT enabled/disabled as specified.
- **3:** When operation below -10°C is expected, use T1OSC High-Power mode, where LPT1OSC (CONFIG3H<2>) = 0. When operation will always be above -10°C, then the low-power Timer1 oscillator may be selected.
- 4: BOR and HLVD enable internal band gap reference. With both modules enabled, current consumption will be less than the sum of both specifications.

26.4.3 TIMING DIAGRAMS AND SPECIFICATIONS





TABLE 26-6: EXTERNAL CLOCK TIMING REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Мах	Units	Conditions
1A	Fosc	External CLKI Frequency ⁽¹⁾	DC	1	MHz	XT, RC Oscillator mode
			DC	25	MHz	HS Oscillator mode
			DC	31.25	kHz	LP Oscillator mode
		Oscillator Frequency ⁽¹⁾	DC	40	MHz	EC Oscillator mode
			DC	4	MHz	RC Oscillator mode
			0.1	4	MHz	XT Oscillator mode
			4	25	MHz	HS Oscillator mode
			4	10	MHz	HS + PLL Oscillator mode
			5	200	kHz	LP Oscillator mode
1	Tosc	External CLKI Period ⁽¹⁾	1000	—	ns	XT, RC Oscillator mode
			40	—	ns	HS Oscillator mode
			32	—	μs	LP Oscillator mode
		Oscillator Period ⁽¹⁾	25	—	ns	EC Oscillator mode
			250	—	ns	RC Oscillator mode
			0.25	10	μs	XT Oscillator mode
			40	250	ns	HS Oscillator mode
			100	250	ns	HS + PLL Oscillator mode
			5	200	μs	LP Oscillator mode
2	Тсү	Instruction Cycle Time ⁽¹⁾	100	—	ns	Tcy = 4/Fosc, Industrial
			160	—	ns	Tcy = 4/Fosc, Extended
3	TosL,	External Clock in (OSC1)	30	—	ns	XT Oscillator mode
	IOSH	High or Low Time	2.5	—	μs	LP Oscillator mode
			10	—	ns	HS Oscillator mode
4	TosR,	External Clock in (OSC1)	—	20	ns	XT Oscillator mode
	IOSF	Rise or Fall Time	—	50	ns	LP Oscillator mode
			—	7.5	ns	HS Oscillator mode

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period for all configurations except PLL. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKI pin. When an external clock input is used, the "max." cycle time limit is "DC" (no clock) for all devices.

PIC18F2420/2520/4420/4520







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