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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf4420-i-p

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC18F2420 PIC18LF2420
- PIC18F2520 PIC18LF2520
- PIC18F4420 PIC18LF4420
- PIC18F4520
 PIC18LF4520

This family offers the advantages of all PIC18 microcontrollers – namely, high computational performance at an economical price – with the addition of high-endurance, Enhanced Flash program memory. On top of these features, the PIC18F2420/2520/4420/4520 family introduces design enhancements that make these microcontrollers a logical choice for many high-performance, power sensitive applications.

1.1 New Core Features

1.1.1 nanoWatt TECHNOLOGY

All of the devices in the PIC18F2420/2520/4420/4520 family incorporate a range of features that can significantly reduce power consumption during operation. Key items include:

- Alternate Run Modes: By clocking the controller from the Timer1 source or the internal oscillator block, power consumption during code execution can be reduced by as much as 90%.
- **Multiple Idle Modes:** The controller can also run with its CPU core disabled but the peripherals still active. In these states, power consumption can be reduced even further, to as little as 4% of normal operation requirements.
- On-the-Fly Mode Switching: The powermanaged modes are invoked by user code during operation, allowing the user to incorporate power-saving ideas into their application's software design.
- Low Consumption in Key Modules: The power requirements for both Timer1 and the Watchdog Timer are minimized. See Section 26.0 "Electrical Characteristics" for values.

1.1.2 MULTIPLE OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC18F2420/2520/4420/4520 family offer ten different oscillator options, allowing users a wide range of choices in developing application hardware. These include:

- Four Crystal modes, using crystals or ceramic resonators
- Two External Clock modes, offering the option of using two pins (oscillator input and a divide-by-4 clock output) or one pin (oscillator input, with the second pin reassigned as general I/O)
- Two External RC Oscillator modes with the same pin options as the External Clock modes
- An internal oscillator block which provides an 8 MHz clock and an INTRC source (approximately 31 kHz), as well as a range of 6 user-selectable clock frequencies, between 125 kHz to 4 MHz, for a total of 8 clock frequencies. This option frees the two oscillator pins for use as additional general purpose I/O.
- A Phase Lock Loop (PLL) frequency multiplier, available to both the High-Speed Crystal and Internal Oscillator modes, which allows clock speeds of up to 40 MHz. Used with the internal oscillator, the PLL gives users a complete selection of clock speeds, from 31 kHz to 32 MHz – all without using an external crystal or clock circuit.

Besides its availability as a clock source, the internal oscillator block provides a stable reference source that gives the family additional features for robust operation:

- Fail-Safe Clock Monitor: This option constantly monitors the main clock source against a reference signal provided by the internal oscillator. If a clock failure occurs, the controller is switched to the internal oscillator block, allowing for continued low-speed operation or a safe application shutdown.
- **Two-Speed Start-up:** This option allows the internal oscillator to serve as the clock source from Power-on Reset, or wake-up from Sleep mode, until the primary clock source is available.

5.3 Data Memory Organization

Note: The operation of some aspects of data memory are changed when the PIC18 extended instruction set is enabled. See Section 5.5 "Data Memory and the Extended Instruction Set" for more information.

The data memory in PIC18 devices is implemented as static RAM. Each register in the data memory has a 12-bit address, allowing up to 4096 bytes of data memory. The memory space is divided into as many as 16 banks that contain 256 bytes each; PIC18F2420/2520/4420/4520 devices implement all 16 banks. Figure 5-5 shows the data memory organization for the PIC18F2420/2520/4420/4520 devices.

The data memory contains Special Function Registers (SFRs) and General Purpose Registers (GPRs). The SFRs are used for control and status of the controller and peripheral functions, while GPRs are used for data storage and scratchpad operations in the user's application. Any read of an unimplemented location will read as '0's.

The instruction set and architecture allow operations across all banks. The entire data memory may be accessed by Direct, Indirect or Indexed Addressing modes. Addressing modes are discussed later in this subsection.

To ensure that commonly used registers (SFRs and select GPRs) can be accessed in a single cycle, PIC18 devices implement an Access Bank. This is a 256-byte memory space that provides fast access to SFRs and the lower portion of GPR Bank 0 without using the BSR. **Section 5.3.2** "Access Bank" provides a detailed description of the Access RAM.

5.3.1 BANK SELECT REGISTER (BSR)

Large areas of data memory require an efficient addressing scheme to make rapid access to any address possible. Ideally, this means that an entire address does not need to be provided for each read or write operation. For PIC18 devices, this is accomplished with a RAM banking scheme. This divides the memory space into 16 contiguous banks of 256 bytes. Depending on the instruction, each location can be addressed directly by its full 12-bit address, or an 8-bit low-order address and a 4-bit Bank Pointer.

Most instructions in the PIC18 instruction set make use of the Bank Pointer, known as the Bank Select Register (BSR). This SFR holds the 4 Most Significant bits of a location's address; the instruction itself includes the 8 Least Significant bits. Only the four lower bits of the BSR are implemented (BSR<3:0>). The upper four bits are unused; they will always read '0' and cannot be written to. The BSR can be loaded directly by using the MOVLB instruction.

The value of the BSR indicates the bank in data memory; the 8 bits in the instruction show the location in the bank and can be thought of as an offset from the bank's lower boundary. The relationship between the BSR's value and the bank division in data memory is shown in Figure 5-7.

Since up to 16 registers may share the same low-order address, the user must always be careful to ensure that the proper bank is selected before performing a data read or write. For example, writing what should be program data to an 8-bit address of F9h while the BSR is 0Fh will end up resetting the program counter.

While any bank can be selected, only those banks that are actually implemented can be read or written to. Writes to unimplemented banks are ignored, while reads from unimplemented banks will return '0's. Even so, the STATUS register will still be affected as if the operation was successful. The data memory map in Figure 5-5 indicates which banks are implemented.

In the core PIC18 instruction set, only the MOVFF instruction fully specifies the 12-bit address of the source and target registers. This instruction ignores the BSR completely when it executes. All other instructions include only the low-order address as an operand and must use either the BSR or the Access Bank to locate their target registers.

NOTES:

8.0 8 x 8 HARDWARE MULTIPLIER

8.1 Introduction

All PIC18 devices include an 8 x 8 hardware multiplier as part of the ALU. The multiplier performs an unsigned operation and yields a 16-bit result that is stored in the product register pair, PRODH:PRODL. The multiplier's operation does not affect any flags in the STATUS register.

Making multiplication a hardware operation allows it to be completed in a single instruction cycle. This has the advantages of higher computational throughput and reduced code size for multiplication algorithms and allows the PIC18 devices to be used in many applications previously reserved for digital signal processors. A comparison of various hardware and software multiply operations, along with the savings in memory and execution time, is shown in Table 8-1.

8.2 Operation

Example 8-1 shows the instruction sequence for an 8 x 8 unsigned multiplication. Only one instruction is required when one of the arguments is already loaded in the WREG register.

Example 8-2 shows the sequence to do an 8 x 8 signed multiplication. To account for the sign bits of the arguments, each argument's Most Significant bit (MSb) is tested and the appropriate subtractions are done.

EXAMPLE 8-1:	8 x 8 UNSIGNED MULTIPLY
	ROUTINE

MOVF	ARG1, W	;
MULWF	ARG2	; ARG1 * ARG2 ->
		; PRODH:PRODL

8 x 8 SIGNED MULTIPLY

EXAMPLE 8-2:

		ROUTINE	
MOVF	ARG1, W		
MULWF	ARG2	; ARG1 * ARG2 ->	
		; PRODH:PRODL	
BTFSC	ARG2, SB	; Test Sign Bit	
SUBWF	PRODH, F	; PRODH = PRODH	
		; - ARG1	
MOVF	ARG2, W		
BTFSC	ARG1, SB	; Test Sign Bit	
SUBWF	PRODH, F	; PRODH = PRODH	
		; – ARG2	

		Program	Cycles	Time			
Routine	Multiply Method	Memory (Words)	(Max)	@ 40 MHz	@ 10 MHz	@ 4 MHz	
9 x 9 uppigpod	Without hardware multiply	13	69	6.9 μs	27.6 μs	69 µs	
8 x 8 unsigned	Hardware multiply	1	1	100 ns	400 ns	1 μs	
⁹ x ⁹ signed	Without hardware multiply	33	91	9.1 μs	36.4 μs	91 µs	
8 x 8 signed	Hardware multiply	6	6	600 ns	2.4 μs	6 µs	
16 x 16 uppigpod	Without hardware multiply	21	242	24.2 μs	96.8 μs	242 μs	
To X To unsigned	Hardware multiply	28	28	2.8 μs	11.2 μs	28 µs	
10 × 10 signed	Without hardware multiply	52	254	25.4 μs	102.6 μs	254 μs	
To x To signed	Hardware multiply	35	40	4.0 μs	16.0 μs	40 µs	

TABLE 8-1: PERFORMANCE COMPARISON FOR VARIOUS MULTIPLY OPERATIONS

12.1 **Timer1 Operation**

Timer1 can operate in one of these modes:

- Timer
- · Synchronous Counter
- Asynchronous Counter

The operating mode is determined by the clock select bit, TMR1CS (T1CON<1>). When TMR1CS is cleared (= 0), Timer1 increments on every internal instruction

cycle (Fosc/4). When the bit is set, Timer1 increments on every rising edge of the Timer1 external clock input or the Timer1 oscillator, if enabled.

When Timer1 is enabled, the RC1/T1OSI and RC0/ T1OSO/T13CKI pins become inputs. This means the values of TRISC<1:0> are ignored and the pins are read as '0'.



FIGURE 12-2: TIMER1 BLOCK DIAGRAM (16-BIT READ/WRITE MODE)



FIGURE 12-1: TIMER1 BLOCK DIAGRAM

15.0 CAPTURE/COMPARE/PWM (CCP) MODULES

PIC18F2420/2520/4420/4520 devices all have two CCP (Capture/Compare/PWM) modules. Each module contains a 16-bit register which can operate as a 16-bit Capture register, a 16-bit Compare register or a PWM Master/Slave Duty Cycle register.

In 28-pin devices, the two standard CCP modules (CCP1 and CCP2) operate as described in this chapter. In 40/ 44-pin devices, CCP1 is implemented as an Enhanced CCP module with standard Capture and Compare modes and Enhanced PWM modes. The ECCP implementation is discussed in **Section 16.0 "Enhanced Capture/Compare/PWM (ECCP) Module"**. The capture and compare operations described in this chapter apply to all standard and Enhanced CCP modules.

Note: Throughout this section and Section 16.0 "Enhanced Capture/Compare/PWM (ECCP) Module", references to the register and bit names for CCP modules are referred to generically by the use of 'x' or 'y' in place of the specific module number. Thus, "CCPxCON" might refer to the control register for CCP1, CCP2 or ECCP1. "CCPxCON" is used throughout these sections to refer to the module control register, regardless of whether the CCP module is a standard or enhanced implementation.

REGISTER 15-1:	CCPxCON: CCPx CONTROL REGISTER (28-PIN DEVICES)
----------------	---

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DCxB1	DCxB0	CCPxM3	CCPxM2	CCPxM1	CCPxM0
bit 7							bit 0

Legend:R = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 DCxB<1:0>: PWM Duty Cycle bit 1 and bit 0 for CCPx Module

Capture mode: Unused.

Compare mode:

Unused.

PWM mode:

These bits are the two LSbs (bit 1 and bit 0) of the 10-bit PWM duty cycle. The eight MSbs (DCxB<9:2>) of the duty cycle are found in CCPRxL.

bit 3-0 CCPxM<3:0>: CCPx Module Mode Select bits

- 0000 = Capture/Compare/PWM disabled (resets CCPx module)
- 0001 = Reserved
- 0010 = Compare mode, toggle output on match (CCPxIF bit is set)
- 0011 = Reserved
- 0100 = Capture mode, every falling edge
- 0101 = Capture mode, every rising edge
- 0110 = Capture mode, every 4th rising edge
- 0111 = Capture mode, every 16th rising edge
- 1000 = Compare mode, initialize CCPx pin low; on compare match, force CCPx pin high (CCPxIF bit is set)
- 1001 = Compare mode, initialize CCPx pin high; on compare match, force CCPx pin low (CCPxIF bit is set)
- 1010 = Compare mode, generate software interrupt on compare match (CCPxIF bit is set, CCPx pin reflects I/O state)
- 1011 = Compare mode, trigger special event; reset timer; CCP2 match starts A/D conversion (CCPxIF bit is set)
- 11xx = PWM mode

16.4.7.1 Auto-Shutdown and Automatic Restart

The auto-shutdown feature can be configured to allow automatic restarts of the module following a shutdown event. This is enabled by setting the PRSEN bit of the PWM1CON register (PWM1CON<7>).

In Shutdown mode with PRSEN = 1 (Figure 16-10), the ECCPASE bit will remain set for as long as the cause of the shutdown continues. When the shutdown condition clears, the ECCPASE bit is cleared. If PRSEN = 0 (Figure 16-11), once a shutdown condition occurs, the ECCPASE bit will remain set until it is cleared by firmware. Once ECCPASE is cleared, the Enhanced PWM will resume at the beginning of the next PWM period.

Note:	Writing to the ECCPASE bit is disabled
	while a shutdown condition is active.

Independent of the PRSEN bit setting, if the autoshutdown source is one of the comparators, the shutdown condition is a level. The ECCPASE bit cannot be cleared as long as the cause of the shutdown persists.

The Auto-Shutdown mode can be forced by writing a '1' to the ECCPASE bit.

16.4.8 START-UP CONSIDERATIONS

When the ECCP module is used in the PWM mode, the application hardware must use the proper external pullup and/or pull-down resistors on the PWM output pins. When the microcontroller is released from Reset, all of the I/O pins are in the high-impedance state. The external circuits must keep the power switch devices in the OFF state until the microcontroller drives the I/O pins with the proper signal levels or activates the PWM output(s).

The CCP1M<1:0> bits (CCP1CON<1:0>) allow the user to choose whether the PWM output signals are active-high or active-low for each pair of PWM output pins (P1A/P1C and P1B/P1D). The PWM output polarities must be selected before the PWM pins are configured as outputs. Changing the polarity configuration while the PWM pins are configured as outputs is not recommended, since it may result in damage to the application circuits.

The P1A, P1B, P1C and P1D output latches may not be in the proper states when the PWM module is initialized. Enabling the PWM pins for output at the same time as the ECCP module may cause damage to the application circuit. The ECCP module must be enabled in the proper output mode and complete a full PWM cycle before configuring the PWM pins as outputs. The completion of a full PWM cycle is indicated by the TMR2IF bit being set as the second PWM period begins.

FIGURE 16-10: PWM AUTO-SHUTDOWN (PRSEN = 1, AUTO-RESTART ENABLED)



FIGURE 16-11: PWM AUTO-SHUTDOWN (PRSEN = 0, AUTO-RESTART DISABLED)



17.3.3 ENABLING SPI I/O

To enable the serial port, MSSP Enable bit, SSPEN (SSPCON1<5>), must be set. To reset or reconfigure SPI mode, clear the SSPEN bit, reinitialize the SSPCON registers and then set the SSPEN bit. This configures the SDI, SDO, SCK and SS pins as serial port pins. For the pins to behave as the serial port function, some must have their data direction bits (in the TRIS register) appropriately programmed as follows:

- · SDI is automatically controlled by the SPI module
- SDO must have TRISC<5> bit cleared
- SCK (Master mode) must have TRISC<3> bit cleared
- SCK (Slave mode) must have TRISC<3> bit set
- SS must have TRISA<5> bit set

Any serial port function that is not desired may be overridden by programming the corresponding data direction (TRIS) register to the opposite value.

17.3.4 TYPICAL CONNECTION

Figure 17-2 shows a typical connection between two microcontrollers. The master controller (Processor 1) initiates the data transfer by sending the SCK signal. Data is shifted out of both shift registers on their programmed clock edge and latched on the opposite edge of the clock. Both processors should be programmed to the same Clock Polarity (CKP), then both controllers would send and receive data at the same time. Whether the data is meaningful (or dummy data) depends on the application software. This leads to three scenarios for data transmission:

- · Master sends data Slave sends dummy data
- · Master sends data Slave sends data
- · Master sends dummy data Slave sends data



FIGURE 17-2: SPI MASTER/SLAVE CONNECTION

17.4 I²C Mode

The MSSP module in I^2C mode fully implements all master and slave functions (including general call support) and provides interrupts on Start and Stop bits in hardware to determine a free bus (multi-master function). The MSSP module implements the standard mode specifications, as well as 7-Bit and 10-Bit Addressing modes.

Two pins are used for data transfer:

- Serial clock (SCL) RC3/SCK/SCL
- Serial data (SDA) RC4/SDI/SDA

The user must configure these pins as inputs or outputs through the TRISC<4:3> bits.

FIGURE 17-7: MSSP BLOCK DIAGRAM (I²C MODE)



17.4.1 REGISTERS

The MSSP module has six registers for $\mathsf{I}^2\mathsf{C}$ operation. These are:

- MSSP Control Register 1 (SSPCON1)
- MSSP Control Register 2 (SSPCON2)
- MSSP Status Register (SSPSTAT)
- Serial Receive/Transmit Buffer Register (SSPBUF)
- MSSP Shift Register (SSPSR) Not directly accessible
- MSSP Address Register (SSPADD)

SSPCON1, SSPCON2 and SSPSTAT are the control and status registers in I^2C mode operation. The SSPCON1 and SSPCON2 registers are readable and writable. The lower 6 bits of the SSPSTAT are read-only. The upper two bits of the SSPSTAT are read/write.

SSPSR is the shift register used for shifting data in or out. SSPBUF is the buffer register to which data bytes are written to or read from.

SSPADD register holds the slave device address when the MSSP is configured in I²C Slave mode. When the MSSP is configured in Master mode, the lower seven bits of SSPADD act as the Baud Rate Generator reload value.

In receive operations, SSPSR and SSPBUF together create a double-buffered receiver. When SSPSR receives a complete byte, it is transferred to SSPBUF and the SSPIF interrupt is set.

During transmission, the SSPBUF is not doublebuffered. A write to SSPBUF will write to both SSPBUF and SSPSR.





The value in the ADRESH:ADRESL registers is not modified for a Power-on Reset. The ADRESH:ADRESL registers will contain unknown data after a Power-on Reset.

After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as an input. To determine acquisition time, see **Section 19.1 "A/D Acquisition Requirements"**. After this acquisition time has elapsed, the A/D conversion can be started. An acquisition time can be programmed to occur between setting the GO/DONE bit and the actual start of the conversion.

The following steps should be followed to perform an A/D conversion:

- 1. Configure the A/D module:
 - Configure analog pins, voltage reference and digital I/O (ADCON1)
 - Select A/D input channel (ADCON0)
 - · Select A/D acquisition time (ADCON2)
 - Select A/D conversion clock (ADCON2)
 - Turn on A/D module (ADCON0)
- 2. Configure A/D interrupt (if desired):
 - · Clear ADIF bit
 - Set ADIE bit
 - Set GIE bit
- 3. Wait the required acquisition time (if required).
- 4. Start conversion:
 - Set GO/DONE bit (ADCON0 register)

- 5. Wait for A/D conversion to complete, by either:
 - Polling for the GO/DONE bit to be cleared
 OR

• Waiting for the A/D interrupt

- 6. Read A/D Result registers (ADRESH:ADRESL); clear bit, ADIF, if required.
- 7. For next conversion, go to step 1 or step 2, as required. The A/D conversion time per bit is defined as TAD. A minimum wait of 2 TAD is required before the next acquisition starts.

FIGURE 19-2: A/D TRANSFER FUNCTION





21.0 COMPARATOR VOLTAGE REFERENCE MODULE

The comparator voltage reference is a 16-tap resistor ladder network that provides a selectable reference voltage. Although its primary purpose is to provide a reference for the analog comparators, it may also be used independently of them.

A block diagram of the module is shown in Figure 21-1. The resistor ladder is segmented to provide two ranges of CVREF values and has a power-down function to conserve power when the reference is not being used. The module's supply reference can be provided from either device VDD/VSS or an external voltage reference.

21.1 Configuring the Comparator Voltage Reference

The voltage reference module is controlled through the CVRCON register (Register 21-1). The comparator voltage reference provides two ranges of output voltage, each with 16 distinct levels. The range to be used

is selected by the CVRR bit (CVRCON<5>). The primary difference between the ranges is the size of the steps selected by the CVREF Selection bits (CVR<3:0>), with one range offering finer resolution. The equations used to calculate the output of the comparator voltage reference are as follows:

If CVRR = 1:

CVREF = ((CVR<3:0>)/24) x CVRSRC

<u>If CVRR = 0:</u>

CVREF = (CVRSRC x 1/4) + (((CVR<3:0>)/32) x CVRSRC)

The comparator reference supply voltage can come from either VDD and Vss, or the external VREF+ and VREF- that are multiplexed with RA2 and RA3. The voltage source is selected by the CVRSS bit (CVRCON<4>).

The settling time of the comparator voltage reference must be considered when changing the CVREF output (see Table 26-3 in **Section 26.0 "Electrical Characteristics"**).

REGISTER 21-1: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
CVREN	CVROE ⁽¹⁾	CVRR	CVRSS	CVR3	CVR2	CVR1	CVR0	
bit 7	÷						bit 0	
l								
Legend:								
R = Readal	ble bit	W = Writable	bit	U = Unimplem	nented bit, read	l as '0'		
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown	
bit 7	CVREN: Con	nparator Voltag	e Reference E	nable bit				
	1 = CVREF ci	rcuit powered of	on					
	0 = CVREF ci	rcuit powered of	down					
bit 6	CVROE: Con	nparator VREF (Output Enable	bit ⁽¹⁾				
	1 = CVREF V	oltage level is a	Ilso output on f	he RA2/AN2/Vi	REF-/CVREF pin			
	0 = CVREF V	oltage is discon	nected from th	ne RA2/AN2/VR	EF-/CVREF pin			
bit 5	CVRR: Comp	arator VREF Ra	ange Selection	bit				
	1 = 0 to 0.66	7 CVRSRC, with	CVRSRC/24 s	tep size (low ra	nge)			
	0 = 0.25 CVRSRC to 0.75 CVRSRC, with CVRSRC/32 step size (high range)							
bit 4	CVRSS: Corr	parator VREF S	Source Selection	on bit				
	1 = Compara	tor reference s	ource, CVRSR	C = (VREF+) - (\	/REF-)			
	0 = Compara	tor reference s	ource, CVRSR	c = VDD - Vss				
bit 3-0	CVR3:CVR0:	Comparator V	REE Value Sele	ection bits $(0 < 0)$	CVR<3:0>) < 1	5)		

bit 3-0	CVR3:CVR0: Comparator VREF Value Selection bits (0 ≤ (CVR<3:0>) ≤
	When CVRR = 1:
	$CVREF = ((CVR<3:0>)/24) \bullet (CVRSRC)$
	When CVRR = 0:
	CVREF = (CVRSRC/4) + ((CVR<3:0>)/32) • (CVRSRC)

Note 1: CVROE overrides the TRISA<2> bit setting.

23.5 Program Verification and Code Protection

The overall structure of the code protection on the PIC18 Flash devices differs significantly from other $\text{PIC}^{\texttt{®}}$ devices.

The user program memory is divided into five blocks. One of these is a boot block of 2 Kbytes. The remainder of the memory is divided into four blocks on binary boundaries. Each of the five blocks has three code protection bits associated with them. They are:

- Code-Protect bit (CPn)
- Write-Protect bit (WRTn)
- External Block Table Read bit (EBTRn)

Figure 23-5 shows the program memory organization for 16 and 32-Kbyte devices and the specific code protection bit associated with each block. The actual locations of the bits are summarized in Table 23-3.

FIGURE 23-5: CODE-PROTECTED PROGRAM MEMORY FOR PIC18F2420/2520/4420/4520

MEMORY S	IZE/DEVICE		Plack Code Protoction		
16 Kbytes 32 Kbytes (PIC18F2420/4420) (PIC18F2520/4520)		Address Range	Controlled By:		
Boot Block	Boot Block	000000h 0007FFh	CPB, WRTB, EBTRB		
Block 0	Block 0	000800h 001FFFh	CP0, WRT0, EBTR0		
Block 1	Block 1	002000h 003FFFh	CP1, WRT1, EBTR1		
	Block 2	004000h 005FFFh	CP2, WRT2, EBTR2		
	Block 3	006000h 007FFFh	CP3, WRT3, EBTR3		
Unimplemented Read '0's	Unimplemented Read '0's		(Unimplemented Memory Space)		
		1FFFFFh			

TABLE 23-3: SUMMARY OF CODE PROTECTION REGISTERS

File	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3 Bit 2		Bit 1	Bit 0
300008h	CONFIG5L	_	_			CP3 ⁽¹⁾	CP2 ⁽¹⁾	CP1	CP0
300009h	CONFIG5H	CPD	CPB	—	_	_	—	-	_
30000Ah	CONFIG6L	—	_	—	_	WRT3 ⁽¹⁾	WRT2 ⁽¹⁾	WRT1	WRT0
30000Bh	CONFIG6H	WRTD	WRTB	WRTC	_	_	—		_
30000Ch	CONFIG7L	—	—	—	-	EBTR3 ⁽¹⁾	EBTR2 ⁽¹⁾	EBTR1	EBTR0
30000Dh	CONFIG7H	—	EBTRB	_	_	_	_	_	_

Legend: Shaded cells are unimplemented.

Note 1: Unimplemented in PIC18F2420/4420 devices; maintain this bit set.

BTG	Bit Toggle f		BOV	BOV		Branch if Overflow			
Syntax:	BTG f, b {,a}			Synta	ax:	BOV n			
Operands:	0 ≤ f ≤ 255			Oper	ands:	-128 ≤ n ≤ 127			
	0 ≤ b < 7 a ∈ [0,1]			Oper	ation:	if Overflow bit is '1', (PC) + 2 + 2n \rightarrow PC			
Operation: $(\overline{f < b^>}) \rightarrow f < b^>$			Statu	s Affected:	None				
Status Affected:	None			Enco	dina:	1110	0100 nnr	nn nnnn	
Encoding:	0111 bbba ffff ffff			Desc	rintion:	If the Overflow bit is '1', then the program will branch. The 2's complement number, '2n', is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is then a two-cycle instruction. 1 1(2)			
Description:	Bit b in data memory location 'f' is inverted. If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default). If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See Section 24.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode" for details.		Word Cycle Q C	s: es: ycle Activity: mo:					
Words:	1			1100	Q1	Q2	Q3	Q4	
Cycles: 1			Decode	Read literal	Process	Write to PC			
Q Cycle Activity						'n'	Data		
Q1	Q2	Q3 Q4			No operation	No operation	No operation	No operation	
Decode	Read	Proces	s Write	lf No	Jump:				
	register f	Data	register T		Q1	Q2	Q3	Q4	
Example:	BTG P	ORTC, 4	, 0		Decode	Read literal 'n'	Process Data	No operation	
Before Instruct PORTC After Instructi PORTC	ction: = 0111 (on: = 0110 (0101 [75h]	<u>Exan</u>	nple: PC After Instruction If Overflor PC If Overflor PC	HERE stion = add on = 1; w = 1; w = 0; w = 0; = add	BOV Jump dress (HERE) dress (Jump) dress (HERE	+ 2)	

26.2

DC Characteristics: Power-Down and Supply Current PIC18F2420/2520/4420/4520 (Industrial) PIC18LF2420/2520/4420/4520 (Industrial) (Continued)

PIC18LF2420/2520/4420/4520 (Industrial)		Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial								
PIC18F2420/2520/4420/4520 (Industrial, Extended)		Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended								
Param Device		Тур	Max	Units	Conditions					
	Supply Current (IDD) ⁽²⁾									
	PIC18LF2X2X/4X20	165	250	μA	-40°C					
		175	250	μΑ	+25°C	VDD = 2.0V				
		190	270	μΑ	+85°C					
	PIC18LF2X2X/4X20	250	360	μΑ	-40°C					
		270	360	μA	+25°C	VDD = 3.0V	Fosc = 1 MHz			
		290	380	μΑ	+85°C					
	All devices	500	700	μΑ	-40°C					
		520	700	μA	+25°C					
		550	700	μA	+85°C	VDD - 5.0V				
	Extended devices only	0.6	1	mA	+125°C					
	PIC18LF2X2X/4X20	340	500	μA	-40°C					
		350	500	μΑ	+25°C	VDD = 2.0V				
		360	500	μA	+85°C					
	PIC18LF2X2X/4X20	520	800	μA	-40°C					
		540	800	μA	+25°C	VDD = 3.0V	FOSC = 4 MHz			
		580	850	μA	+85°C		INTOSC source)			
	All devices	1.0	1.6	mA	-40°C					
		1.1	1.4	mA	+25°C					
		1.1	1.4	mA	+85°C	vuu = 5.0v				
	Extended devices only	1.1	2.0	mA	+125°C	1				

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

- OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD or VSS; MCLR = VDD; WDT enabled/disabled as specified.
- **3:** When operation below -10°C is expected, use T1OSC High-Power mode, where LPT1OSC (CONFIG3H<2>) = 0. When operation will always be above -10°C, then the low-power Timer1 oscillator may be selected.
- 4: BOR and HLVD enable internal band gap reference. With both modules enabled, current consumption will be less than the sum of both specifications.



TABLE 26-4: HIGH/LOW-VOLTAGE DETECT CHARACTERISTICS

Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial								
Param No.	Sym	Charact	Min	Тур	Max	Units	Conditions	
D420	20 HLVD Voltage on VDD Transition High-to-Low	HLVDL<3:0> = 0000	2.06	2.17	2.28	V		
		HLVDL<3:0> = 0001	2.12	2.23	2.34	V		
		HLVDL<3:0> = 0010	2.24	2.36	2.48	V		
		HLVDL<3:0> = 0011	2.32	2.44	2.56	V		
			HLVDL<3:0> = 0100	2.47	2.60	2.73	V	
			HLVDL<3:0> = 0101	2.65	2.79	2.93	V	
			HLVDL<3:0> = 0110	2.74	2.89	3.04	V	
			HLVDL<3:0> = 0111	2.96	3.12	3.28	V	
		HLVDL<3:0> = 1000	3.22	3.39	3.56	V		
		HLVDL<3:0> = 1001	3.37	3.55	3.73	V		
		HLVDL<3:0> = 1010	3.52	3.71	3.90	V		
		HLVDL<3:0> = 1011	3.70	3.90	4.10	V		
			HLVDL<3:0> = 1100	3.90	4.11	4.32	V	
			HLVDL<3:0> = 1101	4.11	4.33	4.55	V	
			HLVDL<3:0> = 1110	4.36	4.59	4.82	V	

Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial







FIGURE 27-6: TYPICAL TIOSC DELTA CURRENT vs. VDD ACROSS TEMP. (DEVICE IN SLEEP,

NOTES:

INDEX

Α	
A/D	223
Acquisition Requirements	228
ADCON0 Register	223
ADCON1 Register	223
ADCON2 Register	223
ADRESH Register223, 2	226
ADRESL Register	223
Analog Port Pins, Configuring	230
Associated Registers	232
Configuring the Module	227
Conversion Clock (TAD)	229
Conversion Status (GO/DONE Bit)	226
Conversions	231
Converter Unaracteristics	359
Disebarge	221
Operation in Power Managed Modes	231
Selecting and Configuring Acquisition Time	230
Special Event Trigger (CCP)	223
Special Event Trigger (ECCP)	148
Use of the CCP2 Trigger	232
Absolute Maximum Ratings	321
AC (Timing) Characteristics	340
Load Conditions for Device	0.0
Timing Specifications	341
Parameter Symbology	340
Temperature and Voltage Specifications	341
Timing Conditions	341
AC Characteristics	
Internal RC Accuracy	343
Access Bank	
Mapping with Indexed Literal Offset Mode	72
ACKSTAT	191
ACKSTAT Status Flag	191
ADCON0 <u>Regis</u> ter	223
GO/DONE Bit	226
ADCON1 Register	223
ADCON2 Register	223
ADDFSR	310
ADDLW	273
	310
ADDWF	273
	274
ADRESH Register	223
ADRESL Registel Converter See A/D	220
	271
	274
Assembler	215
MDASM Assembler	318
Auto-Wake-up on Sync Break Character	214
В	
Bank Select Register (BSR)	. 59
Baud Rate Generator	187
BC	275
BCF	276
BF	191

BF Status Flag......191

Block Diagrams
A/D226
Analog Input Model 227
Baud Rate Generator 187
Capture Mode Operation 141
Comparator Analog Input Model 237
Comparator I/O Operating Modes
Comparator Output 236
Comparator Voltage Reference
Comparator Voltage Reference Output
Buffer Example241
Compare Mode Operation 142
Device Clock
Enhanced PWM 149
EUSART Receive
EUSART Transmit 211
External Power-on Reset Circuit
(Slow VDD Power-up)43
Fail-Safe Clock Monitor (FSCM)
Generic I/O Port 105
High/Low-Voltage Detect with External Input
Interrupt Logic
MSSP (I ² C Master Mode) 185
MSSP (I ² C Mode)
MSSP (SPI Mode) 161
On-Chip Reset Circuit41
PIC18F2420/252010
PIC18F4420/452011
PLL (HS Mode) 25
PORTD and PORTE (Parallel Slave Port) 120
PWM Operation (Simplified) 144
Reads from Flash Program Memory77
Single Comparator
Table Read Operation73
Table Write Operation74
Table Writes to Flash Program Memory
Timer0 in 16-Bit Mode 124
Timer0 in 8-Bit Mode 124
Timer1128
Timer1 (16-Bit Read/Write Mode) 128
Timer2134
Timer3136
Timer3 (16-Bit Read/Write Mode)136
Watchdog Timer 258
BN
BNC
BNN
BNOV
BNZ
BOR. See Brown-out Reset.
BOV
BRA
Break Character (12-Bit) Transmit and Receive
BRG. See Baud Rate Generator.
Brown-out Reset (BOR)
Detecting 44
Disabling in Sleep Mode 44
Software Enabled 44
BSF279
BTFSC
BTFSS
BTG
BZ