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Details

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Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf4420-i-pt

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Features	PIC18F2420	PIC18F2520	PIC18F4420	PIC18F4520
Operating Frequency	DC – 40 MHz	DC – 40 MHz	DC – 40 MHz	DC – 40 MHz
Program Memory (Bytes)	16384	32768	16384	32768
Program Memory (Instructions)	8192	16384	8192	16384
Data Memory (Bytes)	768	1536	768	1536
Data EEPROM Memory (Bytes)	256	256	256	256
Interrupt Sources	19	19	20	20
I/O Ports	Ports A, B, C, (E)	Ports A, B, C, (E)	Ports A, B, C, D, E	Ports A, B, C, D, E
Timers	4	4	4	4
Capture/Compare/PWM Modules	2	2	1	1
Enhanced Capture/Compare/PWM Modules	0	0 1		1
Serial Communications	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART
Parallel Communications (PSP)	No	No	Yes	Yes
10-Bit Analog-to-Digital Module	10 Input Channels	10 Input Channels	13 Input Channels	13 Input Channels
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack <u>Underfl</u> ow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT
Programmable High/Low-Voltage Detect	Yes	Yes	Yes	Yes
Programmable Brown-out Reset	Yes	Yes	Yes	Yes
Instruction Set	75 Instructions; 83 with Extended Instruction Set Enabled	75 Instructions; 83 with Extended Instruction Set Enabled	75 Instructions; 83 with Extended Instruction Set Enabled	75 Instructions; 83 with Extended Instruction Set Enabled
Packages	28-Pin SPDIP 28-Pin SOIC 28-Pin QFN	28-Pin SPDIP 28-Pin SOIC 28-Pin QFN	40-Pin PDIP 44-Pin QFN 44-Pin TQFP	40-Pin PDIP 44-Pin QFN 44-Pin TQFP

TABLE 1-1: DEVICE FEATURES

2.8 Effects of Power-Managed Modes on the Various Clock Sources

When PRI_IDLE mode is selected, the designated primary oscillator continues to run without interruption. For all other power-managed modes, the oscillator using the OSC1 pin is disabled. The OSC1 pin (and OSC2 pin, if used by the oscillator) will stop oscillating.

In secondary clock modes (SEC_RUN and SEC_IDLE), the Timer1 oscillator is operating and providing the device clock. The Timer1 oscillator may also run in all power-managed modes if required to clock Timer1 or Timer3.

In internal oscillator modes (RC_RUN and RC_IDLE), the internal oscillator block provides the device clock source. The 31 kHz INTRC output can be used directly to provide the clock and may be enabled to support various special features, regardless of the powermanaged mode (see Section 23.2 "Watchdog Timer (WDT)", Section 23.3 "Two-Speed Start-up" and Section 23.4 "Fail-Safe Clock Monitor" for more information on WDT, Fail-Safe Clock Monitor and Two-Speed Start-up). The INTOSC output at 8 MHz may be used directly to clock the device or may be divided down by the postscaler. The INTOSC output is disabled if the clock is provided directly from the INTRC output.

If Sleep mode is selected, all clock sources are stopped. Since all the transistor switching currents have been stopped, Sleep mode achieves the lowest current consumption of the device (only leakage currents).

Enabling any on-chip feature that will operate during Sleep will increase the current consumed during Sleep. The INTRC is required to support WDT operation. The Timer1 oscillator may be operating to support a Real-Time Clock. Other features may be operating that do not require a device clock source (i.e., MSSP slave, PSP, INTx pins and others). Peripherals that may add significant current consumption are listed in **Section 26.2 "DC Characteristics".**

2.9 Power-up Delays

Power-up delays are controlled by two timers so that no external Reset circuitry is required for most applications. The delays ensure that the device is kept in Reset until the device power supply is stable under normal circumstances and the primary clock is operating and stable. For additional information on power-up delays, see **Section 4.5 "Device Reset Timers"**.

The first timer is the Power-up Timer (PWRT), which provides a fixed delay on power-up (parameter 33, Table 26-10). It is enabled by clearing (= 0) the PWRTEN Configuration bit.

The second timer is the Oscillator Start-up Timer (OST), intended to keep the chip in Reset until the crystal oscillator is stable (LP, XT and HS modes). The OST does this by counting 1024 oscillator cycles before allowing the oscillator to clock the device.

When the HSPLL Oscillator mode is selected, the device is kept in Reset for an additional 2 ms, following the HS mode OST delay, so the PLL can lock to the incoming clock frequency.

There is a delay of interval, TCSD (parameter 38, Table 26-10), following POR, while the controller becomes ready to execute instructions. This delay runs concurrently with any other delays. This may be the only delay that occurs when any of the EC, RC or INTIO modes are used as the primary clock source.

OSC Mode	OSC1 Pin	OSC2 Pin
RC, INTIO1	Floating, external resistor should pull high	At logic low (clock/4 output)
RCIO	Floating, external resistor should pull high	Configured as PORTA, bit 6
INTIO2	Configured as PORTA, bit 7	Configured as PORTA, bit 6
ECIO	Floating, pulled by external clock	Configured as PORTA, bit 6
EC	Floating, pulled by external clock	At logic low (clock/4 output)
LP, XT and HS	Feedback inverter disabled at quiescent voltage level	Feedback inverter disabled at quiescent voltage level

TABLE 2-3:OSC1 AND OSC2 PIN STATES IN SLEEP MODE

Note: See Table 4-2 in Section 4.0 "Reset" for time-outs due to Sleep and MCLR Reset.

3.1.3 CLOCK TRANSITIONS AND STATUS INDICATORS

The length of the transition between clock sources is the sum of two cycles of the old clock source and three to four cycles of the new clock source. This formula assumes that the new clock source is stable.

Three bits indicate the current clock source and its status. They are:

- OSTS (OSCCON<3>)
- IOFS (OSCCON<2>)
- T1RUN (T1CON<6>)

In general, only one of these bits will be set while in a given power-managed mode. When the OSTS bit is set, the primary clock is providing the device clock. When the IOFS bit is set, the INTOSC output is providing a stable 8 MHz clock source to a divider that actually drives the device clock. When the T1RUN bit is set, the Timer1 oscillator is providing the clock. If none of these bits are set, then either the INTRC clock source is clocking the device or the INTOSC source is not yet stable.

If the internal oscillator block is configured as the primary clock source by the FOSC<3:0> Configuration bits, then both the OSTS and IOFS bits may be set when in PRI_RUN or PRI_IDLE modes. This indicates that the primary clock (INTOSC output) is generating a stable 8 MHz output. Entering another power-managed RC mode at the same frequency would clear the OSTS bit.

- Note 1: Caution should be used when modifying a single IRCF bit. If VDD is less than 3V, it is possible to select a higher clock speed than is supported by the low VDD. Improper device operation may result if the VDD/Fosc specifications are violated.
 - 2: Executing a SLEEP instruction does not necessarily place the device into Sleep mode. It acts as the trigger to place the controller into either the Sleep mode or one of the Idle modes, depending on the setting of the IDLEN bit.

3.1.4 MULTIPLE SLEEP COMMANDS

The power-managed mode that is invoked with the SLEEP instruction is determined by the setting of the IDLEN bit at the time the instruction is executed. If another SLEEP instruction is executed, the device will enter the power-managed mode specified by IDLEN at that time. If IDLEN has changed, the device will enter the new power-managed mode specified by the new setting.

3.2 Run Modes

In the Run modes, clocks to both the core and peripherals are active. The difference between these modes is the clock source.

3.2.1 PRI_RUN MODE

The PRI_RUN mode is the normal, full-power execution mode of the microcontroller. This is also the default mode upon a device Reset unless Two-Speed Start-up is enabled (see **Section 23.3 "Two-Speed Start-up"** for details). In this mode, the OSTS bit is set. The IOFS bit may be set if the internal oscillator block is the primary clock source (see **Section 2.7.1 "Oscillator Control Register"**).

3.2.2 SEC_RUN MODE

The SEC_RUN mode is the compatible mode to the "clock switching" feature offered in other PIC18 devices. In this mode, the CPU and peripherals are clocked from the Timer1 oscillator. This gives users the option of lower power consumption while still using a high-accuracy clock source.

SEC_RUN mode is entered by setting the SCS<1:0> bits to '01'. The device clock source is switched to the Timer1 oscillator (see Figure 3-1), the primary oscillator is shut down, the T1RUN bit (T1CON<6>) is set and the OSTS bit is cleared.

Note: The Timer1 oscillator should already be running prior to entering SEC_RUN mode. If the T1OSCEN bit is not set when the SCS<1:0> bits are set to '01', entry to SEC_RUN mode will not occur. If the Timer1 oscillator is enabled, but not yet running, device clocks will be delayed until the oscillator has started. In such situations, initial oscillator operation is far from stable and unpredictable operation may result.

On transitions from SEC_RUN mode to PRI_RUN mode, the peripherals and CPU continue to be clocked from the Timer1 oscillator while the primary clock is started. When the primary clock becomes ready, a clock switch back to the primary clock occurs (see Figure 3-2). When the clock switch is complete, the T1RUN bit is cleared, the OSTS bit is set and the primary clock is providing the clock. The IDLEN and SCS bits are not affected by the wake-up; the Timer1 oscillator continues to run.

4.6 Reset State of Registers

Most registers are unaffected by a Reset. Their status is unknown on POR and unchanged by all other Resets. The other registers are forced to a "Reset state" depending on the type of Reset that occurred.

Most registers are not affected by a WDT wake-up, since this is viewed as the resumption of normal operation. Status bits from the RCON register, \overline{RI} , \overline{TO} , \overline{PD} , \overline{POR} and \overline{BOR} , are set or cleared differently in different Reset situations, as indicated in Table 4-3. These bits are used in software to determine the nature of the Reset. Table 4-4 describes the Reset states for all of the Special Function Registers. These are categorized by Power-on and Brown-out Resets, Master Clear and WDT Resets and WDT wake-ups.

TABLE 4-3:	STATUS BITS, THEIR SIGNIFICANCE AND THE INITIALIZATION CONDITION
	FOR RCON REGISTER

Condition	Program	RCON Register					STKPTR Register		
Condition	Counter	RI	то	PD	POR	BOR	STKFUL	STKUNF	
Power-on Reset	0000h	1	1	1	0	0	0	0	
RESET Instruction	0000h	0	u	u	u	u	u	u	
Brown-out Reset	0000h	1	1	1	u	0	u	u	
MCLR Reset during Power-Managed Run Modes	0000h	u	1	u	u	u	u	u	
MCLR Reset during Power-Managed Idle Modes and Sleep Mode	0000h	u	1	0	u	u	u	u	
WDT Time-out during Full Power or Power-Managed Run Mode	0000h	u	0	u	u	u	u	u	
MCLR Reset during Full-Power Execution	0000h	u	u	u	u	u	u	u	
Stack Full Reset (STVREN = 1)	0000h	u	u	u	u	u	1	u	
Stack Underflow Reset (STVREN = 1)	0000h	u	u	u	u	u	u	1	
Stack Underflow Error (not an actual Reset, STVREN = 0)	0000h	u	u	u	u	u	u	1	
WDT Time-out during Power-Managed Idle or Sleep Modes	PC + 2	u	0	0	u	u	u	u	
Interrupt Exit from Power-Managed Modes	PC + 2 ⁽¹⁾	u	u	0	u	u	u	u	

Legend: u = unchanged

Note 1: When the wake-up is due to an interrupt and the GIEH or GIEL bits are set, the PC is loaded with the interrupt vector (008h or 0018h).

5.4.3.1 FSR Registers and the INDF Operand

At the core of Indirect Addressing are three sets of registers: FSR0, FSR1 and FSR2. Each represents a pair of 8-bit registers, FSRnH and FSRnL. The four upper bits of the FSRnH register are not used so each FSR pair holds a 12-bit value. This represents a value that can address the entire range of the data memory in a linear fashion. The FSR register pairs, then, serve as pointers to data memory locations.

Indirect Addressing is accomplished with a set of Indirect File Operands, INDF0 through INDF2. These can be thought of as "virtual" registers: they are mapped in the SFR space but are not physically implemented. Reading or writing to a particular INDF register actually accesses its corresponding FSR register pair. A read from INDF1, for example, reads the data at the address indicated by FSR1H:FSR1L. Instructions that use the INDF registers as operands actually use the contents of their corresponding FSR as a pointer to the instruction's target. The INDF operand is just a convenient way of using the pointer.

Because Indirect Addressing uses a full 12-bit address, data RAM banking is not necessary. Thus, the current contents of the BSR and the Access RAM bit have no effect on determining the target address.

5.4.3.2 FSR Registers and POSTINC, POSTDEC, PREINC and PLUSW

In addition to the INDF operand, each FSR register pair also has four additional indirect operands. Like INDF, these are "virtual" registers that cannot be indirectly read or written to. Accessing these registers actually accesses the associated FSR register pair, but also performs a specific action on it stored value. They are:

- POSTDEC: accesses the FSR value, then automatically decrements it by 1 afterwards
- POSTINC: accesses the FSR value, then automatically increments it by 1 afterwards
- PREINC: increments the FSR value by 1, then uses it in the operation
- PLUSW: adds the signed value of the W register (range of -127 to 128) to that of the FSR and uses the new value in the operation.

In this context, accessing an INDF register uses the value in the FSR registers without changing them. Similarly, accessing a PLUSW register gives the FSR value offset by that in the W register; neither value is actually changed in the operation. Accessing the other virtual registers changes the value of the FSR registers.

Operations on the FSRs with POSTDEC, POSTINC and PREINC affect the entire register pair; that is, rollovers of the FSRnL register from FFh to 00h carry over to the FSRnH register. On the other hand, results of these operations do not change the value of any flags in the STATUS register (e.g., Z, N, OV, etc.).



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R/W-x	R/W-x	U-0	R/W-0	R/W-x	R/W-0	R/S-0	R/S-0
EEPGD	CFGS		FREE	WRERR ⁽¹⁾	WREN	WR	RD
bit 7			•				bit 0
Legend:		S = Settable b	oit (cannot be	cleared in softwa	are)		
R = Readab	le bit	W = Writable	bit	U = Unimplem	ented bit, rea	d as '0'	
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown
bit 7	EEPGD: Flas 1 = Access F 0 = Access c	sh Program or E Flash program r lata EEPROM r Program/Data	Data EEPROM nemory nemory	Memory Select	bit		
DILO	1 = Access (0 = Access F	Configuration re	gisters gistata EEPRO	OM memory			
bit 5	Unimplemen	ted: Read as '	כ'				
bit 4	FREE: Flash	Row Erase Ena	able bit				
	1 = Erase th completion 0 = Perform	e program mer on of erase ope write only	nory row addr ration)	essed by TBLP	TR on the ne	ext WR comma	nd (cleared by
bit 3	WRERR: Fla	sh Program/Da	ta EEPROM E	rror Flag bit ⁽¹⁾			
	1 = A write o operation 0 = The write	peration is prei n, or an imprope e operation com	maturely termi er write attemp ipleted	nated (any Reso ot)	et during self-	timed program	ming in normal
bit 2	WREN: Flash	n Program/Data	EEPROM Wr	ite Enable bit			
	1 = Allows w 0 = Inhibits w	rite cycles to FI vrite cycles to F	ash program/o lash program/	lata EEPROM data EEPROM			
bit 1	WR: Write Co	ontrol bit					
	1 = Initiates a (The ope can only 0 = Write cyc	a data EEPRON ration is self-tin be set (not clea cle to the EEPR	I erase/write c ned and the bi ared) in softwa OM is comple	ycle or a prograi t is cleared by ha ire.) te	m memory era ardware once	ase cycle or writ write is comple	te cycle te. The WR bit
bit 0	RD: Read Co	ontrol bit					
	1 = Initiates a be set (n 0 = Does not	an EEPROM re ot cleared) in so t initiate an EEF	ad (Read take oftware. RD bit PROM read	s one cycle. RD cannot be set w	is cleared in I hen EEPGD =	nardware. The F = 1 or CFGS = 1	RD bit can only)

REGISTER 7-1: EECON1: EEPROM CONTROL REGISTER 1

Note 1: When a WRERR occurs, the EEPGD and CFGS bits are not cleared. This allows tracing of the error condition.

15.1 CCP Module Configuration

Each Capture/Compare/PWM module is associated with a control register (generically, CCPxCON) and a data register (CCPRx). The data register, in turn, is comprised of two 8-bit registers: CCPRxL (low byte) and CCPRxH (high byte). All registers are both readable and writable.

15.1.1 CCP MODULES AND TIMER RESOURCES

The CCP modules utilize Timers 1, 2 or 3, depending on the mode selected. Timer1 and Timer3 are available to modules in Capture or Compare modes, while Timer2 is available for modules in PWM mode.

TABLE 15-1:CCP MODE – TIMER
RESOURCE

CCP/ECCP Mode	Timer Resource
Capture	Timer1 or Timer3
Compare	Timer1 or Timer3
PWM	Timer2

The assignment of a particular timer to a module is determined by the Timer to CCP enable bits in the T3CON register (Register 14-1). Both modules may be active at any given time and may share the same timer resource if they are configured to operate in the same mode (Capture/Compare or PWM) at the same time. The interactions between the two modules are summarized in Figure 15-1 and Figure 15-2. In Timer1 in Asynchronous Counter mode, the capture operation will not work.

15.1.2 CCP2 PIN ASSIGNMENT

The pin assignment for CCP2 (Capture input, Compare and PWM output) can change, based on device configuration. The CCP2MX Configuration bit determines which pin CCP2 is multiplexed to. By default, it is assigned to RC1 (CCP2MX = 1). If the Configuration bit is cleared, CCP2 is multiplexed with RB3.

Changing the pin assignment of CCP2 does not automatically change any requirements for configuring the port pin. Users must always verify that the appropriate TRIS register is configured correctly for CCP2 operation, regardless of where it is located.

TABLE 15-2: INTERACTIONS BETWEEN CCP1 AND CCP2 FOR TIMER RESOURCES

CCP1 Mode	CCP2 Mode	Interaction
Capture	Capture	Each module can use TMR1 or TMR3 as the time base. The time base can be different for each CCP.
Capture	Compare	CCP2 can be configured for the Special Event Trigger to reset TMR1 or TMR3 (depending upon which time base is used). Automatic A/D conversions on trigger event can also be done. Operation of CCP1 could be affected if it is using the same timer as a time base.
Compare	Capture	CCP1 can be configured for the Special Event Trigger to reset TMR1 or TMR3 (depending upon which time base is used). Operation of CCP2 could be affected if it is using the same timer as a time base.
Compare	Compare	Either module can be configured for the Special Event Trigger to reset the time base. Automatic A/D conversions on CCP2 trigger event can be done. Conflicts may occur if both modules are using the same time base.
Capture	PWM ⁽¹⁾	None
Compare	PWM ⁽¹⁾	None
PWM ⁽¹⁾	Capture	None
PWM ⁽¹⁾	Compare	None
PWM ⁽¹⁾	PWM ⁽¹⁾	Both PWMs will have the same frequency and update rate (TMR2 interrupt).

Note 1: Includes standard and Enhanced PWM operation.

17.0 MASTER SYNCHRONOUS SERIAL PORT (MSSP) MODULE

17.1 Master SSP (MSSP) Module Overview

The Master Synchronous Serial Port (MSSP) module is a serial interface, useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, A/D Converters, etc. The MSSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I²C)
 - Full Master mode
 - Slave mode (with general address call)

The I^2C interface supports the following modes in hardware:

- Master mode
- · Multi-Master mode
- Slave mode

17.2 Control Registers

The MSSP module has three associated registers. These include a status register (SSPSTAT) and two control registers (SSPCON1 and SSPCON2). The use of these registers and their individual configuration bits differ significantly depending on whether the MSSP module is operated in SPI or I^2C mode.

Additional details are provided under the individual sections.

17.3 SPI Mode

The SPI mode allows 8 bits of data to be synchronously transmitted and received simultaneously. All four modes of SPI are supported. To accomplish communication, typically three pins are used:

- Serial Data Out (SDO) RC5/SDO
- Serial Data In (SDI) RC4/SDI/SDA
- Serial Clock (SCK) RC3/SCK/SCL

Additionally, a fourth pin may be used when in a Slave mode of operation:

Slave Select (SS) – RA5/SS

Figure 17-1 shows the block diagram of the MSSP module when operating in SPI mode.





17.4.3.2 Reception

When the R/\overline{W} bit of the address byte is clear and an address match occurs, the R/\overline{W} bit of the SSPSTAT register is cleared. The received address is loaded into the SSPBUF register and the SDA line is held low (ACK).

When the address byte overflow condition exists, then the no Acknowledge (ACK) pulse is given. An overflow condition is defined as either bit, BF (SSPSTAT<0>), is set, or bit, SSPOV (SSPCON1<6>), is set.

An MSSP interrupt is generated for each data transfer byte. Flag bit, SSPIF (PIR1<3>), must be cleared in software. The SSPSTAT register is used to determine the status of the byte.

If SEN is enabled (SSPCON2<0> = 1), RC3/SCK/SCL will be held low (clock stretch) following each data transfer. The clock must be released by setting bit, CKP (SSPCON<4>). See **Section 17.4.4** "**Clock Stretching**" for more details.

17.4.3.3 Transmission

When the R/W bit of the incoming address byte is set and an address match occurs, the R/W bit of the SSPSTAT register is set. The received address is loaded into the SSPBUF register. The ACK pulse will be sent on the ninth bit and the RC3/SCK/SCL pin is held low regardless of SEN (see Section 17.4.4 "Clock Stretching" for more detail). By stretching the clock, the master will be unable to assert another clock pulse until the slave is done preparing the transmit data. The transmit data must be loaded into the SSPBUF register which also loads the SSPSR register. Then the RC3/SCK/SCL pin should be enabled by setting bit, CKP (SSPCON1<4>). The eight data bits are shifted out on the falling edge of the SCL input. This ensures that the SDA signal is valid during the SCL high time (Figure 17-9).

The ACK pulse from the master-receiver is latched on the rising edge of the ninth SCL input pulse. If the SDA line is high (not ACK), then the data transfer is complete. In this case, when the ACK is latched by the slave, the slave logic is reset (resets SSPSTAT register) and the slave monitors for another occurrence of the Start bit. If the SDA line was low (ACK), the next transmit data must be loaded into the SSPBUF register. Again, the RC3/SCK/SCL pin must be enabled by setting bit, CKP.

An MSSP interrupt is generated for each data transfer byte. The SSPIF bit must be cleared in software and the SSPSTAT register is used to determine the status of the byte. The SSPIF bit is set on the falling edge of the ninth clock pulse.

17.4.10 I²C MASTER MODE TRANSMISSION

Transmission of a data byte, a 7-bit address or the other half of a 10-bit address is accomplished by simply writing a value to the SSPBUF register. This action will set the Buffer Full flag bit, BF, and allow the Baud Rate Generator to begin counting and start the next transmission. Each bit of address/data will be shifted out onto the SDA pin after the falling edge of SCL is asserted (see data hold time specification parameter 106). SCL is held low for one Baud Rate Generator rollover count (TBRG). Data should be valid before SCL is released high (see data setup time specification parameter 107). When the SCL pin is released high, it is held that way for TBRG. The data on the SDA pin must remain stable for that duration and some hold time after the next falling edge of SCL. After the eighth bit is shifted out (the falling edge of the eighth clock), the BF flag is cleared and the master releases SDA. This allows the slave device being addressed to respond with an ACK bit during the ninth bit time if an address match occurred, or if data was received properly. The status of ACK is written into the ACKDT bit on the falling edge of the ninth clock. If the master receives an Acknowledge, the Acknowledge Status bit, ACKSTAT, is cleared. If not, the bit is set. After the ninth clock, the SSPIF bit is set and the master clock (Baud Rate Generator) is suspended until the next data byte is loaded into the SSPBUF, leaving SCL low and SDA unchanged (Figure 17-21).

After the write to the SSPBUF, each bit of the address will be shifted out on the falling edge of SCL until all seven address bits and the R/W bit are completed. On the falling edge of the eighth clock, the master will deassert the SDA pin, allowing the slave to respond with an Acknowledge. On the falling edge of the ninth clock, the master will sample the SDA pin to see if the address was recognized by a slave. The status of the ACK bit is loaded into the ACKSTAT status bit (SSPCON2<6>). Following the falling edge of the ninth clock transmission of the address, the SSPIF is set, the BF flag is cleared and the Baud Rate Generator is turned off until another write to the SSPBUF takes place, holding SCL low and allowing SDA to float.

17.4.10.1 BF Status Flag

In Transmit mode, the BF bit (SSPSTAT<0>) is set when the CPU writes to SSPBUF and is cleared when all 8 bits are shifted out.

17.4.10.2 WCOL Status Flag

If the user writes the SSPBUF when a transmit is already in progress (i.e., SSPSR is still shifting out a data byte), the WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

WCOL must be cleared in software.

17.4.10.3 ACKSTAT Status Flag

In Transmit mode, the ACKSTAT bit (SSPCON2<6>) is cleared when the slave has sent an Acknowledge $(\overline{ACK} = 0)$ and is set when the slave does not Acknowledge $(\overline{ACK} = 1)$. A slave sends an Acknowledge when it has recognized its address (including a general call), or when the slave has properly received its data.

17.4.11 I²C MASTER MODE RECEPTION

Master mode reception is enabled by programming the Receive Enable bit, RCEN (SSPCON2<3>).

Note: The MSSP module must be in an Idle state before the RCEN bit is set or the RCEN bit will be disregarded.

The Baud Rate Generator begins counting and on each rollover, the state of the SCL pin changes (high-to-low/ low-to-high) and data is shifted into the SSPSR. After the falling edge of the eighth clock, the receive enable flag is automatically cleared, the contents of the SSPSR are loaded into the SSPBUF, the BF flag bit is set, the SSPIF flag bit is set and the Baud Rate Generator is suspended from counting, holding SCL low. The MSSP is now in Idle state awaiting the next command. When the buffer is read by the CPU, the BF flag bit is automatically cleared. The user can then send an Acknowledge bit at the end of reception by setting the Acknowledge Sequence Enable bit, ACKEN (SSPCON2<4>).

17.4.11.1 BF Status Flag

In receive operation, the BF bit is set when an address or data byte is loaded into SSPBUF from SSPSR. It is cleared when the SSPBUF register is read.

17.4.11.2 SSPOV Status Flag

In receive operation, the SSPOV bit is set when 8 bits are received into the SSPSR and the BF flag bit is already set from a previous reception.

17.4.11.3 WCOL Status Flag

If the user writes the SSPBUF when a receive is already in progress (i.e., SSPSR is still shifting in a data byte), the WCOL bit is set and the contents of the buffer are unchanged (the write doesn't occur).



18.2.5 BREAK CHARACTER SEQUENCE

The EUSART module has the capability of sending the special Break character sequences that are required by the LIN bus standard. The Break character transmit consists of a Start bit, followed by twelve '0' bits and a Stop bit. The frame Break character is sent whenever the SENDB and TXEN bits (TXSTA<3> and TXSTA<5>) are set while the Transmit Shift register is loaded with data. Note that the value of data written to TXREG will be ignored and all '0's will be transmitted.

The SENDB bit is automatically reset by hardware after the corresponding Stop bit is sent. This allows the user to preload the transmit FIFO with the next transmit byte following the Break character (typically, the Sync character in the LIN specification).

Note that the data value written to the TXREG for the Break character is ignored. The write simply serves the purpose of initiating the proper sequence.

The TRMT bit indicates when the transmit operation is active or Idle, just as it does during normal transmission. See Figure 18-10 for the timing of the Break character sequence.

18.2.5.1 Break and Sync Transmit Sequence

The following sequence will send a message frame header made up of a Break, followed by an Auto-Baud Sync byte. This sequence is typical of a LIN bus master.

- Configure the EUSART for the desired mode. 1.
- 2. Set the TXEN and SENDB bits to set up the Break character.
- 3. Load the TXREG with a dummy character to initiate transmission (the value is ignored).
- Write '55h' to TXREG to load the Sync character 4. into the transmit FIFO buffer.
- After the Break has been sent, the SENDB bit is 5. reset by hardware. The Sync character now transmits in the preconfigured mode.

When the TXREG becomes empty, as indicated by the TXIF, the next data byte can be written to TXREG.

18.2.6 **RECEIVING A BREAK CHARACTER**

The Enhanced USART module can receive a Break character in two ways.

The first method forces configuration of the baud rate at a frequency of 9/13 the typical speed. This allows for the Stop bit transition to be at the correct sampling location (13 bits for Break versus Start bit and 8 data bits for typical data).

The second method uses the auto-wake-up feature described in Section 18.2.4 "Auto-Wake-up on Sync Break Character". By enabling this feature, the EUSART will sample the next two transitions on RX/DT, cause an RCIF interrupt and receive the next data byte followed by another interrupt.

Note that following a Break character, the user will typically want to enable the Auto-Baud Rate Detect feature. For both methods, the user can set the ABD bit once the TXIF interrupt is observed.



FIGURE 18-10: SEND BREAK CHARACTER SEQUENCE

19.1 A/D Acquisition Requirements

For the A/D Converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 19-3. The source impedance (Rs) and the internal sampling switch (Rss) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (Rss) impedance varies over the device voltage (VDD). The source impedance affects the offset voltage at the analog input (due to pin leakage current). The maximum recommended impedance for analog sources is 2.5 k Ω . After the analog input channel is selected (changed), the channel must be sampled for at least the minimum acquisition time before starting a conversion.

Note: When the conversion is started, the holding capacitor is disconnected from the input pin.

EQUATION 19-1: ACQUISITION TIME

TACQ = Amplifier Settling Time + Holding Capacitor Charging Time + Temperature Coefficient = TAMP + TC + TCOFF

EQUATION 19-2: A/D MINIMUM CHARGING TIME

VHOLD	=	$(\text{VREF} - (\text{VREF}/2048)) \bullet (1 - e^{(-\text{TC/CHOLD}(\text{Ric} + \text{Rss} + \text{Rs}))})$
or		
TC	=	-(CHOLD)(RIC + RSS + RS) ln(1/2048)

EQUATION 19-3: CALCULATING THE MINIMUM REQUIRED ACQUISITION TIME

TACQ	=	TAMP + TC + TCOFF
TAMP	=	0.2 μs
TCOFF	=	(Temp – 25°C)(0.02 μs/°C) (85°C – 25°C)(0.02 μs/°C) 1.2 μs
Tempera	ture c	befficient is only required for temperatures > 25°C. Below 25°C, TCOFF = 0 μ s.
ТС	=	-(Chold)(Ric + Rss + Rs) $\ln(1/2047) \ \mu s$ -(25 pF) (1 k Ω + 2 k Ω + 2.5 k Ω) ln(0.0004883) μs 1.05 μs
TACQ	=	$0.2 \ \mu s + 1 \ \mu s + 1.2 \ \mu s$ 2.4 \ \ \ \ \ \ \ \ s

To calculate the minimum acquisition time, Equation 19-1 may be used. This equation assumes that 1/2 LSb error is used (1024 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified resolution.

Example 19-3 shows the calculation of the minimum required acquisition time TACQ. This calculation is based on the following application system assumptions:

CHOLD	=	25 pF
Rs	=	2.5 kΩ
Conversion Error	\leq	1/2 LSb
Vdd	=	$5V ightarrow Rss$ = 2 k Ω
Temperature	=	85°C (system max.)

19.8 Use of the CCP2 Trigger

An A/D conversion can be started by the Special Event Trigger of the CCP2 module. This requires that the CCP2M<3:0> bits (CCP2CON<3:0>) be programmed as '1011' and that the A/D module is enabled (ADON bit is set). When the trigger occurs, the GO/DONE bit will be set, starting the A/D acquisition and conversion, and the Timer1 (or Timer3) counter will be reset to zero. Timer1 (or Timer3) is reset to automatically repeat the A/D acquisition period with minimal software overhead (moving ADRESH:ADRESL to the desired location). The appropriate analog input channel must be selected and the minimum acquisition period is either timed by the user, or an appropriate TACQ time is selected before the Special Event Trigger sets the GO/DONE bit (starts a conversion).

If the A/D module is not enabled (ADON is cleared), the Special Event Trigger will be ignored by the A/D module, but will still reset the Timer1 (or Timer3) counter.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page	
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	49	
PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	52	
PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	52	
IPR1	PSPIP ⁽¹⁾	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	52	
PIR2	OSCFIF	CMIF	—	EEIF	BCLIF	HLVDIF	TMR3IF	CCP2IF	52	
PIE2	OSCFIE	CMIE	—	EEIE	BCLIE	HLVDIE	TMR3IE	CCP2IE	52	
IPR2	OSCFIP	CMIP	—	EEIP	BCLIP	HLVDIP	TMR3IP	CCP2IP	52	
ADRESH	A/D Result Register High Byte									
ADRESL	A/D Result	Register Lo	w Byte						51	
ADCON0	_	_	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON	51	
ADCON1	_	_	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	51	
ADCON2	ADFM		ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0	51	
PORTA	RA7 ⁽²⁾	RA6 ⁽²⁾	RA5	RA4	RA3	RA2	RA1	RA0	52	
TRISA	TRISA7(2)	TRISA6 ⁽²⁾	PORTA Da	ita Direction F	Register				52	
PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	52	
TRISB	PORTB Dat	ta Direction F	Register						52	
LATB	PORTB Dat	ta Latch Reg	ister (Read	and Write to	Data Latch)			52	
PORTE ⁽⁴⁾	_	_	_		RE3 ⁽³⁾	RE2	RE1	RE0	52	
TRISE ⁽⁴⁾	IBF	OBF	IBOV	PSPMODE		TRISE2	TRISE1	TRISE0	52	
LATE ⁽⁴⁾	_		_	_		PORTE Da	ata Latch Re	gister	52	

TABI F 19-2	REGISTERS ASSOCIATED WITH A/D OPERATION

Legend: — = unimplemented, read as '0'. Shaded cells are not used for A/D conversion.

Note 1: These bits are unimplemented on 28-pin devices; always maintain these bits clear.

2: PORTA<7:6> and their direction bits are individually configured as port pins based on various primary oscillator modes. When disabled, these bits read as '0'.

3: RE3 port bit is available only as an input pin when the MCLRE Configuration bit is '0'.

4: These registers are not implemented on 28-pin devices.

ANDWF	AND W with f		BC		Branch if Carry						
Syntax:	ANDWF	ANDWF f {,d {,a}}		Synta	ix:	BC n					
Operands:	$0 \le f \le 255$		Ope		ands:	$-128 \le n \le 127$					
	d ∈ [0,1] a ∈ [0,1]			Oper	Operation:		if Carry bit is '1', (PC) + 2 + 2n \rightarrow PC				
Operation: (W) .AND. (f) \rightarrow dest Statu		Status Affected: None									
Status Affected:	Affected: N, Z		Enco	ding:	1110	0010	nnnn	nnnn			
Encoding: Description:	0001 The conten register 'f. I in W. If 'd' is in register ' If 'a' is '0', t If 'a' is '1', t GPR bank If 'a' is '0' a set is enabl in Indexed mode wher Section 24 Bit-Oriented	000101daffffffff.e contents of W are ANDed with gister 'f'. If 'd' is '0', the result is storedW. If 'd' is '1', the result is stored back register 'f' (default).a' is '0', the Access Bank is selected. a' is '1', the BSR is used to select the PR bank (default).a' is '0' and the extended instruction t is enabled, this instruction operates Indexed Literal Offset Addressing ode whenever $f \le 95$ (5Fh). See ection 24.2.3 "Byte-Oriented and t-Oriented Instructions in Indexed		Desc Word Cycle Q C If Ju	ription: s: es: ycle Activity: mp: Q1	If the Carry bit is '1', then the provide the provide the carry bit is '1', then the provide the providet the provide the providet the p			program 2n' is 2 will have vill be s then a Q4		
Words:	1		uctans.		Decode	Read literal	Process Data	s Wr	Write to PC		
Cycles:	1				No	No	No		No		
Q Cycle Activity:				If No	operation	operation	operation	n o	peration		
Q1	Q2	Q3	Q4		Q1	Q2	Q3		Q4		
Decode	Read register 'f'	Process Data	Write to destination		Decode	Read literal 'n'	Process Data	3 0	No peration		
Example: Before Instrue	ANDWF	REG, 0, 0		Exan	<u>iple:</u> Refere Instru	HERE	BC 5				
W REG After Instructi W REG	= 17h = C2h on = 02h = C2h				PC PC After Instructi If Carry PC If Carry PC	= ac on = 1; = ac = 0; = ac	Idress (HE Idress (HE Idress (HE	RE) RE + 1 RE + 2	12) 2)		

SUBWFB	Subtract W from f with Borrow						
Syntax:	S	JBWFB	f {,d {,a	a}}			
Operands:	0 : d a	≤ f ≤ 255 ∈ [0,1] ∈ [0,1]					
Operation:	(f)	– (W) –	$(\overline{C}) \rightarrow de$	st			
Status Affected:	N, OV, C, DC, Z						
Encoding:	Г	0101	10da	fff	f ffff		
Description:	n: Subtract W and the Carry flag (borrow) from register 'f' (2's complement method). If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f' (default). If 'a' is '0', the Access Bank is selected. If 'a' is '0', the BSR is used to select the GPR bank (default). If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See Section 24.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed						
Wordo	Li 1	teral Off	set Mode	e" for c	letails.		
Cycles:	1						
	1						
		02	0'	3	04		
Decode		Read	Proc	ess	Write to		
	re	gister 'f'	Dat	ta	destination		
Example 1:	:	SUBWFB	REG, 1	L, 0			
Before Instruc	tion	104	(
REG W C	= = =	0Dh 1	(000)	1 100 0 110)1))1)		
After Instructio REG W C Z	n = = =	1 = OCh (0000 1011) = ODh (0000 1101) = 1 = 0					
IN Example 2:	-		, lesu		ISILIVE		
Refore Instruct	, tion	SUBWFB	REG, U	, 0			
REG W C	= = =	1Bh 1Ah 0	(000 (000	1 101 1 101	.1) .0)		
After Instructic REG W	n = =	1Bh 00h 1	(000	1 101	.1)		
Z N	=	= 1 ; result is zero = 0			ro		
Example 3:	3	SUBWFB	REG, 1	L, O			
Before Instruc REG W C	tion = = =	03h 0Eh 1	(000 (000	0 001 0 110	.1))1)		
Aπer Instructio REG W	n = =	F5h 0Eh	(111 ; [2's (000	1 010 comp] 0 110	00) 01)		
C Z N	= = =	0 0 1	; resu	lt is ne	egative		

SWAPF	Swap f							
Syntax:	SWAPF f	SWAPF f {,d {,a}}						
Operands:	$0 \le f \le 255$ $d \in [0,1]$ $a \in [0,1]$	$0 \le f \le 255$ $d \in [0,1]$ $a \in [0,1]$						
Operation:	$(f<3:0>) \rightarrow$ $(f<7:4>) \rightarrow$	$(f<3:0>) \rightarrow dest<7:4>,$ $(f<7:4>) \rightarrow dest<3:0>$						
Status Affected:	None							
Encoding:	0011	10da	ffff	ffff				
Description:	The upper a 'f' are excha- is placed in re- lf 'a' is '0', t If 'a' is '1', t GPR bank If 'a' is '0' a set is enabl in Indexed mode wher Section 24 Bit-Oriente Literal Offs	The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed in register 'f' (default). If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default). If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See Section 24.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode" for dotails						
Words:	1							
Cycles:	1							
Q Cycle Activity:								
Q1	Q2	Q3		Q4				
Decode	Read register 'f'	Proce Data	ess V a de	Vrite to stination				
Example: SWAPF REG, 1, 0 Before Instruction REG = 53h After Instruction REG = 35h								

26.2 DC Characteristics: Power-Down and Supply Current PIC18F2420/2520/4420/4520 (Industrial) PIC18LF2420/2520/4420/4520 (Industrial) (Continued)

PIC18LF2420/2520/4420/4520 (Industrial)		Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial							
PIC18F2420/2520/4420/4520 (Industrial, Extended)		Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended							
Param No.	Device	Тур	Max	Units	Conditions				
	Module Differential Currer	nts (∆lw	DT, Δ IBC	dr, ∆Ilv	D, Δ IOSCB, Δ IAD)				
D026	A/D Converter	0.2	1.0	μΑ	-40°C to +85°C	VDD = 2.0V			
(ΔAD)		0.2	1.0	μΑ	-40°C to +85°C	VDD = 3.0V	A/D on not converting		
		0.2	1.0	μΑ	-40°C to +85°C		A/D on, not converting		
		0.5	4.0	μΑ	-40°C to +125°C	VDD - 5.0V			
D022	Watchdog Timer	1.3	2.2	μΑ	-40°C				
(∆lwdt)		1.4	2.2	μΑ	+25°C	VDD = 2.0V			
		1.6	2.3	μΑ	+85°C				
		1.9	3.5	μΑ	-40°C				
		2.0	3.5	μΑ	+25°C	VDD = 3.0V			
		2.2	3.5	μΑ	+85°C				
		3.0	7.5	μA	-40°C				
		3.5	7.5	μΑ	+25°C				
		3.5	7.8	μΑ	+85°C	VDD = 5.0V			
		4.0	10	μΑ	+125°C				
D022A	Brown-out Reset ⁽⁴⁾	35	50	μA	-40°C to +85°C	VDD = 3.0V			
(Δ IBOR)		40	55	μΑ	-40°C to +85°C				
		55	65	μΑ	-40°C to +125°C				
		0	2	μΑ	-40°C to +85°C	VDD = 5.0V	Sleep mode,		
		0	5	μΑ	-40°C to +125°C		BOREN<1:0> = 10		
D022B	High/Low-Voltage	22	38	μΑ	-40°C to +85°C	VDD = 2.0V			
(∆ILVD)	Detect ⁽⁴⁾	25	40	μΑ	-40°C to +85°C	VDD = 3.0V			
		29	45	μΑ	-40°C to +85°C				
		30	45	μΑ	-40°C to +125°C	vDD = 5.0V			

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSs and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD or Vss;

MCLR = VDD; WDT enabled/disabled as specified.

- **3:** When operation below -10°C is expected, use T1OSC High-Power mode, where LPT1OSC (CONFIG3H<2>) = 0. When operation will always be above -10°C, then the low-power Timer1 oscillator may be selected.
- 4: BOR and HLVD enable internal band gap reference. With both modules enabled, current consumption will be less than the sum of both specifications.

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial					
Param No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
		Data EEPROM Memory					
D120	ED	Byte Endurance	100K	1M		E/W	-40°C to +85°C
D121	Vdrw	VDD for Read/Write	VMIN	_	5.5	V	Using EECON to read/write VMIN = Minimum operating voltage
D122	TDEW	Erase/Write Cycle Time	—	4		ms	
D123	TRETD	Characteristic Retention	40	_	—	Year	Provided no other specifications are violated
D124	TREF	Number of Total Erase/Write Cycles before Refresh ⁽¹⁾	1M	10M	—	E/W	-40°C to +85°C
D125	Iddp	Supply Current during Programming	-	10	—	mA	
		Program Flash Memory					
D130	Eр	Cell Endurance	10K	100K	—	E/W	-40°C to +85°C
D131	Vpr	VDD for Read	VMIN	_	5.5	V	Vмın = Minimum operating voltage
D132	VIE	VDD for Block Erase	3.0	—	5.5	V	Using ICSP™ port, +25°C
D132A	Viw	VDD for Externally Timed Erase or Write	4.5	—	5.5	V	Using ICSP™ port, +25°C
D132B	VPEW	VDD for Self-Timed Write	VMIN	—	5.5	V	Vмın = Minimum operating voltage
D133	TIE	ICSP Block Erase Cycle Time	_	4		ms	$VDD \ge 4.5V$
D133A	Tiw	ICSP Erase or Write Cycle Time (externally timed)	1	_	—	ms	VDD ≥ 4.5V, +25°C
D133A	Tiw	Self-Timed Write Cycle Time		2		ms	
D134	TRETD	Characteristic Retention	40	100	_	Year	Provided no other specifications are violated
D135	IDDP	Supply Current during Programming	—	10	—	mA	

TABLE 26-1: MEMORY PROGRAMMING REQUIREMENTS

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Refer to **Section 7.8 "Using the Data EEPROM**" for a more detailed discussion on data EEPROM endurance.



Param. No.	Symbol	Characteristic			Max	Units	Conditions
62	TdtV2wrH	Data In Valid before $\overline{WR} \uparrow$ or $\overline{CS} \uparrow$ (setup time)				ns	
63	TwrH2dtl	WR ↑ or CS ↑ to Data–In	PIC18FXXXX	20	_	ns	
		Invalid (hold time)	PIC18 LF XXXX	35	_	ns	VDD = 2.0V
64	TrdL2dtV	$\overline{RD}\downarrow$ and $\overline{CS}\downarrow$ to Data–Out Valid			80	ns	
65	TrdH2dtl	\overline{RD} \uparrow or \overline{CS} \downarrow to Data–Out Invalid			30	ns	
66	TibfINH	Inhibit of the IBF Flag bit being Cleared from $\overline{\rm WR}\uparrow$ or $\overline{\rm CS}\uparrow$			3 TCY		





