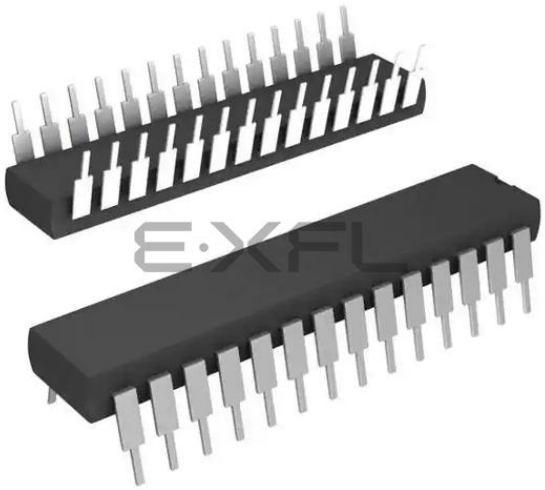

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | Z8 |
| Core Size | 8-Bit |
| Speed | 12MHz |
| Connectivity | EBI/EMI |
| Peripherals | POR, WDT |
| Number of I/O | 24 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 237 x 8 |
| Voltage - Supply (Vcc/Vdd) | 3.5V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 28-DIP (0.600", 15.24mm) |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z8673312psg |

- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive

## Functional Block Diagram

Figure 1 displays the functional block diagram.

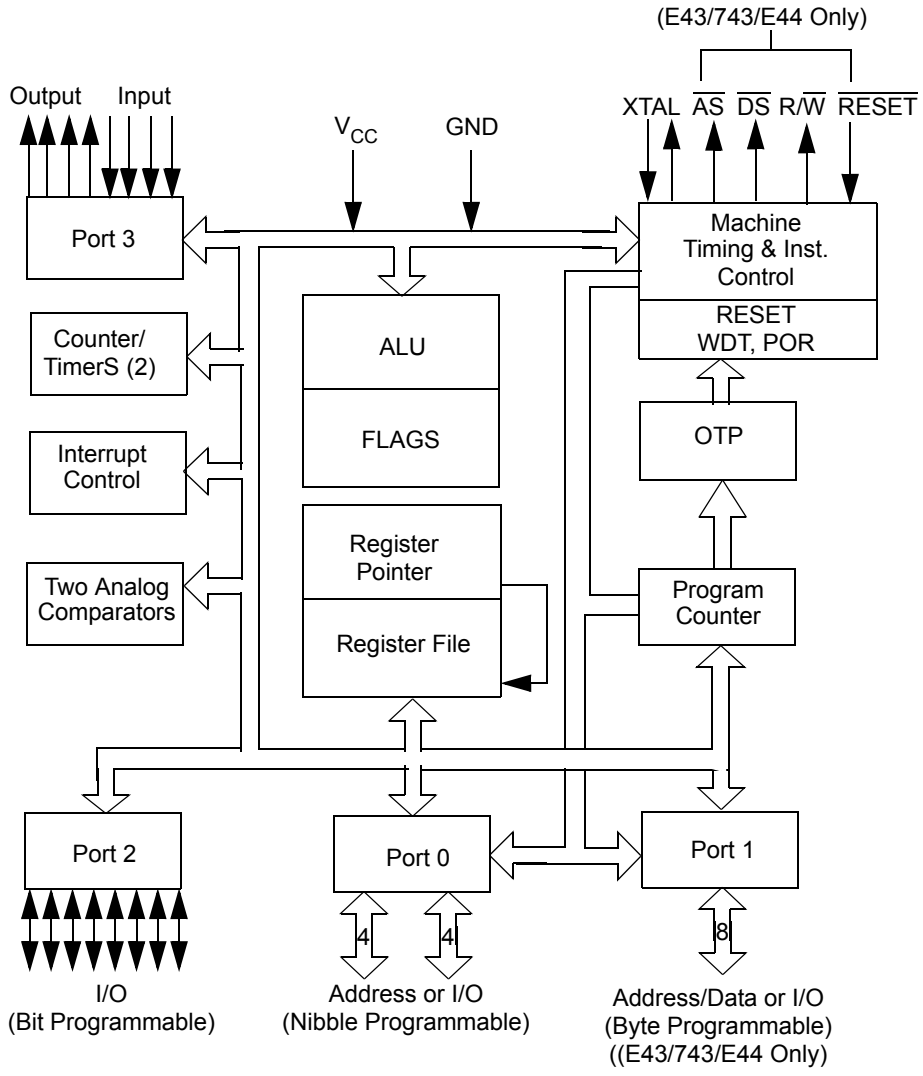



**Figure 1. Functional Block Diagram**

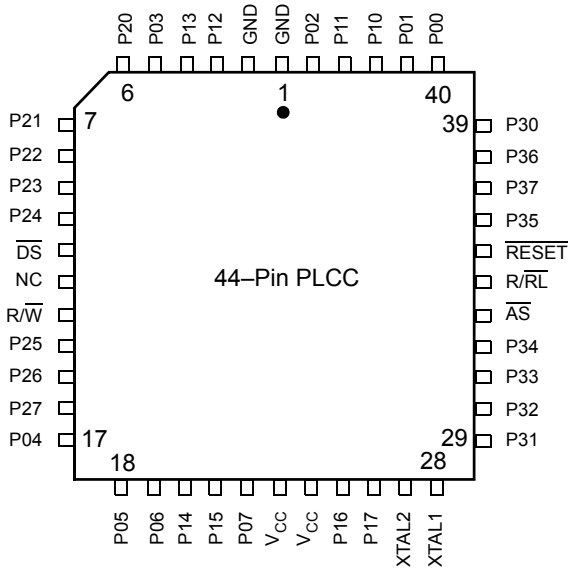



**Figure 4. 44-Pin PLCC Pin Configuration Standard Mode**

**Table 3. 44-Pin PLCC Pin Identification**

| Pin No | Symbol | Function | Direction |
|---|---|---|---|
| 1-2 | GND | Ground | |
| 3-4 | P12-P13 | Port 1, Pins 2,3 | Input/Output |
| 5 | P03 | Port 0, Pin 3 | Input/Output |
| 6-10 | P20-P24 | Port 2, Pins 0,1,2,3,4 | Input/Output |
| 11 | DS | Data Strobe | Output |
| 12 | NC | No Connection | |
| 13 | R/$\overline{W}$ | Read/Write | Output |
| 14-16 | P25-P27 | Port 2, Pins 5,6,7 | Input/Output |
| 17-19 | P04-P06 | Port 0, Pins 4,5,6 | Input/Output |
| 20-21 | P14-P15 | Port 1, Pins 4,5 | Input/Output |
| 22 | P07 | Port 0, Pin 7 | Input/Output |
| 23-24 | $V_{CC}$ | Power Supply | |
| 25-26 | P16-P17 | Port 1, Pins 6,7 | Input/Output |

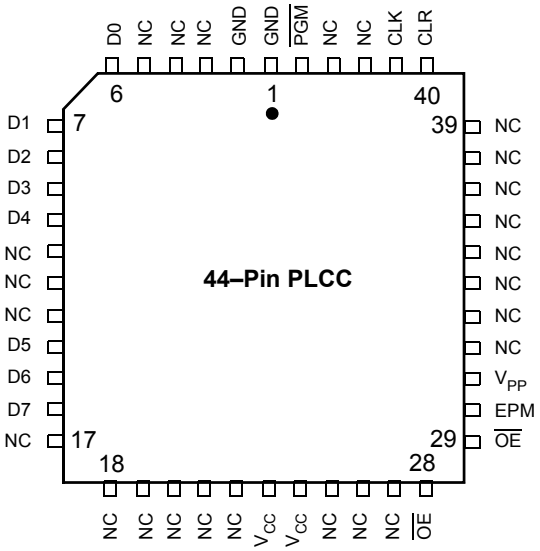



**Figure 7. 44-Pin PLCC Pin Configuration EPROM Programming Mode**

**Table 6. 44-Pin PLCC Pin Configuration EPROM Programming Mode**

| Pin No | Symbol | Function | Direction |
|---|---|---|---|
| 1-2 | GND | Ground | |
| 3-5 | NC | No Connection | |
| 6-10 | D0-D4 | Data 0,1,2,3,4 | Input/Output |
| 11-13 | NC | No Connection | |
| 14-16 | D5-D7 | Data 5,6,7 | Input/Output |
| 17-22 | NC | No Connection | |
| 23-24 | $V_{CC}$ | Power Supply | |
| 25-27 | NC | No Connection | |
| 28 | CE | Chip Select | Input |
| 29 | OE | Output Enable | Input |
| 30 | EPM | EPROM Prog. Mode | Input |
| 31 | $V_{PP}$ | Prog. Voltage | Input |

**Table 6. 44-Pin PLCC Pin Configuration EPROM Programming Mode (Continued)**

| Pin No | Symbol | Function | Direction |
|---|---|---|---|
| 32-39 | NC | No Connection | |
| 40 | CLR | Clear | Input |
| 41 | CLK | Clock | Input |
| 42-43 | NC | No Connection | |
| 44 | /PGM | Prog. Mode | Input |

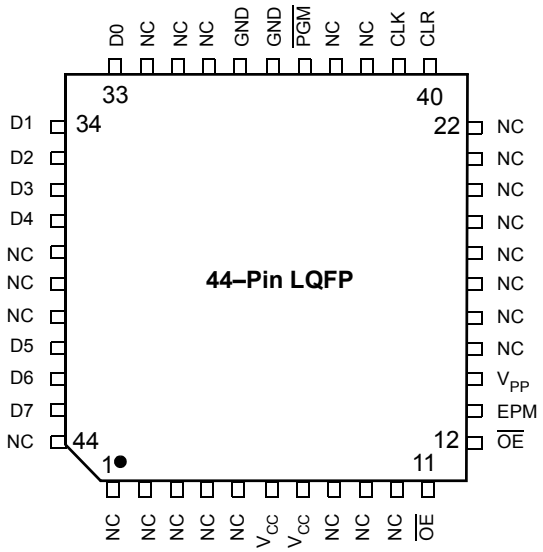



**Figure 8. 44-Pin LQFP Pin Configuration EPROM Programming Mode**

## Table 7. 44-Pin LQFP Pin Identification EPROM Programming Mode

| Pin No | Symbol | Function | Direction |
|---|---|---|---|
| 1-5 | NC | No Connection | |
| 6-7 | $V_{CC}$ | Power Supply | |
| 8-10 | NC | No Connection | |
| 11 | CE | Chip Select | Input |
| 12 | OE | Output Enable | Input |
| 13 | EPM | EPROM Prog. Mode | Input |
| 14 | $V_{PP}$ | Prog. Voltage | Input |
| 15-22 | NC | No Connection | |
| 23 | CLR | Clear | Input |
| 24 | CLK | Clock | Input |
| 25-26 | NC | No Connection | |
| 27 | /PGM | Prog. Mode | Input |
| 28-29 | GND | Ground | |
| 30-32 | NC | No Connection | |

# Electrical Characteristics

## Absolute Maximum Ratings

**Table 10. Absolute Maximum Ratings**

| Parameter | Min | Max | Units | Notes |
|---|---|---|---|---|
| Ambient Temperature under Bias | –40 | +105 | C | |
| Storage Temperature | –65 | +150 | C | |
| Voltage on any Pin with Respect to $V_{SS}$ | –0.6 | +7 | V | 1 |
| Voltage on $V_{DD}$ Pin with Respect to $V_{SS}$ | –0.3 | +7 | V | |
| Voltage on XTAL1, P32, P33 and $\overline{\text{RESET}}$ Pins with Respect to $V_{SS}$ | –0.6 | $V_{DD}$+1 | V | 2 |
| Total Power Dissipation | | 1.21 | W | |
| Maximum Allowable Current out of $V_{SS}$ | | 220 | mA | |
| Maximum Allowable Current into $V_{DD}$ | | 180 | mA | |
| Maximum Allowable Current into an Input Pin | –600 | +600 | µA | 3 |
| Maximum Allowable Current into an Open-Drain Pin | –600 | +600 | µA | 4 |
| Maximum Allowable Output Current Sunk by Any I/O Pin | | 25 | mA | |
| Maximum Allowable Output Current Sourced by Any I/O Pin | | 25 | mA | |
| Maximum Allowable Output Current Sunk by $\overline{\text{RESET}}$ Pin | | 3 | mA | |

**Notes**
1. This applies to all pins except XTAL pins and where otherwise noted.
2. There is no input protection diode from pin to $V_{DD}$.
3. This excludes XTAL pins.
4. Device pin is not at an output Low state.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Total power dissipation should not exceed 1.21 W for the package. Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{DD} \times [I_{DD} - (\text{sum of } I_{OH}), + \text{sum of } [(V_{DD} - V_{OH}) \times I_{OH}] + \text{sum of } (V_{OL} \times I_{OL})$$

## Standard Test Conditions

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Test Load).

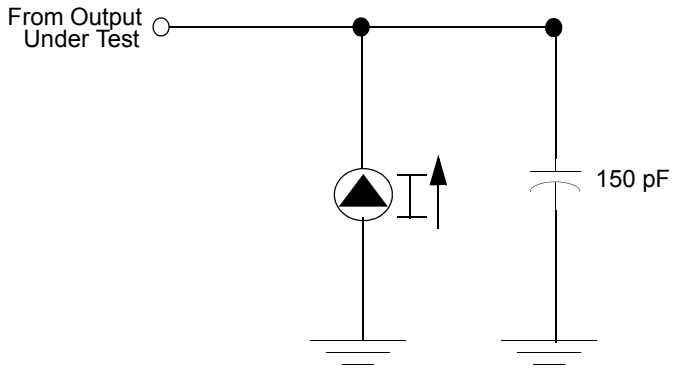



**Figure 13. Test Load Diagram**

## Capacitance

$T_A$ = 25 °C, $V_{CC}$ = GND = 0 V, f = 1.0 MHz, unmeasured pins returned to GND.

| Parameter | Min | Max |
|---|---|---|
| Input capacitance | 0 | 12 pF |
| Output capacitance | 0 | 12 pF |
| I/O capacitance | 0 | 12 pF |

**Table 12. DC Electrical Characteristics $T_A$= -40 °C to +105 °C (Continued)**

| Symbol | Parameter | $V_{CC}$ [1] | Min | Max | Typical @ 25°C | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| $V_{OH1}$ | Output High Voltage | 4.5V | $V_{CC}$ -0.4 | | 4.8 | V | $I_{OH}$ = -2.0 mA | 2 |
| | | 5.5V | $V_{CC}$ -0.4 | | 4.8 | V | $I_{OH}$ = -2.0 mA | 2 |
| $V_{OL}$ | Output Low Voltage Low EMI Mode | 4.5V | | 0.4 | 0.2 | V | $I_{OL}$ = 1.0 mA | |
| | | 5.5V | | 0.4 | 0.2 | V | $I_{OL}$ = 1.0 mA | |
| $V_{OL1}$ | Output Low Voltage | 4.5V | | 0.4 | 0.1 | V | $I_{OL}$ = +4.0 mA | 2 |
| | | 5.5V | | 0.4 | 0.1 | V | $I_{OL}$ = +4.0 mA | 2 |
| $V_{OL2}$ | Output Low Voltage | 4.5V | | 1.2 | 0.5 | V | $I_{OL}$ = +12 mA | 2 |
| | | 5.5V | | 1.2 | 0.5 | V | $I_{OL}$ = +12 mA | 2 |
| $V_{RH}$ | Reset Input High Voltage | 4.5V | .8 $V_{CC}$ | $V_{CC}$ | 1.7 | V | | 3 |
| | | 5.5V | .8 $V_{CC}$ | $V_{CC}$ | 2.1 | V | | 3 |
| $V_{OLR}$ | Reset Output Low Voltage | 4.5V | | 0.6 | 0.3 | V | $I_{OL}$ = 1.0 mA | 3 |
| | | 5.5V | | 0.6 | 0.2 | V | $I_{OL}$ = 1.0 mA | 3 |
| $V_{OFFSET}$ | Comparator Input Offset Voltage | 4.5V | | 25 | 10 | mV | | |
| | | 5.5V | | 25 | 10 | mV | | |
| $V_{ICR}$ | Input Common Mode Voltage Range | 4.5V | 0 | $V_{CC}$ -1.5V | | V | | 4 |
| | | 5.5V | 0 | $V_{CC}$ -1.5V | | V | | 4 |
| $I_{IL}$ | Input Leakage | 4.5V | -1 | 2 | <1 | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| | | 5.5V | -1 | 2 | <1 | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| $I_{OL}$ | Output Leakage | 4.5V | -1 | 2 | <1 | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| | | 5.5V | -1 | 2 | <1 | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| $I_{IR}$ | Reset Input Current | 4.5V | -18 | -180 | -112 | µA | | 3 |
| | | 5.5V | -18 | -180 | -112 | µA | | 3 |
| $I_{CC}$ | Supply Current | 4.5V | | 20 | 15 | mA | @ 12 MHz | 5,6 |
| | | 5.5V | | 20 | 15 | mA | @ 12 MHz | 5,6 |
| $I_{CC1}$ | Standby Current HALT Mode | 4.5V | | 6 | 2 | mA | $V_{IN}$ = 0V, $V_{CC}$ @ 12 MHz | 5,6 |
| | | 5.5V | | 6 | 4 | mA | $V_{IN}$ = 0V, $V_{CC}$ @ 12 MHz | 5,6 |

**Table 12. DC Electrical Characteristics $T_A$= -40 °C to +105 °C (Continued)**

| Symbol | Parameter | $V_{CC}$ [1] | Min | Max | Typical @ 25°C | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| $I_{CC2}$ | Standby Current STOP Mode | 4.5V | | 10 | 2 | µA | $V_{IN}$ = 0V, $V_{CC}$ | 7,8,9 |
| | | 5.5V | | 10 | 3 | µA | $V_{IN}$ = 0V, $V_{CC}$ | 7,8,9 |
| | | 4.5V | | 40 | 10 | µA | $V_{IN}$ = 0V, $V_{CC}$ | 7,8 |
| | | 5.5V | | 40 | 10 | µA | $V_{IN}$ = 0V, $V_{CC}$ | 7,8 |
| $I_{ALL}$ | Auto Latch Low Current | 4.5V | 1.4 | 20 | 4.7 | µA | 0V < $V_{IN}$ < $V_{CC}$ | 10 |
| | | 5.5V | 1.4 | 20 | 4.7 | µA | 0V < $V_{IN}$ < $V_{CC}$ | 10 |
| $I_{ALH}$ | Auto Latch High Current | 4.5V | -1.0 | -10 | -3.8 | µA | 0V < $V_{IN}$ < $V_{CC}$ | 10 |
| | | 5.5V | -1.0 | -10 | -3.8 | µA | 0V < $V_{IN}$ < $V_{CC}$ | 10 |
| $T_{POR}$ | Power-On Reset | 4.5V | 1.0 | 14 | 4 | ms | | |
| | | 5.5V | 1.0 | 14 | 4 | ms | | |
| $V_{LV}$ | Auto Reset Voltage | | 2.0 | 3.3 | 2.8 | V | | 11 |

**Notes**

1. The $V_{CC}$ voltage specification of 5.5 V guarantees 5.0 V ± 0.5 V and the $V_{CC}$ voltage specification of 3.5 V guarantees only 3.5 V.
2. STD Mode (not Low EMI Mode).
3. Z86E43/743/E44 only.
4. For analog comparator inputs when analog comparators are enabled.
5. All outputs unloaded, I/O pins floating, inputs at rail.
6. CL1=CL2=22 pF.
7. Same as note 5 except inputs at $V_{CC}$.
8. Clock must be forced Low, when XTAL1 is clock driven and XTAL2.
9. WDT is not running.
10. Auto Latch (mask option) selected.
11. Device does function down to the Auto Reset voltage.

**Table 13. DC Electrical Characteristics $T_A$ = 0 °C to +70 °C, 12 MHz (Continued)**

| No. | Symbol | Parameter | $V_{CC}$ [1] | Min | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| 4 | TwAS | $\overline{AS}$ Low Width | 3.5V | 55 | | ns | 2 |
| | | | 5.5V | 55 | | ns | 2 |
| 5 | TdAS(DS) | Address Float to $\overline{DS}$ Fall | 3.5V | 0 | | ns | |
| | | | 5.5V | 0 | | ns | |
| 6 | TwDSR | $\overline{DS}$ (Read) Low Width | 3.5V | 200 | | ns | 2,3 |
| | | | 5.5V | 200 | | ns | 2,3 |
| 7 | TwDSW | $\overline{DS}$ (Write) Low Width | 3.5V | 110 | | ns | 2,3 |
| | | | 5.5V | 110 | | ns | 2,3 |
| 8 | TdDSR(DR) | $\overline{DS}$ Fail to Read Data Req'd Valid | 3.5V | | 150 | ns | 2,3 |
| | | | 5.5V | | 150 | ns | 2,3 |
| 9 | ThDR(DS) | Read Data to $\overline{DS}$ Rise Hold Time | 3.5V | 0 | | ns | 2 |
| | | | 5.5V | 0 | | ns | 2 |
| 10 | TdDS(A) | $\overline{DS}$ Rise to Address Active Delay | 3.5V | 45 | | ns | 2 |
| | | | 5.5V | 55 | | ns | 2 |
| 11 | TdDS(AS) | $\overline{DS}$ Rise to $\overline{AS}$ Fall Delay | 3.5V | 30 | | ns | 2 |
| | | | 5.5V | 45 | | ns | 2 |
| 12 | TdR/W(AS) | R/$\overline{W}$ Valid to $\overline{AS}$ Rise Delay | 3.5V | 45 | | ns | 2 |
| | | | 5.5V | 45 | | ns | 2 |
| 13 | TdDS(R/W) | $\overline{DS}$ Rise to R/$\overline{W}$ Not Valid | 3.5V | 45 | | ns | 2 |
| | | | 5.5V | 45 | | ns | 2 |
| 14 | TdDW(DSW) | Write Data Valid to $\overline{DS}$ Fall (Write) Delay | 3.5V | 55 | | ns | 2 |
| | | | 5.5V | 55 | | ns | 2 |
| 15 | TdDS(DW) | $\overline{DS}$ Rise to Write Data Not Valid Delay | 3.5V | 45 | | ns | 2 |
| | | | 5.5V | 55 | | ns | 2 |
| 16 | TdA(DR) | Address Valid to Read Data Req'd Valid | 3.5V | | 310 | ns | 2,3 |
| | | | 5.5V | | 310 | ns | 2,3 |
| 17 | TdAS(DS) | $\overline{AS}$ Rise to $\overline{DS}$ Fall Delay | 3.5V | 65 | | ns | 2 |
| | | | 5.5V | 65 | | ns | 2 |

**Table 14. DC Electrical Characteristics $T_A$ = -40 °C to +105 °C, 12 MHz (Continued)**

| No. | Symbol | Parameter | $V_{CC}$[1] | Min | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| 10 | TdDS(A) | $\overline{DS}$ Rise to Address Active Delay | 4.5V | 45 | | ns | 2 |
| | | | 5.5V | 55 | | ns | 2 |
| 11 | TdDS(AS) | $\overline{DS}$ Rise to $\overline{AS}$ Fall Delay | 4.5V | 45 | | ns | 2 |
| | | | 5.5V | 45 | | ns | 2 |
| 12 | TdR/W(AS) | R/$\overline{W}$ Valid to $\overline{AS}$ Rise Delay | 4.5V | 45 | | ns | 2 |
| | | | 5.5V | 45 | | ns | 2 |
| 13 | TdDS(R/W) | $\overline{DS}$ Rise to R/$\overline{W}$ Not Valid | 4.5V | 45 | | ns | 2 |
| | | | 5.5V | 45 | | ns | 2 |
| 14 | TdDW(DSW) | Write Data Valid to $\overline{DS}$ Fall (Write) Delay | 4.5V | 55 | | ns | 2 |
| | | | 5.5V | 55 | | ns | 2 |
| 15 | TdDS(DW) | $\overline{DS}$ Rise to Write Data Not Valid Delay | 4.5V | 55 | | ns | 2 |
| | | | 5.5V | 55 | | ns | 2 |
| 16 | TdA(DR) | Address Valid to Read Data Req'd Valid | 4.5V | | 310 | ns | 2,3 |
| | | | 5.5V | | 310 | ns | 2,3 |
| 17 | TdAS(DS) | $\overline{AS}$ Rise to $\overline{DS}$ Fall Delay | 4.5V | 65 | | ns | 2 |
| | | | 5.5V | 65 | | ns | 2 |
| 18 | TdDM(AS) | $\overline{DM}$ Valid to $\overline{AS}$ Rise Delay | 4.5V | 35 | | ns | 2 |
| | | | 5.5V | 35 | | ns | 2 |
| 19 | ThDS(AS) | $\overline{DS}$ Valid to Address Valid Hold Time | 4.5V | 35 | | ns | 2 |
| | | | 5.5V | 35 | | ns | 2 |

**Notes**

1. The $V_{CC}$ voltage specification of 5.5 V guarantees 5.0 V ± 0.5 V and the $V_{CC}$ voltage specification of 3.5 V guarantees only 3.5 V.
2. Timing numbers given are for minimum TpC.
3. When using extended memory timing, add 2 TpC.

**Standard Test Load**

All timing references use 0.7 $V_{CC}$ for a logic 1 and 0.2 $V_{CC}$ for a logic 0.

For Standard Mode (not Low-EMI Mode for outputs) with SMR, D1 = 0, D0 = 0.

## Handshake Timing Diagrams

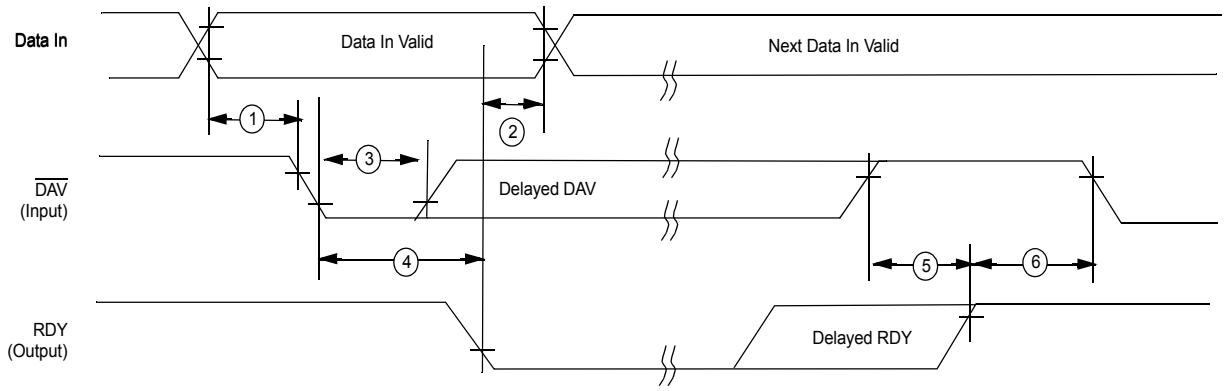



**Figure 16. Input Handshake Timing**

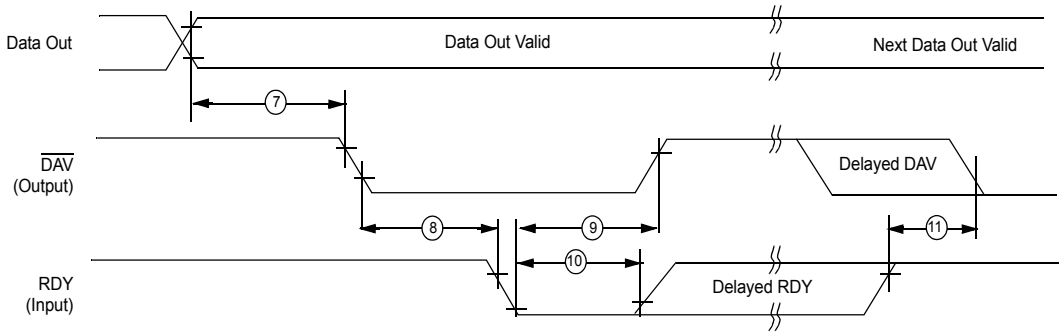



**Figure 17. Output Handshake Timing**

**Table 17. Additional Timing Table (Divide by Two Mode) $T_A$ = 0 °C to +70 °C**

| No | Symbol | Parameter | $V_{CC}$[1] | Min | Max | Min | Max | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | TpC | Input Clock Period | 3.5V | 62.5 | DC | 250 | DC | ns | | 2,6,4 |
| | | | 5.5V | 62.5 | DC | 250 | DC | ns | | 2,6,4 |
| 2 | TrC,TfC | Clock Input Rise & Fall Times | 3.5V | | 15 | | 25 | ns | | 2,6,4 |
| | | | 5.5V | | 15 | | 25 | ns | | 2,6,4 |
| 3 | TwC | Input Clock Width | 3.5V | 31 | | 31 | | ns | | 2,6,4 |
| | | | 5.5V | 31 | | 31 | | ns | | 2,6,4 |

**Table 18. Additional Timing Table (Divide by Two Mode) $T_A$ = -40 °C to +105 °C (Continued)**

| No | Symbol | Parameter | $V_{CC}$ [1] | Min | Max | Min | Max | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| 12 | Twdt | Watchdog Timer Delay Time Before Timeout | 3.5V | 7 | | 10 | | ms | D0 =0 | 8,9 |
| | | | 5.5V | 3.5 | | 5 | | ms | D1 = 0 | 5,11 |
| | | | 3.5V | 14 | | 20 | | ms | D0 =1 | 5,11 |
| | | | 5.5V | 7 | | 10 | | ms | D1 = 0 | 5,11 |
| | | | 3.5V | 28 | | 40 | | ms | D1 = 0 | 5,11 |
| | | | 5.5V | 14 | | 20 | | ms | D1 = 1 | 5,11 |
| | | | 3.5V | 112 | | 160 | | ms | D0 = 1 | 5,11 |
| | | | 5.5V | 56 | | 80 | | ms | D1 = 1 | 5,11 |

**Notes**
1. The $V_{CC}$ voltage specification of 5.5 V guarantees 5.0 V ± 0.5 V and the $V_{CC}$ voltage specification of 3.5 V guarantees only 3.5 V.
2. Timing Reference uses 0.7 VC0 for a logic 1 and 0.2 VGC for a logic 0.
3. SMR D1 = 0.
4. SMR-D5 = 1, POR STOP Mode Delay is on
5. Interrupt request via Port 3 (P31-P33)
6. Interrupt request via Port 3 (P30).
7. Maximum frequency for internal system clock is 2 MHz when using Low EMI OSC PCON Bit D7 = 0
8. Reg. WDTMR.
9. Using internal RC.

# Pin Functions

## EPROM Programming Mode

**D7-D0** Data Bus. The data can be read from or written to external memory through the data bus.

**$V_{CC}$** Power Supply. This pin must supply 5 V during the EPROM read mode and 6 V during other modes.

**$\overline{CE}$** Chip Enable (active Low). This pin is active during EPROM Read Mode, Program Mode, and Program Verify Mode.

**$\overline{OE}$** Output Enable (active Low). This pin drives the direction of the Data Bus. When this pin is Low, the Data Bus is output, when High, the Data Bus is input.

**EPM** EPROM Program Mode. This pin controls the different EPROM Program Mode by applying different voltages.

**$V_{PP}$** Program Voltage. This pin supplies the program voltage.

**PGM** Program Mode (active Low). When this pin is Low, the data is programmed to the EPROM through the Data Bus.

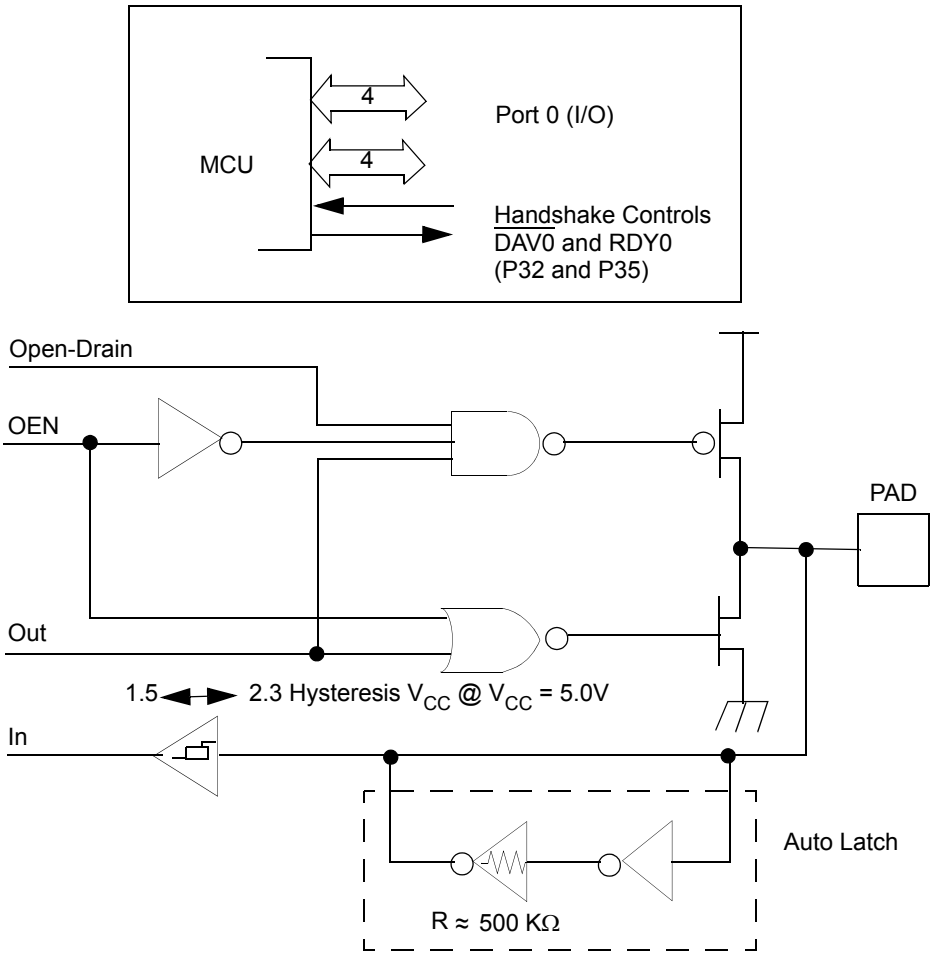



**Figure 18. Port 0 Configuration**

**Port 1 (P17-P10)**. Port 1 is an 8-bit, bidirectional, CMOS-compatible port with multiplexed Address (A7-A0) and Data (D7-D0) ports. These eight I/O lines can be programmed as inputs or outputs or can be configured under software control as an Address/Data port for interfacing external memory. The input buffers are Schmitt-triggered and the output buffers can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 1 can be placed under handshake control. In this configuration, Port 3, lines P33 and P34 are used as the handshake controls RDY1 and $\overline{\text{DAV1}}$ (Ready and Data Available). To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 outputs the additional lines (see Figure 19).

**Table 19. Port 3 Pin Assignments**

| Pin | I/O | CTC1 | Analog | Interrupt | P0 HS | P1 HS | P2 HS | Ext |
|---|---|---|---|---|---|---|---|---|
| P30 | IN | | | IRQ3 | | | | |
| P31 | IN | $T_{IN}$ | AN1 | IRQ2 | | D/R | | |
| P32 | IN | | AN2 | IRQ0 | D/R | | | |
| P33 | IN | | REF | IRQ1 | | D/R | | |
| P34 | OUT | | AN1-Out | | | R/D | | DM |
| P35 | OUT | | | | R/D | | | |
| P36 | OUT | $T_{OUT}$ | | | | R/D | | |
| P37 | OUT | | An2-Out | | | | | |

**Comparator Inputs**. Port 3, P31, and P32, each have a comparator front end. The comparator reference voltage P33 is common to both comparators. In analog mode, P31 and P32 are the positive input of the comparators and P33 is the reference voltage of the comparators.

**Auto Latch**. The Auto Latch puts valid CMOS levels on all CMOS inputs (except P33-P31) that are not externally driven. Whether this level is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer. Auto Latches are available on Port 0, Port 1, Port 2, and P30. There are no Auto Latches on P31, P32, and P33.

**Low EMI Emission**. The Z86E43/743/E44 can be programmed to operate in a low EMI Emission Mode in the PCON register. The oscillator and all I/O ports can be programmed as low EMI emission mode independently. Use of this feature results in:

- The pre-drivers slew rate reduced to 10 ns typical.
- Low EMI output drivers have resistance of 200 Ohms (typical).
- Low EMI Oscillator.
- Internal SCLK/TCLK= XTAL operation limited to a maximum of 4 MHz - 250 ns cycle time, when Low EMI Oscillator is selected.

**Note:** *For emulation only:*
*Do not set the emulator to emulate Port 1 in low EMI mode. Port 1 must always be configured in Standard Mode.*

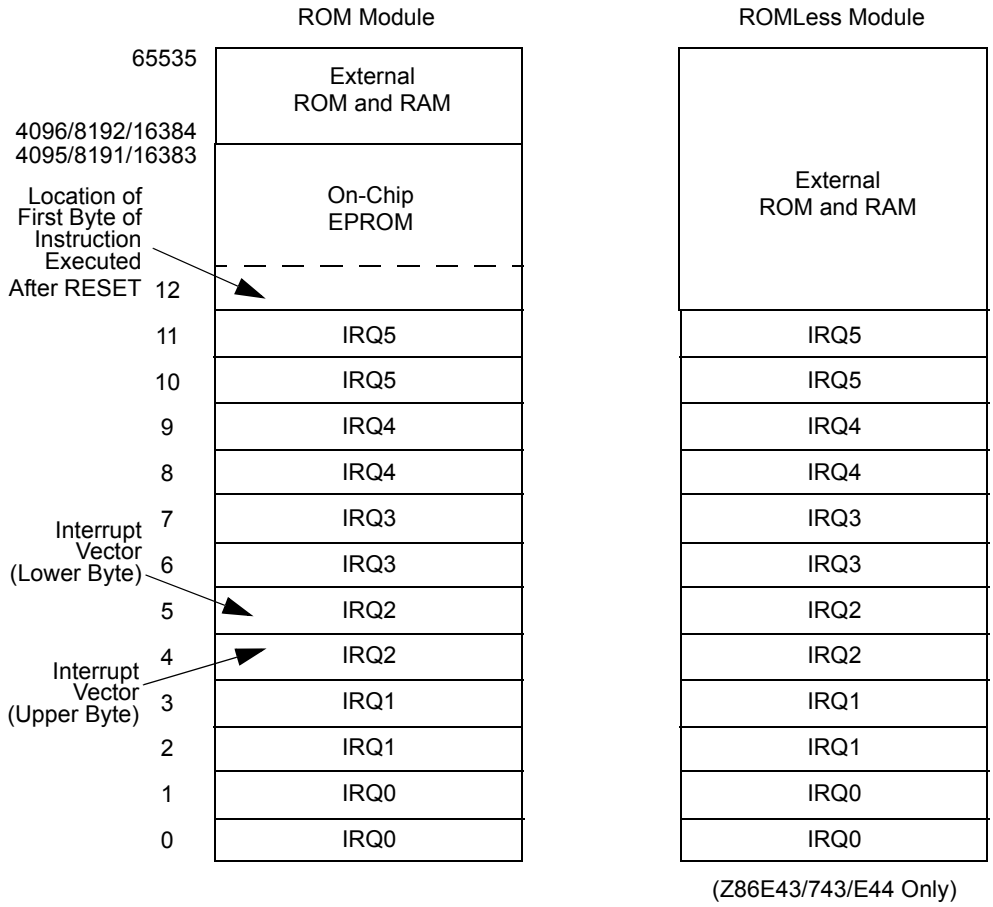



**Figure 22. Program Memory Map**

**EPROM Protect**. When in ROM Protect Mode, and executing out of External Program Memory, instructions LDC, LDCI, LDE, and LDEI cannot read Internal Program Memory.

When in EPROM Protect Mode and executing out of Internal Program Memory, instructions LDC, LDCI, LDE, and LDEI can read Internal Program Memory.

**Data Memory ($\overline{DM}$)**. In ROM Mode, the Z86E43/743/E44 can address up to 60156/48 KB of external data memory beginning at location 4096/8192/16384. In ROMless mode, the Z86E43/743/E44 can address up to 64 KB of data memory. External data memory may be included with, or separated from, the external program memory space. $\overline{DM}$, an optional I/0 function that can be programmed to appear on pin P34, is used to distinguish between data and program memory space (Figure 23). The state of the $\overline{DM}$ signal is controlled by the type of instruction being executed. An LDC opcode references PROGRAM ($\overline{DM}$ inactive) memory, and an LDE instruction references data ($\overline{DM}$ active Low) memory.

from STOP mode when programmed as analog inputs. When the Stop Mode Recovery sources are selected in this register then SMR2 register bits D0, D1 must be set to zero.

**Note:** *If the Port 2 pin is configured as an output, this output level will be read by the SMR circuitry.*

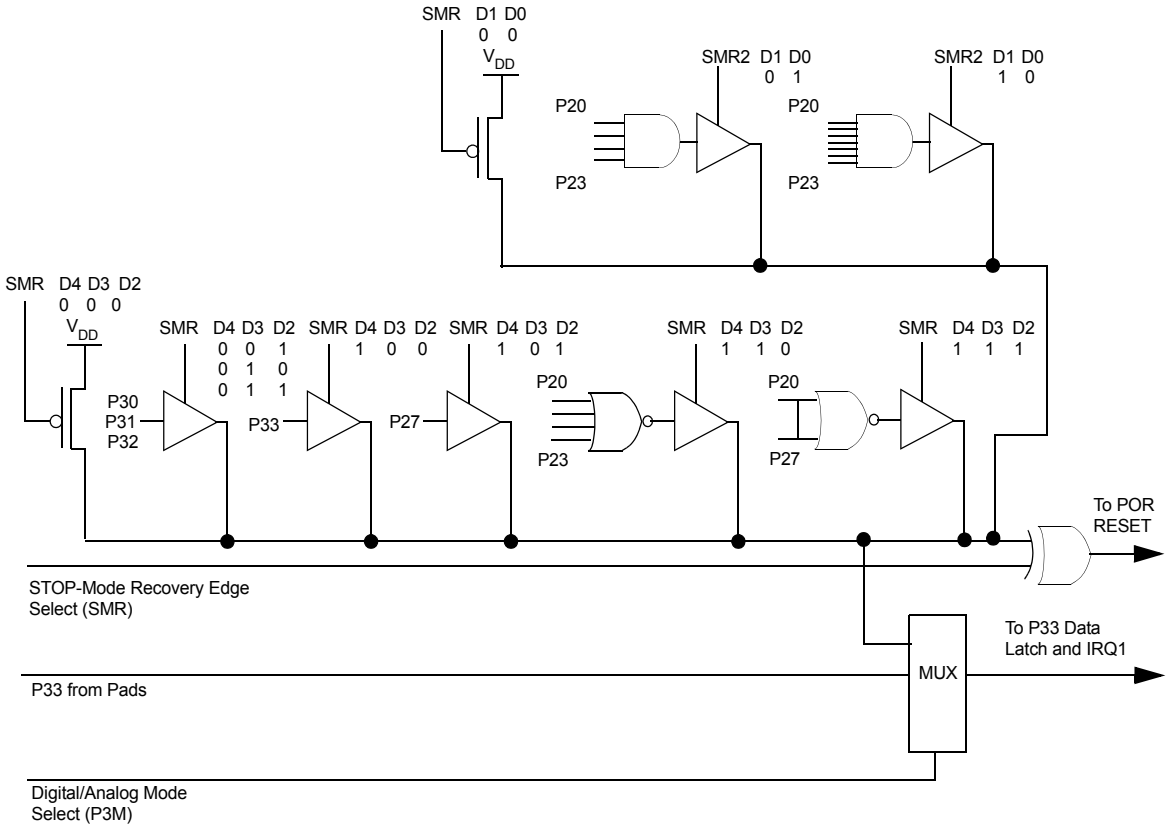



**Figure 32. Stop Mode Recovery Source**

**Note:** *WDT time-out in STOP Mode will not reset SMR,SMR2,PCON, WDTMR, P2M, P3M, Ports 2 & 3 Data Registers, but will activate the $T_{POR}$ delay.*

**WDTMR Register Accessibility**. The WDTMR register is accessible only during the first 60 internal system clock cycles from the execution of the first instruction after Power-On Reset, Watchdog reset or a Stop Mode Recovery (Figure 33 and Figure 34). After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register File at address location 0Fh.

**Clock Free WDT Reset**. The WDT will enable the Z8 to reset the I/0 pins whenever the WDT times out, even without a clock source running on the XTAL1 and XTAL2 pins. WDTMR Bit D4 must be 0 for the clock Free WDT to work. The I/O pins will default to their default settings.

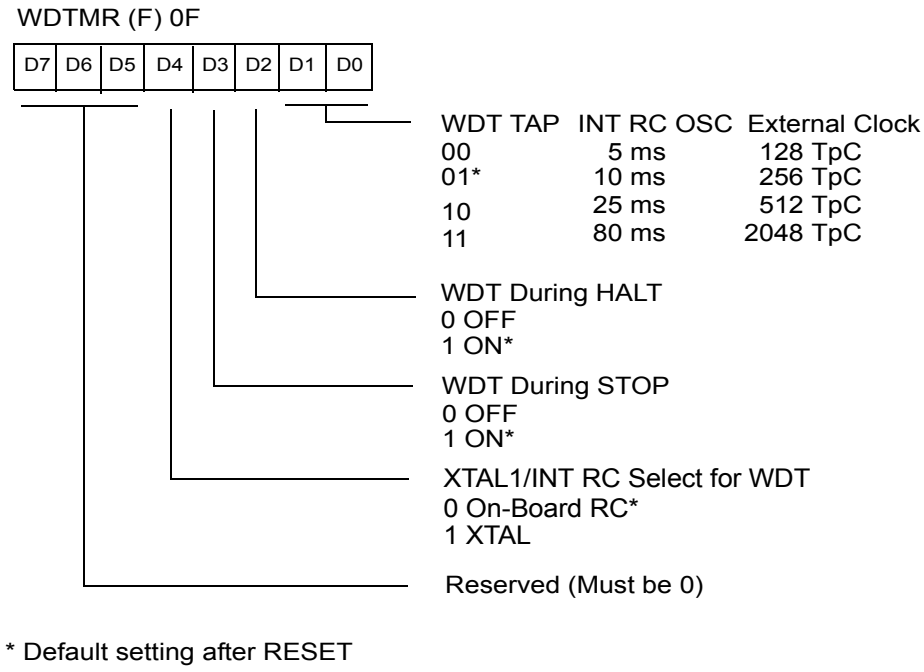
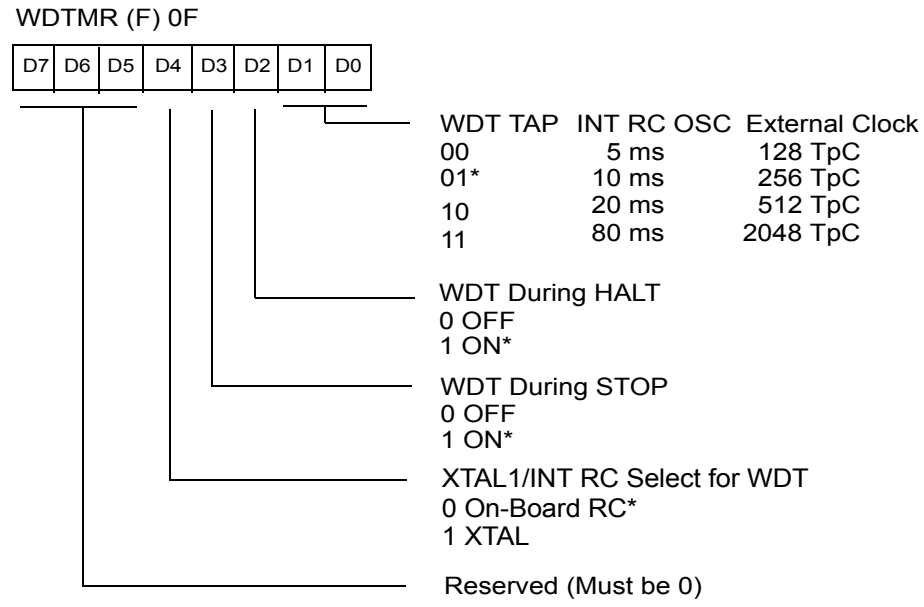
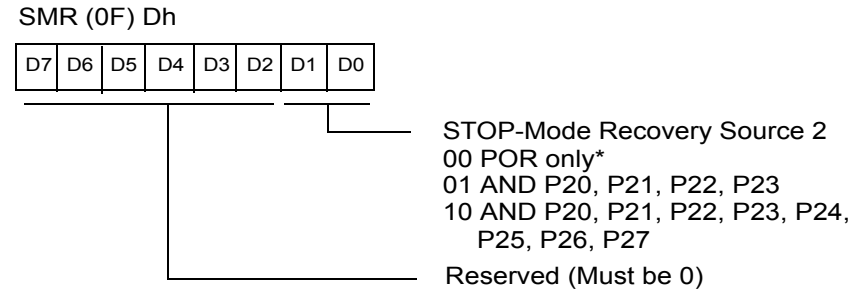



**Figure 33. Watchdog Timer Mode Register Write Only**




* Default setting after RESET

**Figure 38. Watchdog Timer Mode Register (Write Only)**




Note: Not used in conjunction with SMR Source

**Figure 39. Stop Mode Recovery Register2 (Write Only)**

# Customer Support

For answers to technical questions about the product, documentation, or any other issues with Zilog's offerings, please visit Zilog's Knowledge Base at http://www.zilog.com/kb.

For any comments, detail technical questions, or reporting problems, please visit Zilog's Technical Support at http://support.zilog.com.