Zilog - Z8674312ASG Datasheet





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Details

Product Status	Active
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	EBI/EMI
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8674312asg

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Revision History

Each instance in Revision History reflects a change to this document from its previous revision. For more details, refer to the corresponding pages and appropriate links in the table below.

Date	Revision Level	Description	Page No
May 2008	01	Original issue.	All

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Figure 2. EPROM Programming Block Diagram

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Pin No	Symbol	Function	Direction
15	XTAL1	Crystal Oscillator	Input
16-18	P31-P33	Port 3, Pins 1,2,3	Input
19	P34	Port 3, Pin 4	Output
20	AS	Address Strobe	Output
21	RESET	Reset	Input
22	P35	Port 3, Pin 5	Output
23	P37	Port 3, Pin 7	Output
24	P36	Port 3, Pin 6	Output
25	P30	Port 3, Pin 0	Input
26-27	P00-P01	Port 0, Pins 0,1	Input/Output
28-29	P10-P11	Port 1, Pins 0,1	Input/Output
30	P02	Port 0, Pin 2	Input/Output
31	GND	Ground	
32-33	P12-P13	Port 1, Pins 2,3	Input/Output
34	P03	Port 0, Pin 3	Input/Output
35-39	P20-P24	Port 2, Pins 0, 1,2,3,4	Input/Output
40	DS	Data Strobe	Output

Table 2. 40-Pin DIP Pin Identification Standard Mode (Continued)

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Pin No	Symbol	Function	Direction
27	XTAL2	Crystal Oscillator	Output
28	XTAL1	Crystal Oscillator	Input
29-31	P31-P33	Port 3, Pins 1,2,3	Input
32	P34	Port 3, Pin 4	Output
33	AS	Address Strobe	Output
34	R//RL	ROM/ROMless select Input	
35	RESET	Reset	Input
36	P35	Port 3, Pin 5	Output
37	P37	Port 3, Pin 7	Output
38	P36	Port 3, Pin 6	Output
39	P30	Port 3, Pin 0	Input
40-41	P00-P01	Port 0, Pins 0,1	Input/Output
42-43	P10-P11	Port 1, Pins 0,1	Input/Output
44	P02	Port 0, Pin 2	Input/Output

Table 3. 44-Pin PLCC Pin Identification (Continued)

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Table 7. 44-Pin LQFP Pin Identification EPROM Programming Mode (Continued)

Pin No	Symbol	Function	Direction
33-37	D0-D4	Data 0,1,2,3,4	Input/Output
38-40	NC	No Connection	
41-43	D5-D7	Data 5,6,7	Input/Output
44	NC	No Connection	

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Electrical Characteristics

Absolute Maximum Ratings

Table 10. Absolute Maximum Ratings

Min	Max	Units	Notes
-40	+105	С	
-65	+150	С	
-0.6	+7	V	1
-0.3	+7	V	
-0.6	V _{DD} +1	V	2
	1.21	W	
	220	mA	
	180	mA	
-600	+600	μA	3
-600	+600	μA	4
	25	mA	
	25	mA	
	3	mA	
	Min -40 -65 -0.6 -0.3 -0.6 -600 -600	MinMax -40 $+105$ -65 $+150$ -0.6 $+7$ -0.3 $+7$ -0.6 V_{DD} +1 1.21 220 180 180 -600 $+600$ -600 $+600$ 25 25 3	Min Max Units -40 +105 C -65 +150 C -0.6 +7 V -0.3 +7 V -0.6 V _{DD} +1 V -0.6 V _{DD} mA -600 +600 µA -600 25 mA 3 mA

Notes

1. This applies to all pins except XTAL pins and where otherwise noted.

2. There is no input protection diode from pin to V_{DD}.

3. This excludes XTAL pins.

4. Device pin is not at an output Low state.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

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DC Electrical Characteristics

Table 11. DC Electrical Characteristics $T_A = 0$ °C to +70 °C

Symbol	Parameter	V _{CC} ¹	Min	Мах	Typical @ 25°C	Units	Conditions	Notes
V _{CH}	Clock Input High Voltage	3.5V	0.7 V _{CC}	V _{CC} +0.3	1.8	V	Driven by	
		5.5V	0.7 V _{CC}	V _{CC} +0.3	2.5	V	External Clock Generator	
V _{CL}	Clock Input	3.5V	GND -0.3	0.2 V _{CC}	0.9	V	Driven by	
	Low Voltage	5.5V	GND -0.3	0.2 V _{CC}	1.5	V	External Clock Generator	
V _{IH}	Input High	3.5V	0.7 V _{CC}	V _{CC} +0.3	2.5	V		
	Voltage	5.5V	0.7 V _{CC}	V _{CC} +0.3	2.5	V		
V _{IL}	Input Low	3.5V	GND -0.3	0.2 V _{CC}	1.5	V		
	Voltage	5.5V	GND -0.3	0.2 V _{CC}	1.5	V		
V _{OH}	Output High Voltage Low EMI Mode	3.5V	V _{CC} -0.4		3.3		I _{OH} = -0.5 mA	
		5.5V	V _{CC} -0.4		4.8			
V _{OH1}	Output High Voltage	3.5V	V _{CC} -0.4		3.3	V	I _{OH} = -2.0 mA	
		5.5V	V _{CC} -0.4		4.8	V	I _{OH} = -2.0 mA	
V _{OL}	Output Low	3.5V		0.4	0.2	V	I _{OL} = 1.0 mA	
	Voltage Low EMI Mode	5.5V		0.4	0.2	V	I _{OL} = 1.0 mA	
V _{OL1}	Output Low Voltage	3.5V		0.4	0.1	V	I _{OL} = +4.0 mA	2
		5.5V		0.4	0.1	V	I _{OL} = +4.0 mA	2
V _{OL2}	Output Low	3.5V		1.2	0.5	V	I _{OL} = +10 mA	2
	Voltage	5.5V		1.2	0.5	V	I _{OL} = +10 mA	2
V _{RH}	Reset Input	3.5V	.8 V _{CC}	V _{CC}	1.7	V		3
	High Voltage	5.5V	.8 V _{CC}	V _{CC}	2.1	V		3
V _{RL}	Reset Input	3.5V	GND -0.3	0.2 V _{CC}	1.3	V		3
	Low Voltage	5.5V	GND -0.3	0.2 V _{CC}	1.7	V		3
V _{OLR}	Reset Output Low	3.5V		0.6	0.3	V	I _{OL} = 1.0 mA	3
	Voltage	5.5V		0.6	0.2	V	I _{OL} = 1.0 mA	3

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No	Symbol	Parameter	V _{CC} ¹	Min	Max	Min	Max	Units	Conditions	Notes
4	TwTinL	Timer Input Low Width	3.5V	70		70		ns		2,6,4
			5.5V	70		70		ns		2,6,4
5	TwTinH	Timer Input High	3.5V	5TpC		5TpC				2,6,4
		Width	5.5V	5TpC		5TpC				2,6,4
6	TpTin	Timer Input Period	3.5V	8TpC		8TpC				2,6,4
			5.5V	8TpC		8TpC				2,6,4
7	TrTin,	Timer Input Rise &	3.5V		100		100	ns		2,6,4
	TfTin	Fall Timer	5.5V		100		100	ns		2,6,4
8A	TwIL	Int. Request Low	3.5V	70		70		ns		2,6,4,5
		Time	5.5V	70		70		ns		2,6,4,5
8B	TwIL	Int. Request Low	3.5V	5TpC		5TpC				2,6,4,5
		Time	5.5V	5TpC		5TpC				2,6,4,5
9	TwlH	Int. Request Input High Time	3.5V	5TpC		5TpC				2,6,4,5
			5.5V	5TpC		5TpC				2,6,4,5
10	Twsm	Stop Mode Recovery Width Spec	3.5V	12		12		ns		6,7
			5.5V	12		12		ns		6,7
11	Tost	Oscillator Startup	3.5V		5TpC		5TpC			6,7
		Time	5.5V		5TpC		5TpC			6,7
12	Twdt	Watchdog Timer	3.5V	7		10		ms	D0 =0	8,9
		Delay Time Before Timeout	5.5V	3.5		5		ms	D1 = 0	5,11
			3.5V	14		20		ms	D0 =1	5,11
			5.5V	7		10		ms	D1 = 0	5,11
			3.5V	28		40		ms	D1 = 0	5,11
			5.5V	14		20		ms	D1 = 1	5,11
			3.5V	112		160		ms	D0 = 1	5,11
			5.5V	56		80		ms	D1 = 1	5,11

Table 17. Additional Timing Table (Divide by Two Mode) $T_A = 0 \degree C$ to +70 $\degree C$ (Continued)

Notes

1. The V_{CC} voltage specification of 5.5 V guarantees 5.0 V \pm 0.5 V and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V.

2. Timing Reference uses 0.7 VC0 for a logic 1 and 0.2 VGC for a logic 0.

3. SMR D1 = 0.

4. SMR-D5 = 1, POR STOP Mode Delay is on

- 5. Interrupt request via Port 3 (P31-P33)
- 6. Interrupt request via Port 3 (P30).

7. Maximum frequency for internal system clock is 2 MHz when using Low EMI OSC PCON Bit D7 = 0

8. Reg. WDTMR.

9. Using internal RC.

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Table 18. Additional Timing Table (Divide by Two Mode) T_A = -40 °C to +105 °C (Continued)

No	Symbol	Parameter	V _{CC} ¹	Min	Max	Min	Max	Units	Conditions	Notes
12	Twdt	It Watchdog Timer	3.5V	7		10		ms	D0 =0	8,9
		Delay Time Before	5.5V	3.5		5		ms	D1 = 0	5,11
	limeout	Imeout	3.5V	14		20		ms	D0 =1	5,11
			5.5V	7		10		ms	D1 = 0	5,11
			3.5V	28		40		ms	D1 = 0	5,11
		5.5V 3.5V	5.5V	14		20		ms	D1 = 1	5,11
			3.5V	112		160		ms	D0 = 1	5,11
			5.5V	56		80		ms	D1 = 1	5,11

Notes

The V_{CC} voltage specification of 5.5 V guarantees 5.0 V ± 0.5 V and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V.

- 2. Timing Reference uses 0.7 VC0 for a logic 1 and 0.2 VGC for a logic 0.
- 3. SMR D1 = 0.
- 4. SMR-D5 = 1, POR STOP Mode Delay is on
- 5. Interrupt request via Port 3 (P31-P33)
- 6. Interrupt request via Port 3 (P30).
- 7. Maximum frequency for internal system clock is 2 MHz when using Low EMI OSC PCON Bit D7 = 0
- 8. Reg. WDTMR.
- 9. Using internal RC.

Pin Functions

EPROM Programming Mode

D7-D0 Data Bus. The data can be read from or written to external memory through the data bus.

 V_{CC} Power Supply. This pin must supply 5 V during the EPROM read mode and 6 V during other modes.

CE Chip Enable (active Low). This pin is active during EPROM Read Mode, Program Mode, and Program Verify Mode.

OE Output Enable (active Low). This pin drives the direction of the Data Bus. When this pin is Low, the Data Bus is output, when High, the Data Bus is input.

EPM EPROM Program Mode. This pin controls the different EPROM Program Mode by applying different voltages.

 V_{PP} Program Voltage. This pin supplies the program voltage.

PGM Program Mode (active Low). When this pin is Low, the data is programmed to the EPROM through the Data Bus.

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CLR Clear (active High). This pin resets the internal address counter at the High Level.

CLK Address Clock. This pin is a clock input. The internal address counter increases by one for each clock cycle.

Application Precaution

The production test-mode environment may be enabled accidentally during normal operation if excessive noise surges above V_{CC} occur on pins P31 and RESET.

In addition, processor operation of Z8 OTP devices may be affected by excessive noise surges on the V_{PP} EPM, \overline{OE} pins while the microcontroller is in Standard Mode.

Recommendations for dampening voltage surges in both test and OTP mode include the following:

- Using a clamping diode to V_{CC}
- Adding a capacitor to the affected pin
- Enable EPROM/Test Mode Disable OTP option bit.

Standard Mode

XTAL Crystal 1 (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC, RC network, or external single-phase clock to the on-chip oscillator input.

XTAL2 Crystal 2 (time-based output). This pin connects a parallel-resonant crystal, ceramic resonator, LC, or RC network to the on-chip oscillator output.

 $\mathbf{R}/\overline{\mathbf{W}}$ Read/Write (output, write Low). The $\mathbf{R}/\overline{\mathbf{W}}$ signal is Low when the CCP is writing to the external program or data memory (Z86E43/743/E44 only).

RESET Reset (input, active Low). Reset will initialize the MCU. Reset is accomplished either through Power-On, Watchdog Timer reset, Stop Mode Recovery, or external reset. During Power-On Reset and Watchdog Timer Reset, the internally generated reset drives the reset pin low for the POR time. Any devices driving the reset line must be open-drain in order to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally. After the POR time, RESET is a Schmitt-triggered input. (RESET is available on Z86E43/743/E44 only.)

To avoid asynchronous and noisy reset problems, the Z86E43/743/E44 is equipped with a reset filter of four external clocks (4TpC). If the external reset signal is less than 4TpC in duration, no reset occurs. On the fifth clock after the reset is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external reset, whichever is longer. During the reset cycle, $\overline{\text{DS}}$ is held active Low while $\overline{\text{AS}}$ cycles at a rate of TpC/2. Program execution begins at location 000CH, 5-10 TpC cycles after $\overline{\text{RESET}}$ is released. For Power-On Reset, the reset output time is 5 ms.

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The Z86E43/743/E44 does not reset WDTMR, SMR, P2M, and P3M registers on a Stop-Mode Recovery operation.

ROMless (input, active Low). This pin, when connected to GND, disables the internal ROM and forces the device to function as a Z86C90/C89 ROMless Z8. (Note that, when left unconnected or pulled High to V_{CC} , the device functions nor

Note: When using in ROM Mode in High EMI (noisy) environment, the ROMless pins should be connected directly to V_{CC} .

 $\overline{\mathbf{DS}}$ (output, active Low). Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of $\overline{\mathbf{DS}}$. For WRITE operations, the falling edge of $\overline{\mathbf{DS}}$ indicates that output data is valid.

AS (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle for external memory transfer. Address output is from Port 0/Port 1 for all external programs. Memory address transfers are valid at the trailing edge of \overline{AS} . Under program control, \overline{AS} is placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

Port 0 (P07-P00). Port 0 is an 8-bit, bidirectional, CMOS-compatible I/0 port. These eight I/O lines can be configured under software control as a nibble I/0 port, or as an address port for interfacing external memory. The input buffers are Schmitt-triggered and nibble programmed. Either nibble output that can be globally programmed as push-pull or opendrain. Low EMI output buffers can be globally programmed by the software. Port 0 can be placed under handshake control. In Handshake Mode, Port 3 lines P32 and P35 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to Port 0's upper nibble. The lower nibble must have the same direction as the upper nibble.

For external memory references, Port 0 provides address bits A11-A8 (lower nibble) or Al 5-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. In ROMless mode, after a hardware reset, Port 0 is configured as address lines Al 5-A8, and extended timing is set to accommodate slow memory access. The initialization routine can include re-configuration to eliminate this extended timing mode. In ROM mode, Port 0 is defined as input after reset.

Port 0 can be set in the High-Impedance Mode if selected as an address output state, along with Port 1 and the control signals \overline{AS} , \overline{DS} , and R/\overline{W} (Figure 18).

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Figure 18. Port 0 Configuration

Port 1 (P17-P10). Port 1 is an 8-bit, bidirectional, CMOS-compatible port with multiplexed Address (A7-A0) and Data (D7-D0) ports. These eight I/O lines can be programmed as inputs or outputs or can be configured under software control as an Address/ Data port for interfacing external memory. The input buffers are Schmitt-triggered and the output buffers can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 1 can be placed under handshake control. In this configuration, Port 3, lines P33 and P34 are used as the handshake controls RDY1 and DAV1 (Ready and Data Available). To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 outputs the additional lines (see Figure 19).

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Port 1 can be placed in the high-impedance state along with Port 0, \overline{AS} , \overline{DS} , and R/\overline{W} , allowing the Z86E43/743/E44 to share common resources in multiprocessor and DMA applications. In ROM mode, Port 1 is defined as input after reset.



Figure 19. Port 1 Configuration (Z86E43/743/E44 Only)

Port 2 (P27-P20). Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port. These eight I/O lines can be configured under software control as an input or output, independently. All input buffers are Schmitt-triggered. Bits programmed as outputs can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. When used as an I/O port, Port 2 can be placed under handshake control. After reset, Port 2 is defined as an input.





Figure 27. Counter/Timer Block Diagram

Interrupts. The MCU has six different interrupts from six different sources. The interrupts are maskable and prioritized (Figure 28). The six sources are divided as follows: four sources are claimed by Port 3 lines P33-P30) and two in counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 20).

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from STOP mode when programmed as analog inputs. When the Stop Mode Recovery sources are selected in this register then SMR2 register bits D0, D1 must be set to zero.

Note: *If the Port 2 pin is configured as an output, this output level will be read by the SMR circuitry.*





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Note: WDT time-out in STOP Mode will not reset SMR,SMR2,PCON, WDTMR, P2M, P3M, Ports 2 & 3 Data Registers, but will activate the T_{POR} delay.

WDTMR Register Accessibility. The WDTMR register is accessible only during the first 60 internal system clock cycles from the execution of the first instruction after Power-On Reset, Watchdog reset or a Stop Mode Recovery (Figure 33 and Figure 34). After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register File at address location 0Fh.

Clock Free WDT Reset. The WDT will enable the Z8 to reset the I/0 pins whenever the WDT times out, even without a clock source running on the XTAL1 and XTAL2 pins. WDTMR Bit D4 must be 0 for the clock Free WDT to work. The I/O pins will default to their default settings.

WDTMR (F) 0F

>



* Default setting after RESET

Figure 33. Watchdog Timer Mode Register Write Only





Figure 35. Typical V_{LV} Voltage vs. Temperature

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Note: Note used in conjunction with SMR2 Source

* Default setting after RESET

** Default setting after RESET and STOP-Mode Recovery

Figure 37. Stop Mode Recovery Register (Write Only Except Bit D7, Which is Read Only)









