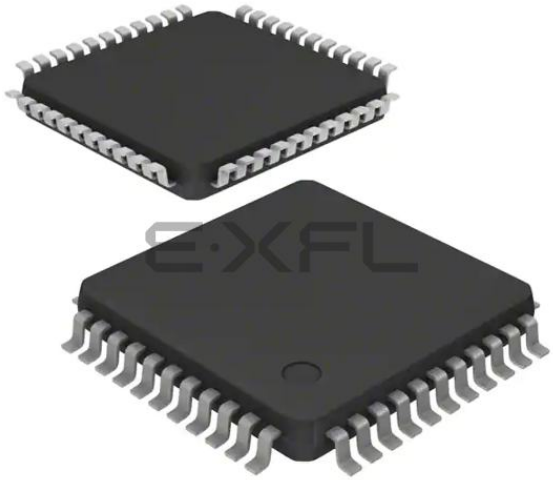

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	EBI/EMI
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8674312fsc00tr

Revision History

Each instance in Revision History reflects a change to this document from its previous revision. For more details, refer to the corresponding pages and appropriate links in the table below.

Date	Revision Level	Description	Page No
May 2008	01	Original issue.	All

Table 1. Z86E33/733/E34, E43/743/E44 Features (Continued)

Device	ROM (KB)	RAM[1] (Bytes)	I/O Lines	Speed (MHz)
Z86E44	16	236	32	12

[1]General-Purpose

- Standard Temperature (V_{CC} = 3.5 V to 5.5 V)
- Extended Temperature (V_{CC} = 3.5 V to 5.5 V)
- Available Packages:
  - 28-Pin DIP/SOIC/PLCC OTP (E33/733/E34)
  - 40-Pin DIP OTP (E43/743/E44)
  - 44-Pin PLCC/LQFP OTP (E43/743/E44)
- Software Enabled Watchdog Timer (WDT)
- Push-Pull/Open-Drain Programmable on Port 0, Port 1, and Port 2
- 24/32 Input/Output Lines
- Clock-Free WDT Reset
- Auto Power-On Reset (POR)
- Programmable OTP Options:
  - RC Oscillator
  - EPROM Protect
  - Auto Latch Disable
  - Permanently Enabled WDT
  - Crystal Oscillator Feedback Resistor Disable
  - RAM Protect
- Low-Power Consumption: 60 mW
- Fast Instruction Pointer: 0.75 µs
- Two Standby Modes: STOP and HALT
- Digital Inputs CMOS Levels, Schmitt-Triggered
- Software Programmable Low EMI Mode
- Two Programmable 8-Bit Counter/Timers Each with a 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Six Different Sources
- Two Comparators

Table 2. 40-Pin DIP Pin Identification Standard Mode (Continued)

Pin No	Symbol	Function	Direction
15	XTAL1	Crystal Oscillator	Input
16-18	P31-P33	Port 3, Pins 1,2,3	Input
19	P34	Port 3, Pin 4	Output
20	AS	Address Strobe	Output
21	RESET	Reset	Input
22	P35	Port 3, Pin 5	Output
23	P37	Port 3, Pin 7	Output
24	P36	Port 3, Pin 6	Output
25	P30	Port 3, Pin 0	Input
26-27	P00-P01	Port 0, Pins 0,1	Input/Output
28-29	P10-P11	Port 1, Pins 0,1	Input/Output
30	P02	Port 0, Pin 2	Input/Output
31	GND	Ground	
32-33	P12-P13	Port 1, Pins 2,3	Input/Output
34	P03	Port 0, Pin 3	Input/Output
35-39	P20-P24	Port 2, Pins 0, 1,2,3,4	Input/Output
40	DS	Data Strobe	Output

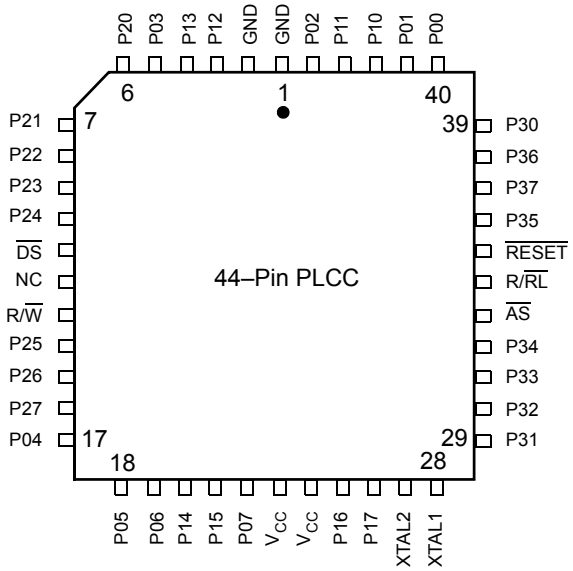


Figure 4. 44-Pin PLCC Pin Configuration Standard Mode

Table 3. 44-Pin PLCC Pin Identification

Pin No	Symbol	Function	Direction
1-2	GND	Ground	
3-4	P12-P13	Port 1, Pins 2,3	Input/Output
5	P03	Port 0, Pin 3	Input/Output
6-10	P20-P24	Port 2, Pins 0,1,2,3,4	Input/Output
11	DS	Data Strobe	Output
12	NC	No Connection	
13	R/$\overline{W}$	Read/Write	Output
14-16	P25-P27	Port 2, Pins 5,6,7	Input/Output
17-19	P04-P06	Port 0, Pins 4,5,6	Input/Output
20-21	P14-P15	Port 1, Pins 4,5	Input/Output
22	P07	Port 0, Pin 7	Input/Output
23-24	V_{CC}	Power Supply	
25-26	P16-P17	Port 1, Pins 6,7	Input/Output

Table 6. 44-Pin PLCC Pin Configuration EPROM Programming Mode (Continued)

Pin No	Symbol	Function	Direction
32-39	NC	No Connection	
40	CLR	Clear	Input
41	CLK	Clock	Input
42-43	NC	No Connection	
44	/PGM	Prog. Mode	Input

Table 12. DC Electrical Characteristics T_A= -40 °C to +105 °C (Continued)

Symbol	Parameter	V_{CC} [1]	Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{OH1}	Output High Voltage	4.5V	V_{CC} -0.4		4.8	V	I_{OH} = -2.0 mA	2
		5.5V	V_{CC} -0.4		4.8	V	I_{OH} = -2.0 mA	2
V_{OL}	Output Low Voltage Low EMI Mode	4.5V		0.4	0.2	V	I_{OL} = 1.0 mA	
		5.5V		0.4	0.2	V	I_{OL} = 1.0 mA	
V_{OL1}	Output Low Voltage	4.5V		0.4	0.1	V	I_{OL} = +4.0 mA	2
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	2
V_{OL2}	Output Low Voltage	4.5V		1.2	0.5	V	I_{OL} = +12 mA	2
		5.5V		1.2	0.5	V	I_{OL} = +12 mA	2
V_{RH}	Reset Input High Voltage	4.5V	.8 V_{CC}	V_{CC}	1.7	V		3
		5.5V	.8 V_{CC}	V_{CC}	2.1	V		3
V_{OLR}	Reset Output Low Voltage	4.5V		0.6	0.3	V	I_{OL} = 1.0 mA	3
		5.5V		0.6	0.2	V	I_{OL} = 1.0 mA	3
V_{OFFSET}	Comparator Input Offset Voltage	4.5V		25	10	mV		
		5.5V		25	10	mV		
V_{ICR}	Input Common Mode Voltage Range	4.5V	0	V_{CC} -1.5V		V		4
		5.5V	0	V_{CC} -1.5V		V		4
I_{IL}	Input Leakage	4.5V	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	4.5V	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	4.5V	-18	-180	-112	µA		3
		5.5V	-18	-180	-112	µA		3
I_{CC}	Supply Current	4.5V		20	15	mA	@ 12 MHz	5,6
		5.5V		20	15	mA	@ 12 MHz	5,6
I_{CC1}	Standby Current HALT Mode	4.5V		6	2	mA	V_{IN} = 0V, V_{CC} @ 12 MHz	5,6
		5.5V		6	4	mA	V_{IN} = 0V, V_{CC} @ 12 MHz	5,6

and P32 with reference to the voltage on P33. The analog function is enabled by setting the D1 of Port 3 Mode Register (P3M). The comparator output can be outputted from P34 and P37, respectively, by setting PCON register Bit D0 to 1 state. For the interrupt function, P30 and P33 are falling edge triggered interrupt inputs. P31 and P32 can be programmed as falling, rising or both edges triggered interrupt inputs (see Figure 21). Access to Counter/Timer 1 is made through P31 (T_{IN}) and P36 (T_{OUT}). Handshake tines for Port 0, Port 1, and Port 2 are also available on Port 3 (see Table 19).

Note: *When enabling or disabling analog mode, the following is recommended:*

1. Allow two NOP decays before reading this comparator output.
2. Disable global interrupts, switch to analog mode, clear interrupts, and then re-enable interrupts.
3. IRQ register bits 3 to 0 must be cleared after enabling analog mode.

Note: *P33-P30 differs from the Z86C33/C43/233/243 in that there is no clamping diode to V_{CC} due to the EPROM high-voltage circuits. Exceeding the V_{IH} maximum specification during standard operating mode may cause the device to enter EPROM mode.*

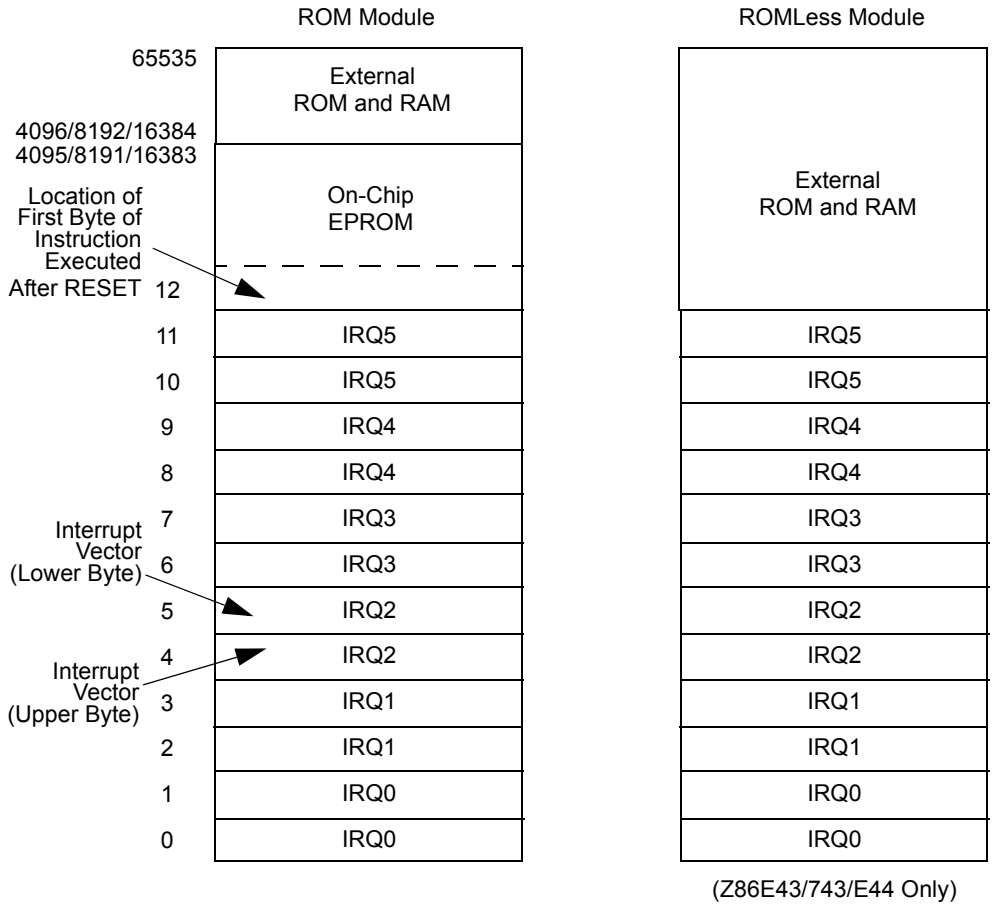


Figure 22. Program Memory Map

EPROM Protect. When in ROM Protect Mode, and executing out of External Program Memory, instructions LDC, LDCI, LDE, and LDEI cannot read Internal Program Memory.

When in EPROM Protect Mode and executing out of Internal Program Memory, instructions LDC, LDCI, LDE, and LDEI can read Internal Program Memory.

Data Memory ($\overline{DM}$). In ROM Mode, the Z86E43/743/E44 can address up to 60156/48 KB of external data memory beginning at location 4096/8192/16384. In ROMless mode, the Z86E43/743/E44 can address up to 64 KB of data memory. External data memory may be included with, or separated from, the external program memory space. $\overline{DM}$, an optional I/0 function that can be programmed to appear on pin P34, is used to distinguish between data and program memory space (Figure 23). The state of the $\overline{DM}$ signal is controlled by the type of instruction being executed. An LDC opcode references PROGRAM ($\overline{DM}$ inactive) memory, and an LDE instruction references data ($\overline{DM}$ active Low) memory.

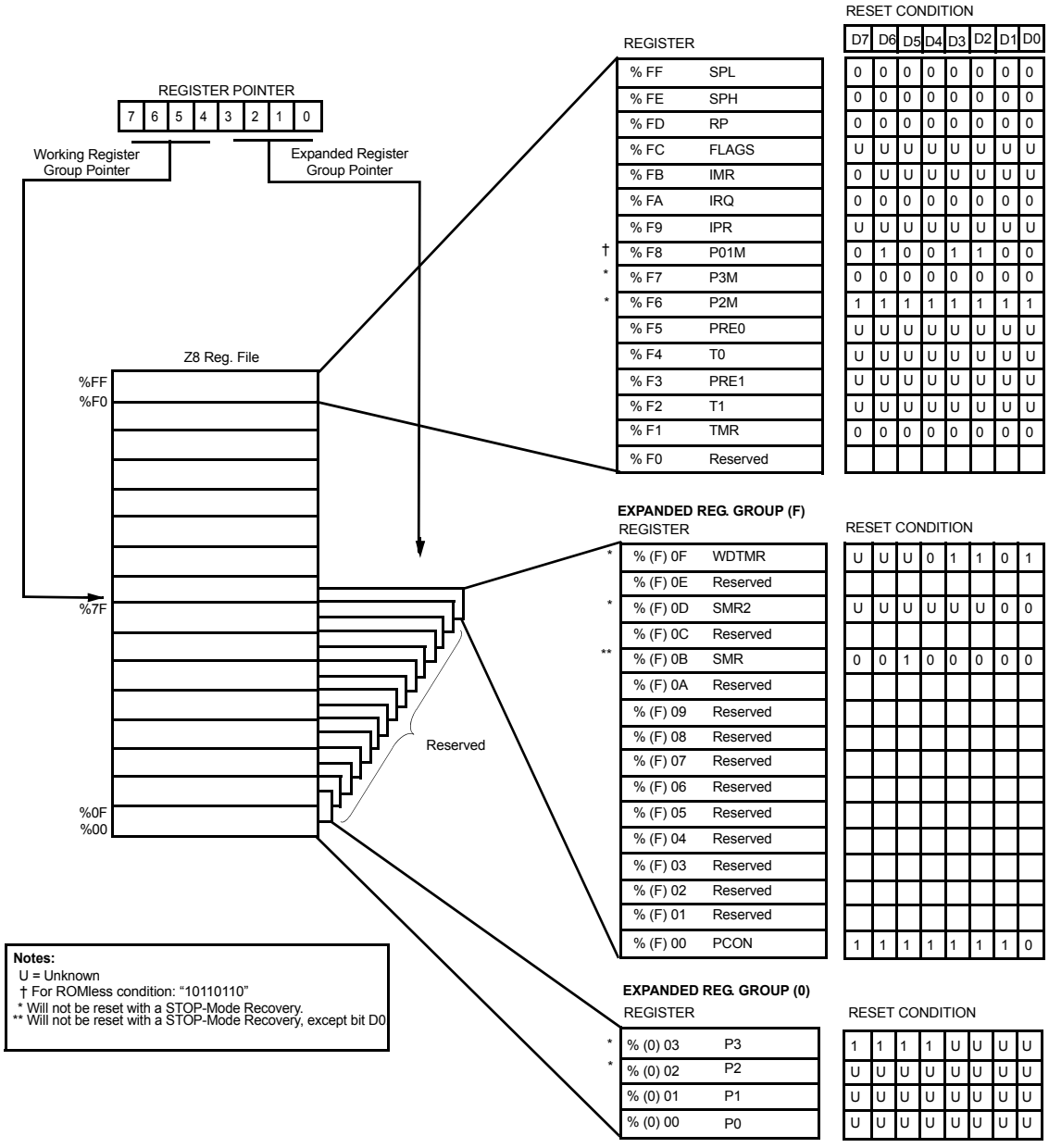


Figure 26. Expanded Register File Architecture

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. The register R254 is general-purpose on Z86E33/733/E34. R254 and R255 are set to 00h after any reset or Stop Mode Recovery.

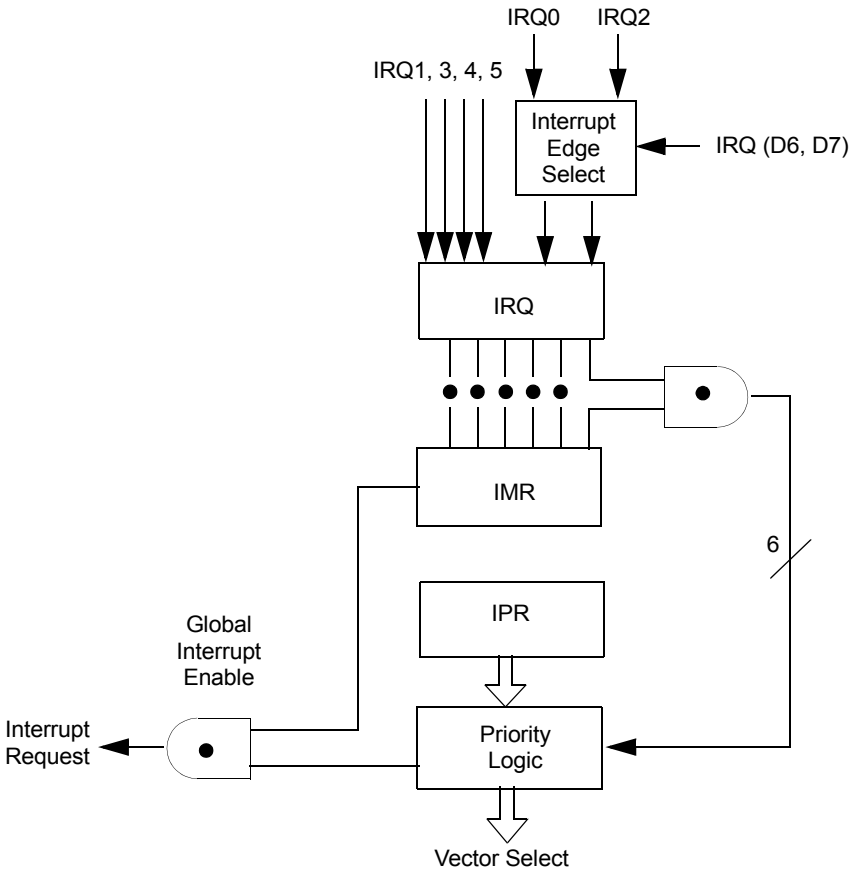


Figure 28. Interrupt Block Diagram

Table 20. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	$\overline{\text{DAV0}}$, IRQ0	0,1	External (P32), Rising/Falling Edge Triggered
IRQ1	IRQ1	2,3	External (P33), Falling Edge Triggered
IRQ2	$\overline{\text{DAV2}}$, IRQ2, T_{IN}	4,5	External (P31), Rising/Falling Edge Triggered
IRQ3	IRQ3	6,7	External (P30), Falling Edge Triggered
1RQ4	T0	8,9	Internal
IRQ5	T1	10,11	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority Register (IPR). An interrupt machine cycle is activated when an interrupt request is granted. Thus, disabling all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests need service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling or both edge triggered, and are programmable by the user. The software may poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in bits D7 and D6 of the IRQ Register (R250). The configuration is shown in Table 21.

Table 21. IRQ Register Configuration

IRO		Interrupt Edge	
D7	**D6**	**P31**	**P32**
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes
1. F = Falling Edge
2. R = Rising Edge

Clock. The on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, RC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 10 kHz to 16 MHz max, with a series resistance (RS) less than or equal to 100 Ω.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's recommended capacitor values from each pin directly to device pin Ground. The RC oscillator option can be selected in the programming mode. The RC oscillator configuration must be an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to Ground (Table 29).

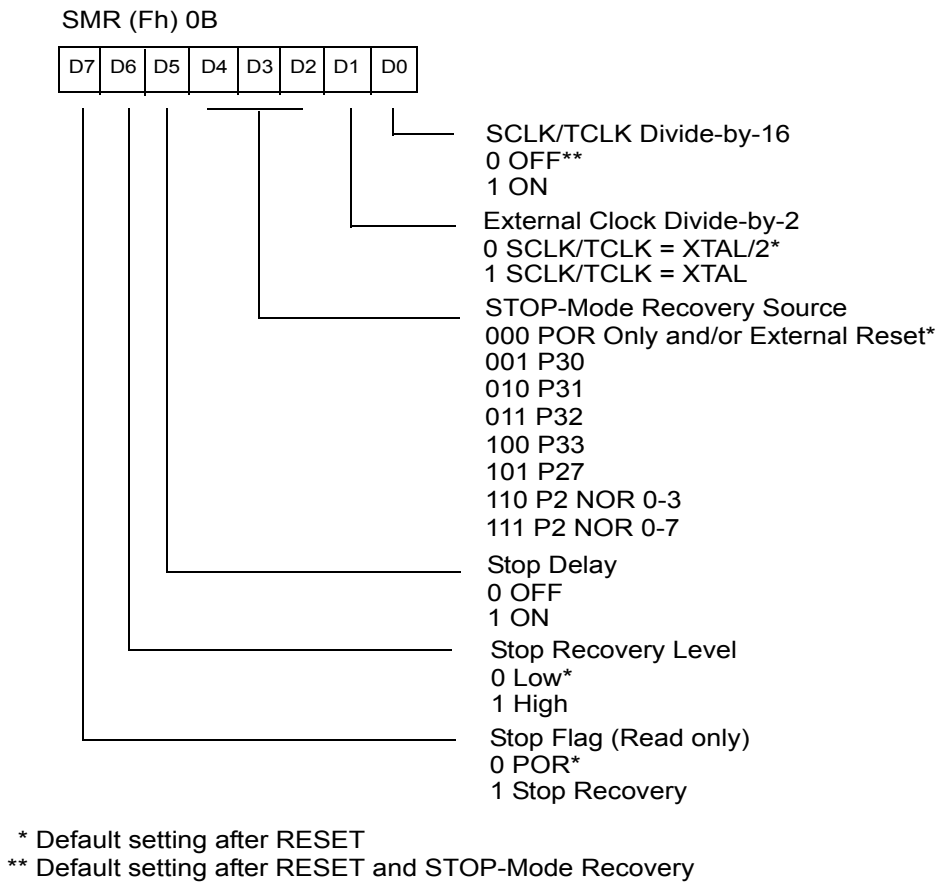


Figure 31. Stop Mode Recovery Register (Write-Only Except Bit D7, Which Is Read-Only)

SCLK/TCLK Divide-by-16 Select (D0). This bit of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources counter/timers and interrupt logic).

External Clock Divide-by-Two (D1). This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, the System Clock (SCLK) and Timer Clock (TCLK) are equal to the external clock frequency divided by two. The SCLK/TCLK is equal to the external clock frequency when this bit is set (D1=1). Using this bit together with D7 of PCON further helps lower EMI (that is, D7 (PCON) = 0, D1 (SMR) = 1). The default setting is zero.

Stop Mode Recovery Source (D2, D3, and D4). These three bits of the SMR register specify the wake up source of the Stop Mode Recovery (Figure 32). Table 22 shows the SMR source selected with the setting of D2 to D4. P33-P31 cannot be used to wake up

from STOP mode when programmed as analog inputs. When the Stop Mode Recovery sources are selected in this register then SMR2 register bits D0, D1 must be set to zero.

Note: *If the Port 2 pin is configured as an output, this output level will be read by the SMR circuitry.*

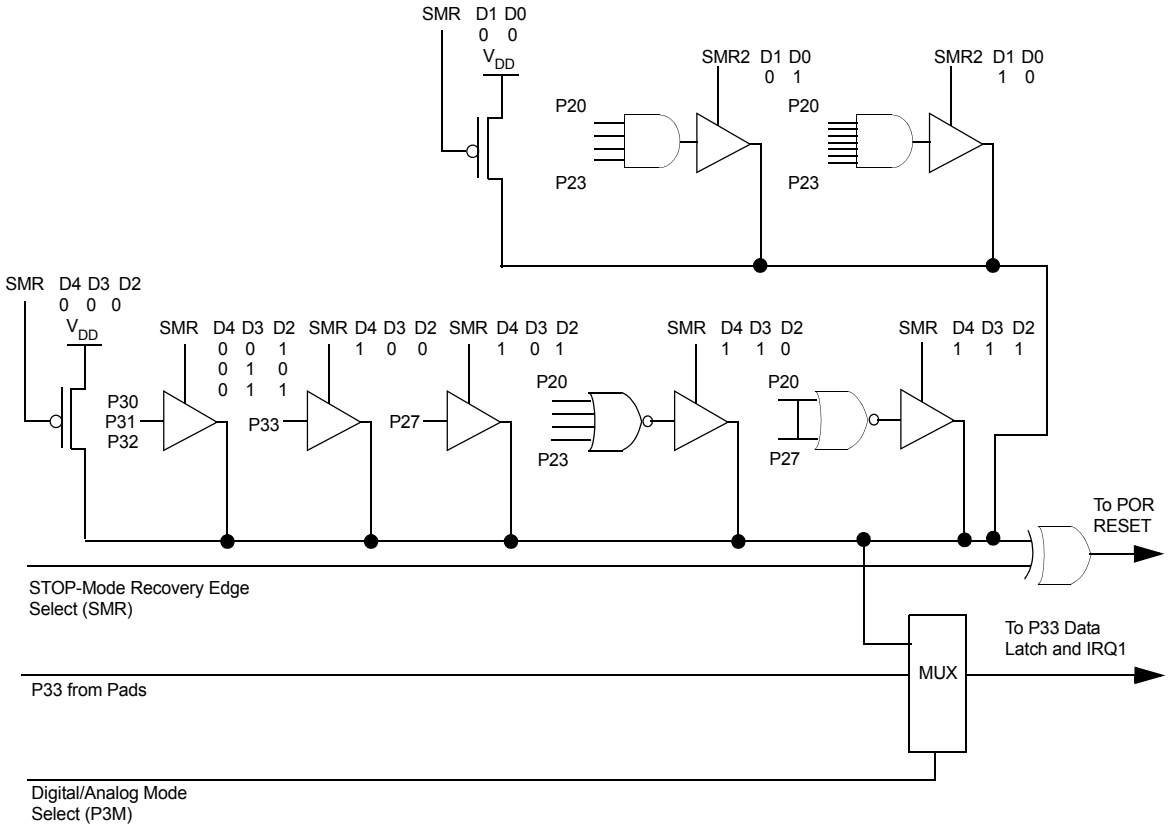


Figure 32. Stop Mode Recovery Source

Table 22. Stop Mode Recovery Source

D4	D3	D2	SMR Source selection
0	0	0	POR recovery only
0	0	1	P30 transition
0	1	0	P31 transition (Not in analog mode)
0	1	1	P32 transition (Not in analog mode)
1	0	0	P33 transition (Not in analog mode)
1	0	1	P27 transition
1	1	0	Logical NOR of Port 2 bits 0-3
1	1	1	Logical NOR of Port 2 bits 0-7

Stop Mode Recovery Delay Select (D5). The 5 ms RESET delay after Stop Mode Recovery is disabled by programming this bit to a zero. A "1" in this bit will cause a 5 ms RESET delay after Stop Mode Recovery. The default condition of this bit is 1. If the fast wake up mode is selected, the Stop Mode Recovery source needs to be kept active for at least 5TpC.

Stop Mode Recovery Level Select (D6). A "1" in this bit defines that a high level on any one of the recovery sources wakes the MCU from STOP Mode. A 0 defines low level recovery. The default value is 0.

Cold or Warm Start (D7). This bit is set by the device upon entering STOP Mode. A "0" in this bit indicates that the device has been reset by POR (cold). A "1" in this bit indicates the device was awakened by a SMR source (warm).

Stop Mode Recovery Register 2 (SMR2). This register contains additional Stop Mode Recovery sources. When the Stop Mode Recovery sources are selected in this register then SMR Register Bits D2, D3, and D4 must be 0.

SMR:10		Operation
D1	DO	Description of Action
0	0	POR and/or external reset recovery
0	1	Logical AND of P20 through P23
1	0	Logical AND of P20 through P27

Watchdog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is disabled after Power-On

Note: *WDT time-out in STOP Mode will not reset SMR,SMR2,PCON, WDTMR, P2M, P3M, Ports 2 & 3 Data Registers, but will activate the T_{POR} delay.*

WDTMR Register Accessibility. The WDTMR register is accessible only during the first 60 internal system clock cycles from the execution of the first instruction after Power-On Reset, Watchdog reset or a Stop Mode Recovery (Figure 33 and Figure 34). After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register File at address location 0Fh.

Clock Free WDT Reset. The WDT will enable the Z8 to reset the I/0 pins whenever the WDT times out, even without a clock source running on the XTAL1 and XTAL2 pins. WDTMR Bit D4 must be 0 for the clock Free WDT to work. The I/O pins will default to their default settings.

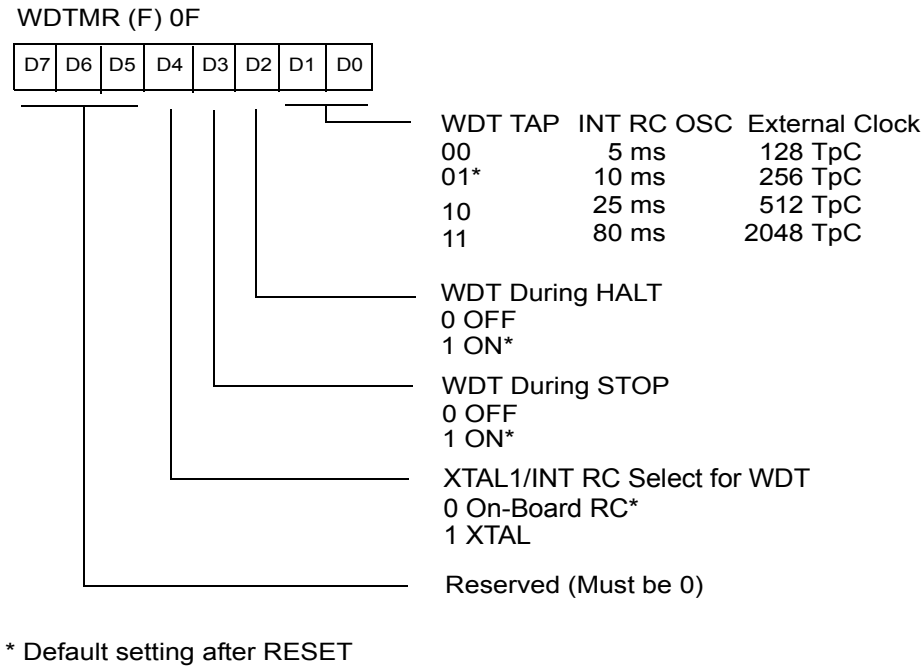


Figure 33. Watchdog Timer Mode Register Write Only

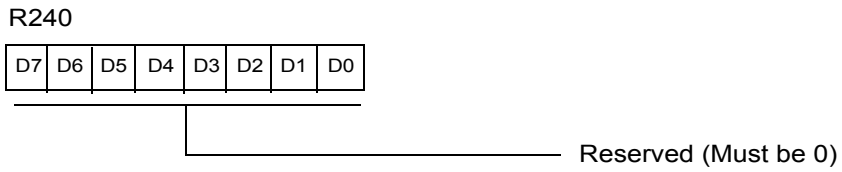


Figure 40. Reserved

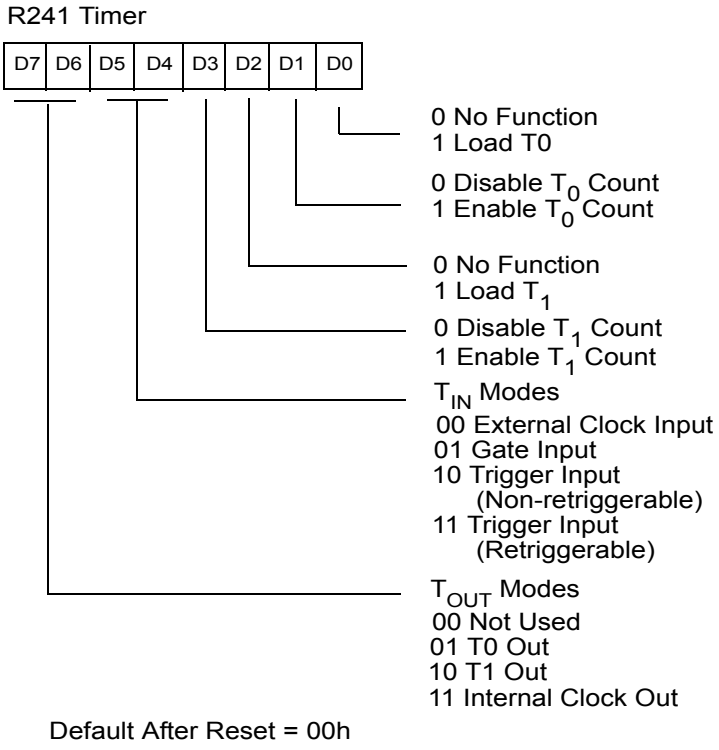


Figure 41. Timer Mode Register ($F1_h$: Read/Write)

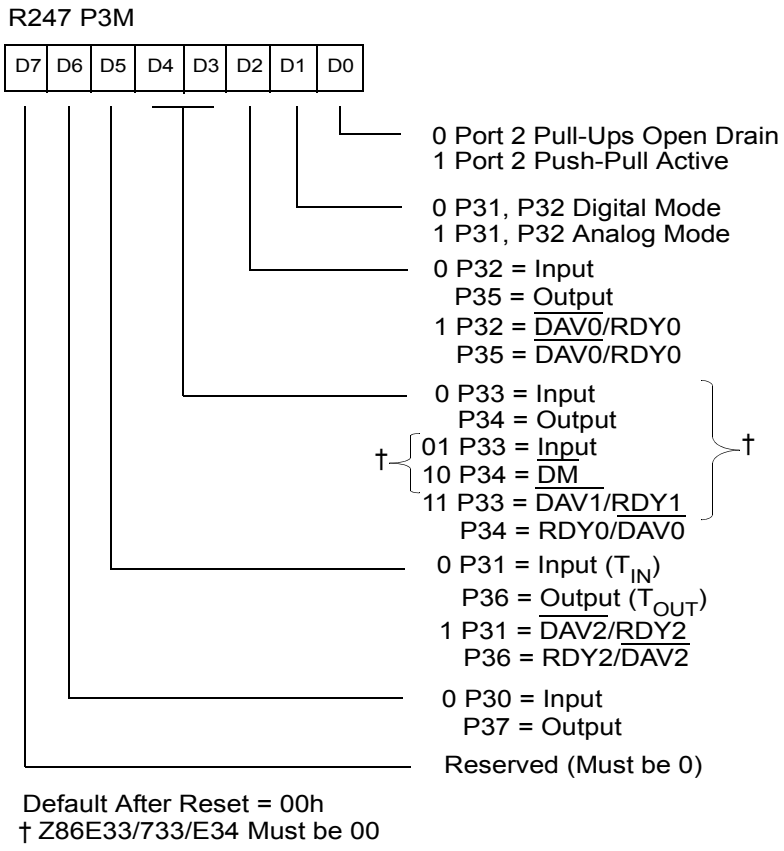
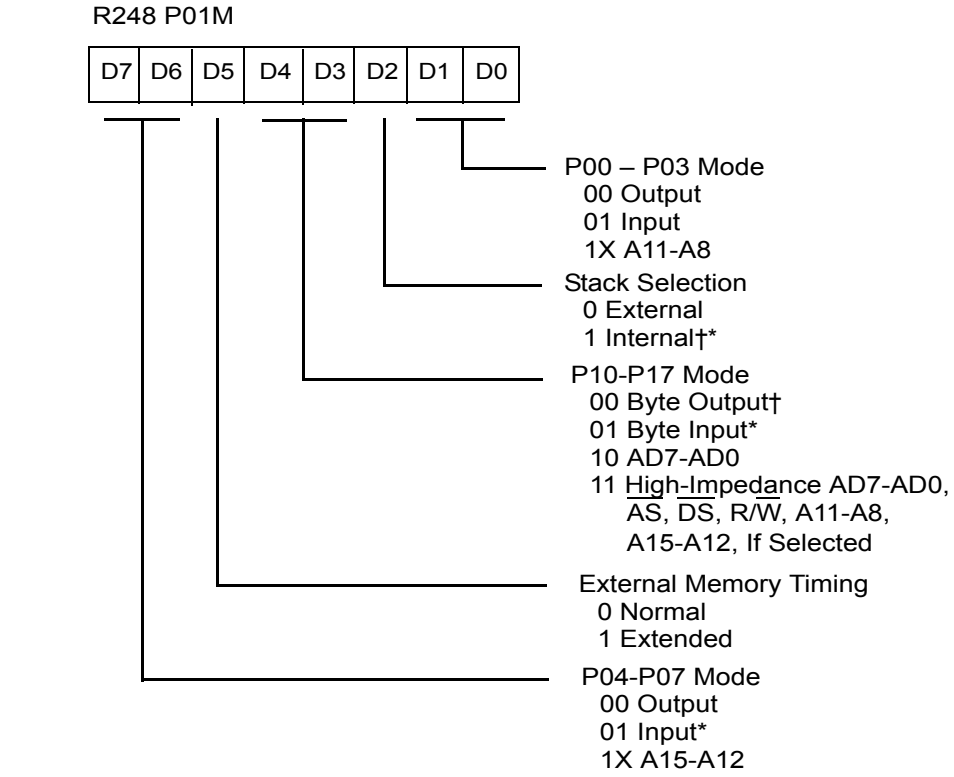
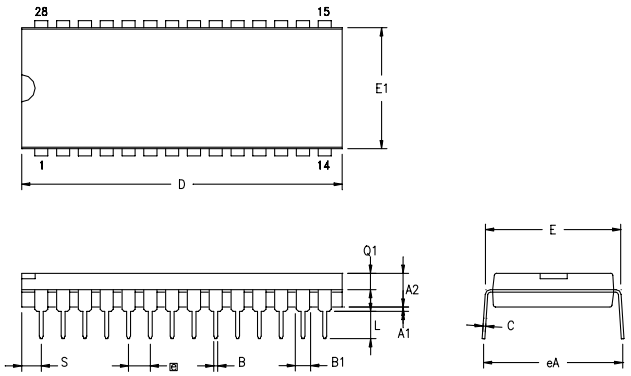


Figure 47. Port 3 Mode Register ($F7_h$: Write Only)



Reset Condition = 0100 1101B
For ROMless Condition = 1011 0110B
† Z86E33/733/E34 Must be 00
* Default after Reset

Figure 48. Port 0 and 1 Mode Register ($F8_h$: Write Only)

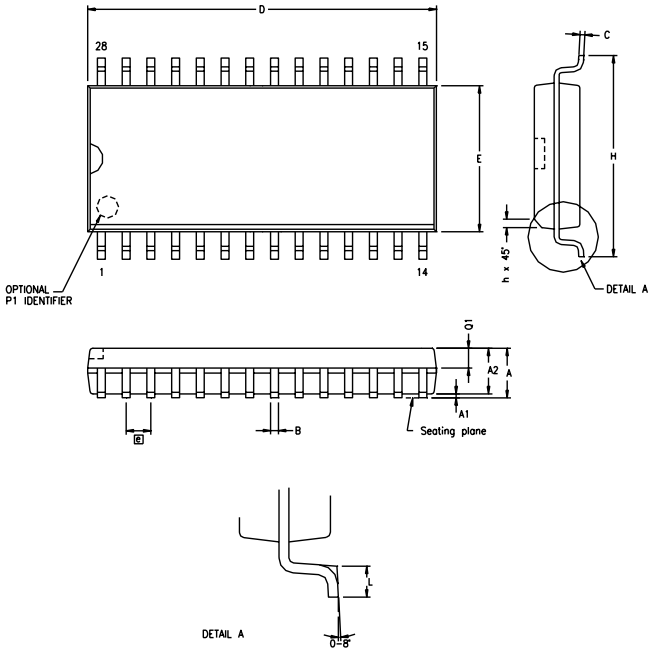


SYMBOL	OPT #	MILLIMETER		INCH	
		MIN	MAX	MIN	MAX
A1		0.38	1.02	.015	.040
A2		3.18	4.19	.125	.165
B		0.38	0.53	.015	.021
B1	01	1.40	1.65	.055	.065
	02	1.14	1.40	.045	.055
C		0.23	0.38	.009	.015
D	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
e		2.54 TYP		.100 TYP	
eA		15.49	16.76	.610	.660
L		3.05	3.81	.120	.150
Q1	01	1.40	1.91	.055	.075
	02	1.40	1.78	.055	.070
S	01	1.52	2.29	.060	.090
	02	1.02	1.52	.040	.060

CONTROLLING DIMENSIONS : INCH

OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

Figure 58. 28-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.64	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	17.78	18.00	.700	.710
E	7.40	7.60	.291	.299
e	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.71	.012	.028
L	0.61	1.00	.024	.039
Q1	0.97	1.09	.038	.043

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 59. 28-Pin SOIC Package Diagram

Ordering Information

Table 24.Ordering Information

Product	Speed (MHz)	Package Type	Pin Count
Z86E3312PSC	12	PDIP	28
Z86E3312SCC	12	SOIC	28
Z86E3312PSC	12	PLCC	28
Z86E3412PEC	12	PDIP	28
Z86E3412PSC	12	PDIP	28
Z86E3412SSC	12	SOIC	28
Z86E3412VSC	12	PLCC	28
Z86E4312FSC	12	LQFP	44
Z86E4312PSC	12	PDIP	40
Z86E4312VSC	12	PLCC	44
Z86E4412FSC	12	LQFP	44
Z86E4412PEC	12	PDIP	40
Z86E4412PSC	12	PDIP	40
Z86E4412VSC	12	PLCC	44
Z8673312PSC	12	PDIP	28
Z8673312SSC	12	SOIC	28
Z8673312VSC	12	PLCC	28
Z8674312FSC	12	LQFP	44
Z8674312PSC	12	PDIP	40
Z8674312VSC	12	PLCC	44