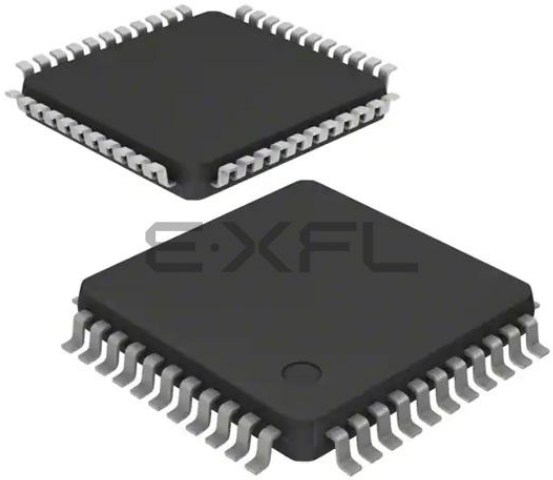

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	EBI/EMI
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8674312fsg

- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive

Functional Block Diagram

Figure 1 displays the functional block diagram.

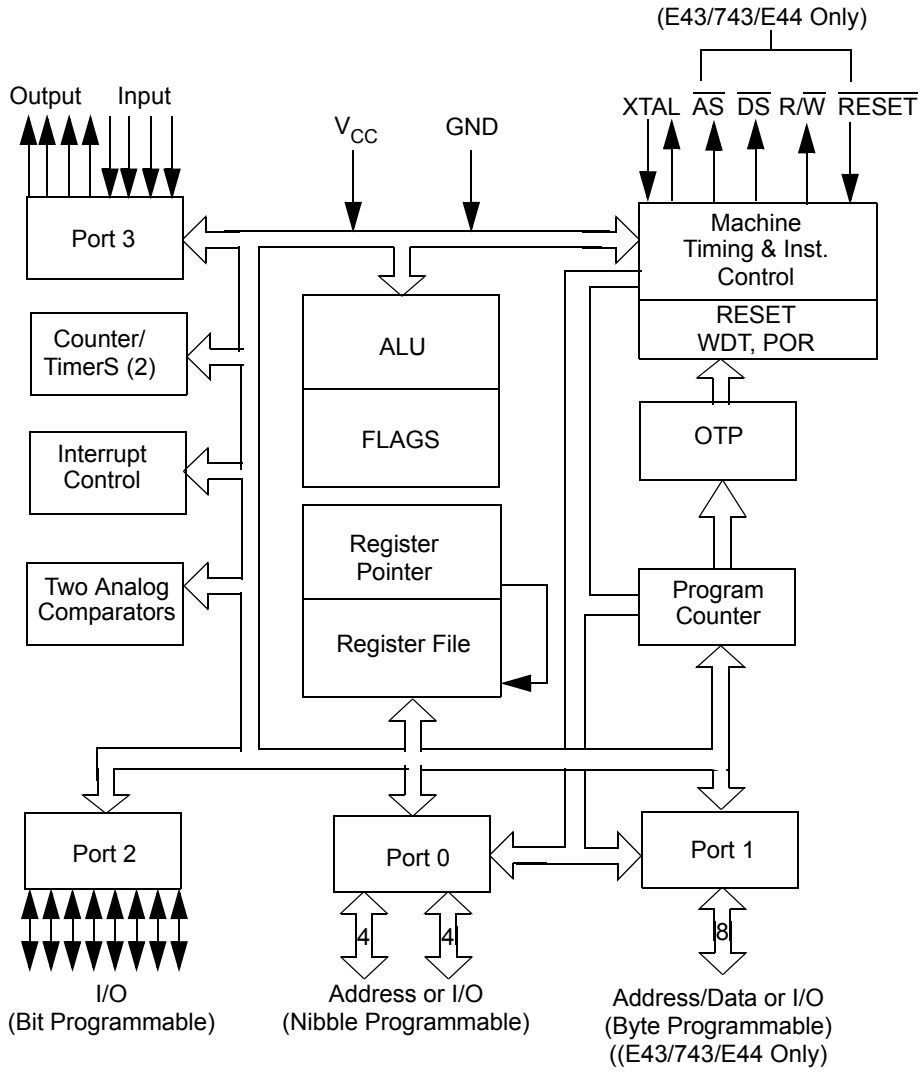


Figure 1. Functional Block Diagram

Table 4. 44-Pin LQFP Pin Identification (Continued)

Pin No	Symbol	Function	Direction
18	RESET	Reset	Input
19	P35	Port 3, Pin 5	Output
20	P37	Port 3, Pin 7	Output
21	P36	Port 3, Pin 6	Output
22	P30	Port 3, Pin 0	Input
23-24	P00-P01	Port 0, Pin 0,1	Input/Output
25-26	P10-P11	Port 1, Pins 0,1	Input/Output
27	P02	Port 0, Pin 2	Input/Output
28-29	GND	Ground	
30-31	P12-P13	Port 1, Pins 2,3	Input/Output
32	P03	Port 0, Pin 3	Input/Output
33-37	P20-24	Port 2, Pins 0,1,2,3,4	Input/Output
38	DS	Data Strobe	Output
39	NC	No Connection	
40	R/$\overline{W}$	Read/Write	Output
41-43	P25-P27	Port 2, Pins 5,6,7	Input/Output
44	P04	Port 0, Pin 4	Input/Output

Table 6. 44-Pin PLCC Pin Configuration EPROM Programming Mode (Continued)

Pin No	Symbol	Function	Direction
32-39	NC	No Connection	
40	CLR	Clear	Input
41	CLK	Clock	Input
42-43	NC	No Connection	
44	/PGM	Prog. Mode	Input

Table 7. 44-Pin LQFP Pin Identification EPROM Programming Mode (Continued)

Pin No	Symbol	Function	Direction
33-37	D0-D4	Data 0,1,2,3,4	Input/Output
38-40	NC	No Connection	
41-43	D5-D7	Data 5,6,7	Input/Output
44	NC	No Connection	

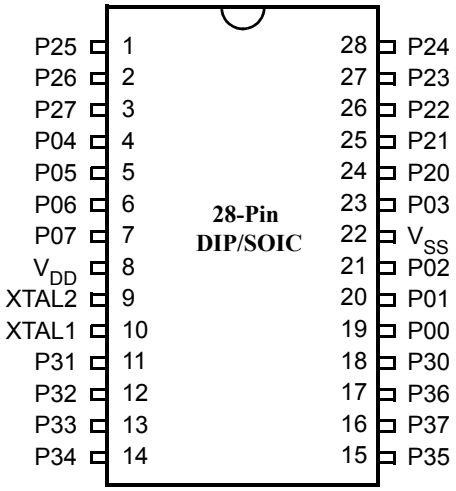


Figure 9. Standard Mode 28-Pin DIP/SOIC Pin Configuration

Table 8. 28-Pin DIP/SOIC/PLCC Pin Identification Standard Mode

Pin No	Symbol	Function	Direction
1-3	P25-P27	Port 2, Pins 5,6,	Input/Output
4-7	P04-P07	Port 0, Pins 4,5,6,7 In/Output	
8	V_{CC}	Power Supply	
9	XTAL2	Crystal Oscillator	Output
10	XTAL1	Crystal Oscillator	Input
11-13	P31-P33	Port 3, Pins 1,2,3	Input
14-15	P34-P35	Port 3, Pins 4,5	Output
16	P37	Port 3, Pin 7	Output
17	P36	Port 3, Pin 6	Output
18	P30	Port 3, Pin 0	Input
19-21	P00-P02	Port 0, Pins 0,1,2	Input/Output
22	V_{SS}	Ground	
23	P03	Port 0, Pin 3	Input/Output
24-28	P20-P24	Port 2, Pins 0,1,2,3,4	Input/Output

Table 11. DC Electrical Characteristics T_A = 0 °C to +70 °C (Continued)

Symbol	Parameter	V_{CC}[1]	Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{OFFSET}	Comparator Input Offset Voltage	3.5V		25	10	mV		
		5.5V		25	10	mV		
V_{ICR}	Input Common Mode Voltage Range	3.5V	0	V_{CC} -1.0V		V		4
		5.5V	0	V_{CC} -1.0V		V		4
I_{IL}	Input Leakage	3.5V	-1	2	0.032	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	2	0.032	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.5V	-1	2	0.032	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	2	0.032	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	3.5V	-20	-130	-65	µA		
		5.5V	-20	-180	-112	µA		
I_{CC}	Supply Current	3.5V		15	5	mA	@ 12 MHz	5,6
		5.5V		20	15	mA	@ 12 MHz	5,6
I_{CC1}	Standby Current HALT Mode	3.5V		4	2	mA	V_{IN} = 0V, V_{CC} @ 12 MHz	5,6
		5.5V		6	4	mA		5,6
		3.5V		3	1.5	mA	Clock Divide by 16 @ 12 MHz	5,6
		5.5V		5	3	mA		5,6
I_{CC2}	Standby Current STOP Mode	3.5V		10	2	µA	V_{IN} = 0V, V_{CC}	7,8,9
		5.5V		10	3	µA	V_{IN} = 0V, V_{CC}	7,8,9
		3.5V		15	7	µA	V_{IN} = 0V, V_{CC}	7,8
		5.5V		30	10	µA	V_{IN} = 0V, V_{CC}	7,8
I_{ALL}	Auto Latch Low Current	3.0V	0.7	8	2.4	µA	0V < V_{IN} < V_{CC}	10
		5.5V	1.4	15	4.7	µA	0V < V_{IN} < V_{CC}	10
I_{ALH}	Auto Latch High Current	3.5V	-0.6	-5	-1.8	µA	0V < V_{IN} < V_{CC}	10
		5.5V	-1	-8	-3.8	µA	0V < V_{IN} < V_{CC}	10

Table 13. DC Electrical Characteristics T_A = 0 °C to +70 °C, 12 MHz (Continued)

No.	Symbol	Parameter	V_{CC} [1]	Min	Max	Units	Notes
4	TwAS	$\overline{AS}$ Low Width	3.5V	55		ns	2
			5.5V	55		ns	2
5	TdAS(DS)	Address Float to $\overline{DS}$ Fall	3.5V	0		ns	
			5.5V	0		ns	
6	TwDSR	$\overline{DS}$ (Read) Low Width	3.5V	200		ns	2,3
			5.5V	200		ns	2,3
7	TwDSW	$\overline{DS}$ (Write) Low Width	3.5V	110		ns	2,3
			5.5V	110		ns	2,3
8	TdDSR(DR)	$\overline{DS}$ Fail to Read Data Req'd Valid	3.5V		150	ns	2,3
			5.5V		150	ns	2,3
9	ThDR(DS)	Read Data to $\overline{DS}$ Rise Hold Time	3.5V	0		ns	2
			5.5V	0		ns	2
10	TdDS(A)	$\overline{DS}$ Rise to Address Active Delay	3.5V	45		ns	2
			5.5V	55		ns	2
11	TdDS(AS)	$\overline{DS}$ Rise to $\overline{AS}$ Fall Delay	3.5V	30		ns	2
			5.5V	45		ns	2
12	TdR/W(AS)	R/$\overline{W}$ Valid to $\overline{AS}$ Rise Delay	3.5V	45		ns	2
			5.5V	45		ns	2
13	TdDS(R/W)	$\overline{DS}$ Rise to R/$\overline{W}$ Not Valid	3.5V	45		ns	2
			5.5V	45		ns	2
14	TdDW(DSW)	Write Data Valid to $\overline{DS}$ Fall (Write) Delay	3.5V	55		ns	2
			5.5V	55		ns	2
15	TdDS(DW)	$\overline{DS}$ Rise to Write Data Not Valid Delay	3.5V	45		ns	2
			5.5V	55		ns	2
16	TdA(DR)	Address Valid to Read Data Req'd Valid	3.5V		310	ns	2,3
			5.5V		310	ns	2,3
17	TdAS(DS)	$\overline{AS}$ Rise to $\overline{DS}$ Fall Delay	3.5V	65		ns	2
			5.5V	65		ns	2

Table 14. DC Electrical Characteristics T_A = -40 °C to +105 °C, 12 MHz (Continued)

No.	Symbol	Parameter	V_{CC}[1]	Min	Max	Units	Notes
10	TdDS(A)	$\overline{DS}$ Rise to Address Active Delay	4.5V	45		ns	2
			5.5V	55		ns	2
11	TdDS(AS)	$\overline{DS}$ Rise to $\overline{AS}$ Fall Delay	4.5V	45		ns	2
			5.5V	45		ns	2
12	TdR/W(AS)	R/$\overline{W}$ Valid to $\overline{AS}$ Rise Delay	4.5V	45		ns	2
			5.5V	45		ns	2
13	TdDS(R/W)	$\overline{DS}$ Rise to R/$\overline{W}$ Not Valid	4.5V	45		ns	2
			5.5V	45		ns	2
14	TdDW(DSW)	Write Data Valid to $\overline{DS}$ Fall (Write) Delay	4.5V	55		ns	2
			5.5V	55		ns	2
15	TdDS(DW)	$\overline{DS}$ Rise to Write Data Not Valid Delay	4.5V	55		ns	2
			5.5V	55		ns	2
16	TdA(DR)	Address Valid to Read Data Req'd Valid	4.5V		310	ns	2,3
			5.5V		310	ns	2,3
17	TdAS(DS)	$\overline{AS}$ Rise to $\overline{DS}$ Fall Delay	4.5V	65		ns	2
			5.5V	65		ns	2
18	TdDM(AS)	$\overline{DM}$ Valid to $\overline{AS}$ Rise Delay	4.5V	35		ns	2
			5.5V	35		ns	2
19	ThDS(AS)	$\overline{DS}$ Valid to Address Valid Hold Time	4.5V	35		ns	2
			5.5V	35		ns	2

Notes

1. The V_{CC} voltage specification of 5.5 V guarantees 5.0 V ± 0.5 V and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V.
2. Timing numbers given are for minimum TpC.
3. When using extended memory timing, add 2 TpC.

Standard Test Load

All timing references use 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

For Standard Mode (not Low-EMI Mode for outputs) with SMR, D1 = 0, D0 = 0.

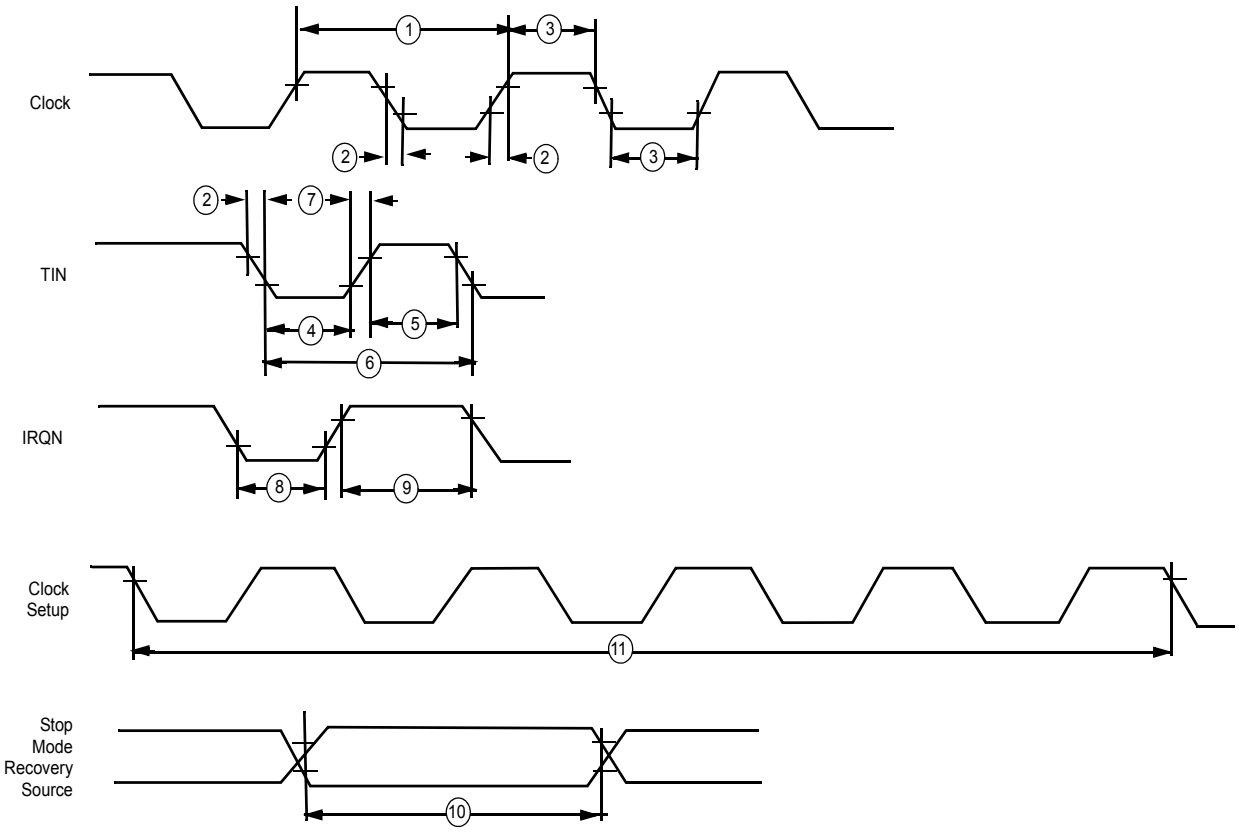


Figure 15. Additional Timing Diagram

Table 15. Additional Timing Table (Divide-By-One Mode) T_A = 0 °C to +70 °C

No	Symbol	Parameter	V_{CC} [1]	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.5V	250	DC	166	DC	ns	2,3,4
			5.5V	250	DC	166	DC	ns	2,3,4
2	TrC,TfC	Clock Input Rise & Fall Times	3.5V		25		25	ns	2,3,4
			5.5V		25		25	ns	2,3,4
3	TwC	Input Clock Width	3.5V	100		100		ns	2,3,4
			5.5V	100		100		ns	2,3,4
4	TwTinL	Timer Input Low Width	3.5V	100		100		ns	2,3,4
			5.5V	70		70		ns	2,3,4

Table 17. Additional Timing Table (Divide by Two Mode) T_A = 0 °C to +70 °C (Continued)

No	Symbol	Parameter	V_{CC}[1]	Min	Max	Min	Max	Units	Conditions	Notes
4	TwTinL	Timer Input Low Width	3.5V	70		70		ns		2,6,4
			5.5V	70		70		ns		2,6,4
5	TwTinH	Timer Input High Width	3.5V	5TpC		5TpC				2,6,4
			5.5V	5TpC		5TpC				2,6,4
6	TpTin	Timer Input Period	3.5V	8TpC		8TpC				2,6,4
			5.5V	8TpC		8TpC				2,6,4
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.5V		100		100	ns		2,6,4
			5.5V		100		100	ns		2,6,4
8A	TwIL	Int. Request Low Time	3.5V	70		70		ns		2,6,4,5
			5.5V	70		70		ns		2,6,4,5
8B	TwIL	Int. Request Low Time	3.5V	5TpC		5TpC				2,6,4,5
			5.5V	5TpC		5TpC				2,6,4,5
9	TwIH	Int. Request Input High Time	3.5V	5TpC		5TpC				2,6,4,5
			5.5V	5TpC		5TpC				2,6,4,5
10	Twsm	Stop Mode Recovery Width Spec	3.5V	12		12		ns		6,7
			5.5V	12		12		ns		6,7
11	Tost	Oscillator Startup Time	3.5V		5TpC		5TpC			6,7
			5.5V		5TpC		5TpC			6,7
12	Twdt	Watchdog Timer Delay Time Before Timeout	3.5V	7		10		ms	D0 =0	8,9
			5.5V	3.5		5		ms	D1 = 0	5,11
			3.5V	14		20		ms	D0 =1	5,11
			5.5V	7		10		ms	D1 = 0	5,11
			3.5V	28		40		ms	D1 = 0	5,11
			5.5V	14		20		ms	D1 = 1	5,11
			3.5V	112		160		ms	D0 = 1	5,11
			5.5V	56		80		ms	D1 = 1	5,11

Notes

1. The V_{CC} voltage specification of 5.5 V guarantees 5.0 V ± 0.5 V and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V.
2. Timing Reference uses 0.7 VC0 for a logic 1 and 0.2 VGC for a logic 0.
3. SMR D1 = 0.
4. SMR-D5 = 1, POR STOP Mode Delay is on
5. Interrupt request via Port 3 (P31-P33)
6. Interrupt request via Port 3 (P30).
7. Maximum frequency for internal system clock is 2 MHz when using Low EMI OSC PCON Bit D7 = 0
8. Reg. WDTMR.
9. Using internal RC.

CLR Clear (active High). This pin resets the internal address counter at the High Level.

CLK Address Clock. This pin is a clock input. The internal address counter increases by one for each clock cycle.

Application Precaution

The production test-mode environment may be enabled accidentally during normal operation if excessive noise surges above V_{CC} occur on pins P31 and $\overline{\text{RESET}}$.

In addition, processor operation of Z8 OTP devices may be affected by excessive noise surges on the V_{PP}, EPM, $\overline{\text{OE}}$ pins while the microcontroller is in Standard Mode.

Recommendations for dampening voltage surges in both test and OTP mode include the following:

- Using a clamping diode to V_{CC}
- Adding a capacitor to the affected pin
- Enable EPROM/Test Mode Disable OTP option bit.

Standard Mode

XTAL Crystal 1 (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC, RC network, or external single-phase clock to the on-chip oscillator input.

XTAL2 Crystal 2 (time-based output). This pin connects a parallel-resonant crystal, ceramic resonator, LC, or RC network to the on-chip oscillator output.

R/$\overline{\text{W}}$ Read/Write (output, write Low). The R/$\overline{\text{W}}$ signal is Low when the CCP is writing to the external program or data memory (Z86E43/743/E44 only).

$\overline{\text{RESET}}$ Reset (input, active Low). Reset will initialize the MCU. Reset is accomplished either through Power-On, Watchdog Timer reset, Stop Mode Recovery, or external reset. During Power-On Reset and Watchdog Timer Reset, the internally generated reset drives the reset pin low for the POR time. Any devices driving the reset line must be open-drain in order to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally. After the POR time, $\overline{\text{RESET}}$ is a Schmitt-triggered input. ($\overline{\text{RESET}}$ is available on Z86E43/743/E44 only.)

To avoid asynchronous and noisy reset problems, the Z86E43/743/E44 is equipped with a reset filter of four external clocks (4TpC). If the external reset signal is less than 4TpC in duration, no reset occurs. On the fifth clock after the reset is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external reset, whichever is longer. During the reset cycle, $\overline{\text{DS}}$ is held active Low while $\overline{\text{AS}}$ cycles at a rate of TpC/2. Program execution begins at location 000CH, 5-10 TpC cycles after $\overline{\text{RESET}}$ is released. For Power-On Reset, the reset output time is 5 ms.

The Z86E43/743/E44 does not reset WDTMR, SMR, P2M, and P3M registers on a Stop-Mode Recovery operation.

$\overline{\text{ROMless}}$ (input, active Low). This pin, when connected to GND, disables the internal ROM and forces the device to function as a Z86C90/C89 ROMless Z8. (Note that, when left unconnected or pulled High to V_{CC}, the device functions nor

Note: *When using in ROM Mode in High EMI (noisy) environment, the ROMless pins should be connected directly to V_{CC}.*

$\overline{\text{DS}}$ (output, active Low). Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of $\overline{\text{DS}}$. For WRITE operations, the falling edge of $\overline{\text{DS}}$ indicates that output data is valid.

$\overline{\text{AS}}$ (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle for external memory transfer. Address output is from Port 0/Port 1 for all external programs. Memory address transfers are valid at the trailing edge of $\overline{\text{AS}}$. Under program control, $\overline{\text{AS}}$ is placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

Port 0 (P07-P00). Port 0 is an 8-bit, bidirectional, CMOS-compatible I/0 port. These eight I/O lines can be configured under software control as a nibble I/0 port, or as an address port for interfacing external memory. The input buffers are Schmitt-triggered and nibble programmed. Either nibble output that can be globally programmed as push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 0 can be placed under handshake control. In Handshake Mode, Port 3 lines P32 and P35 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to Port 0's upper nibble. The lower nibble must have the same direction as the upper nibble.

For external memory references, Port 0 provides address bits A11-A8 (lower nibble) or Al 5-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. In ROMless mode, after a hardware reset, Port 0 is configured as address lines Al 5-A8, and extended timing is set to accommodate slow memory access. The initialization routine can include re-configuration to eliminate this extended timing mode. In ROM mode, Port 0 is defined as input after reset.

Port 0 can be set in the High-Impedance Mode if selected as an address output state, along with Port 1 and the control signals $\overline{\text{AS}}$, $\overline{\text{DS}}$, and R/$\overline{\text{W}}$ (Figure 18).

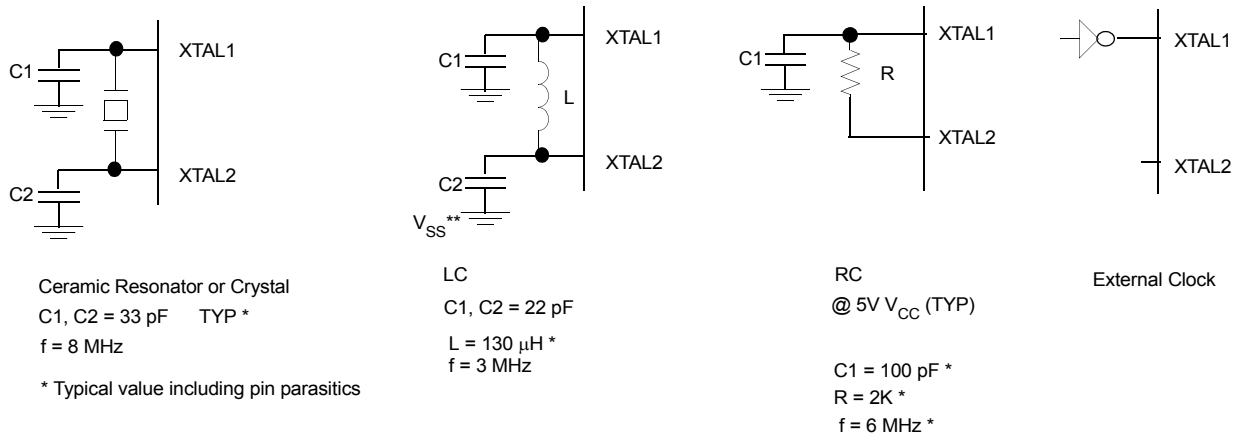


Figure 29. Oscillator Configuration

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR timer allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

1. Power fail to Power OK status
2. Stop Mode Recovery (if D5 of SMR=0)
3. WDT time-out

The POR time is a nominal 5 ms. Bit 5 of the STOP mode Register (SMR) determines whether the POR timer is by-passed after Stop Mode Recovery (typical for an external clock and RC/LC oscillators with fast start up times).

HALT. Turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupt IRQ0, IRQ1, and IRQ2 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT. In order to enter STOP or HALT Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, you must execute a NOP (Opcode = FFh) immediately before the appropriate sleep instruction, that is:

from STOP mode when programmed as analog inputs. When the Stop Mode Recovery sources are selected in this register then SMR2 register bits D0, D1 must be set to zero.

Note: *If the Port 2 pin is configured as an output, this output level will be read by the SMR circuitry.*

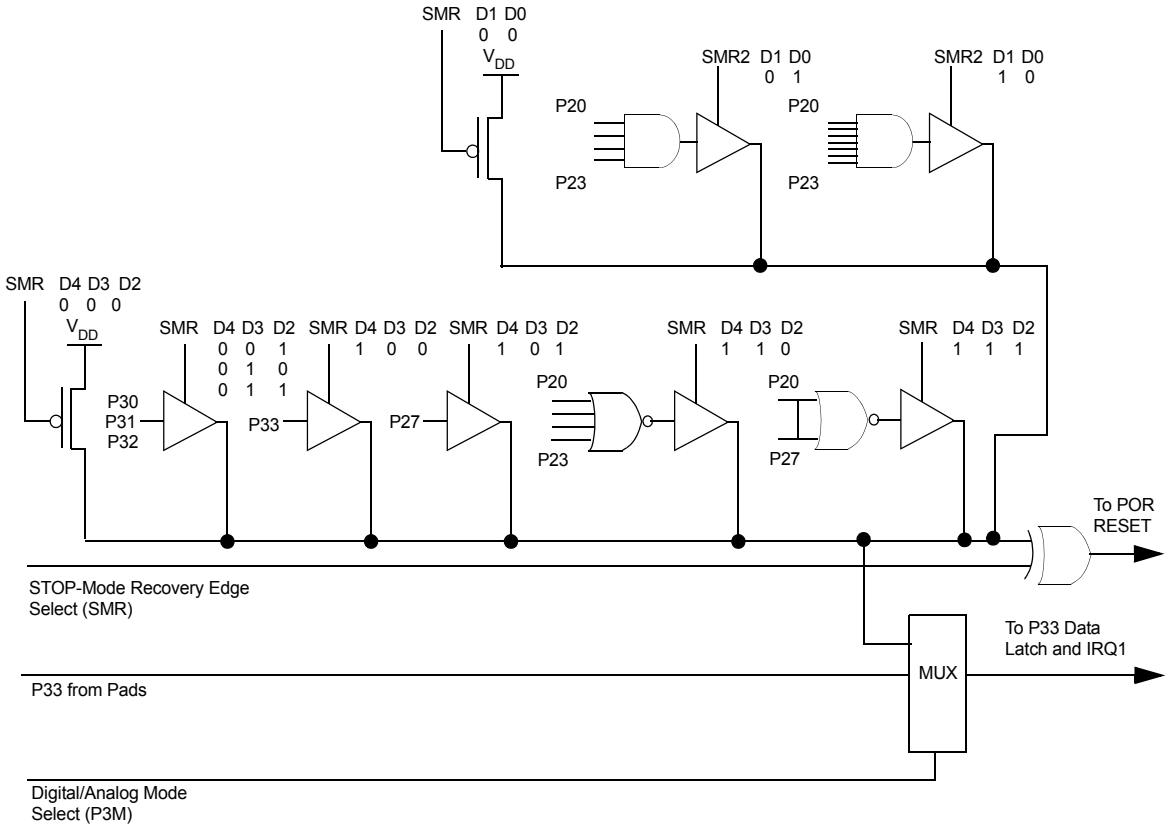


Figure 32. Stop Mode Recovery Source

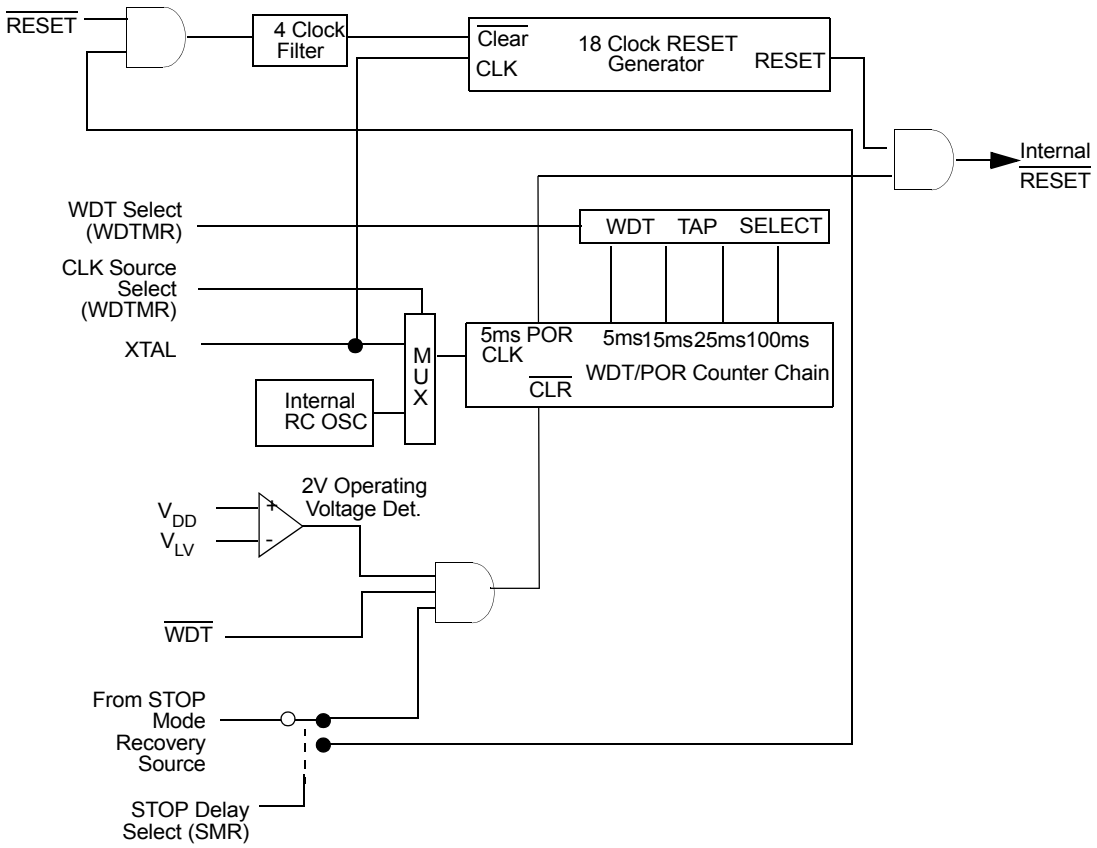


Figure 34. Resets and WDT

Auto Reset Voltage. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. Reset is globally driven if V_{CC} is below VLV (Figure 35).

Z8 Control Register Diagrams

Ordering Information

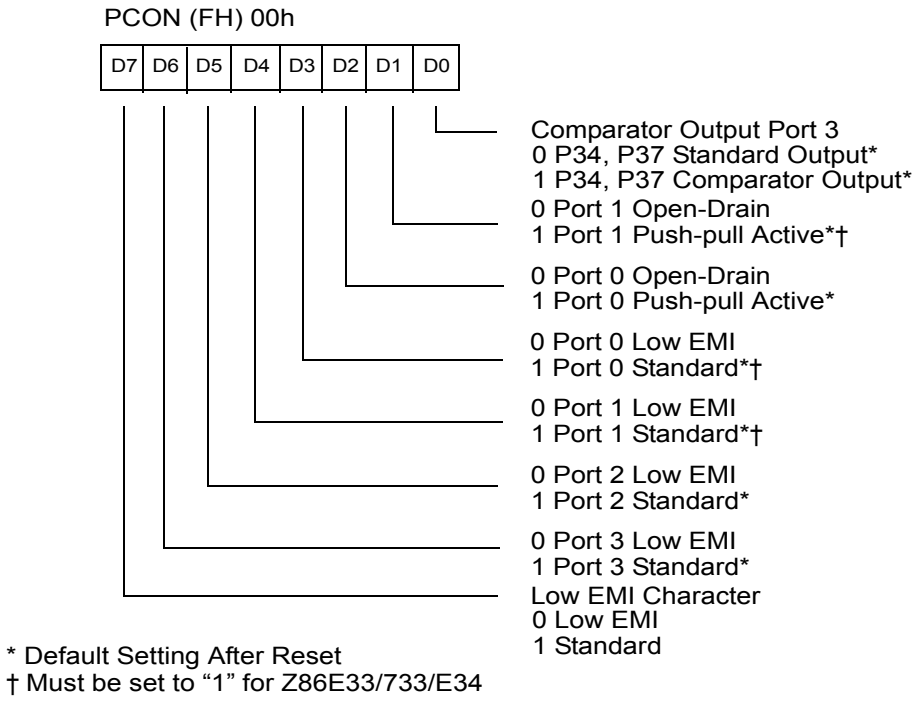


Figure 36. Port Configuration Register (PCON) (Write Only)

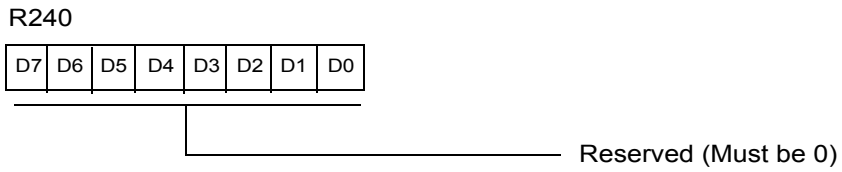


Figure 40. Reserved

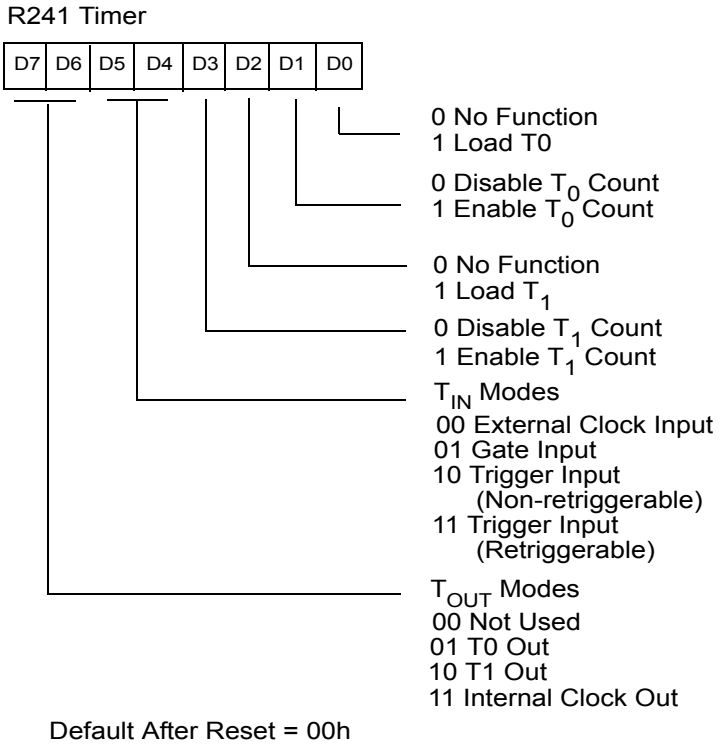


Figure 41. Timer Mode Register ($F1_h$: Read/Write)

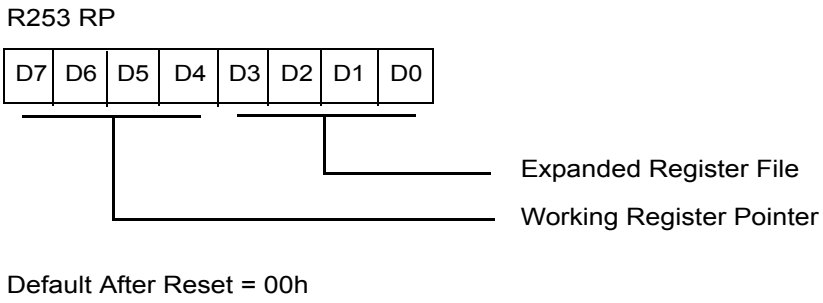


Figure 53. Register Pointer (FD_h: Read/Write)

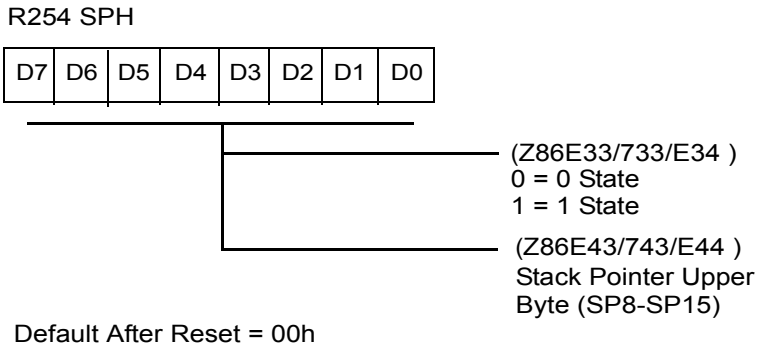


Figure 54. Stack Pointer High (FE_h: Read/Write)

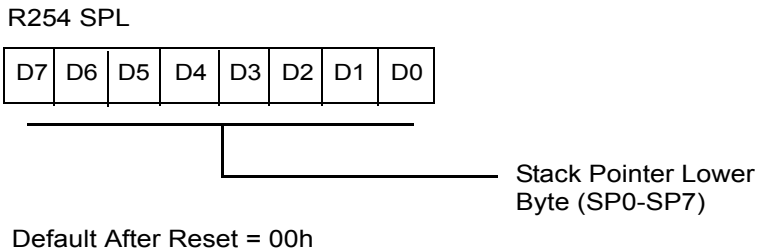
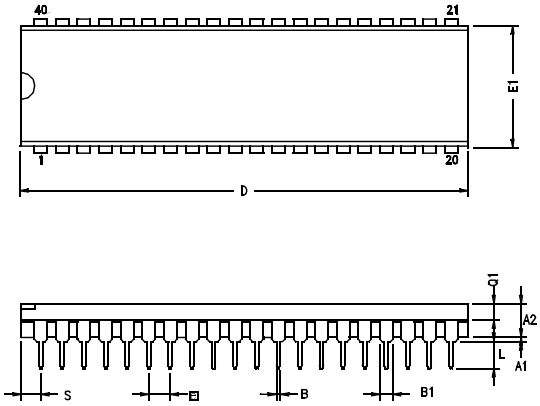


Figure 55. Stack Pointer Low (FF_h: Read/Write)

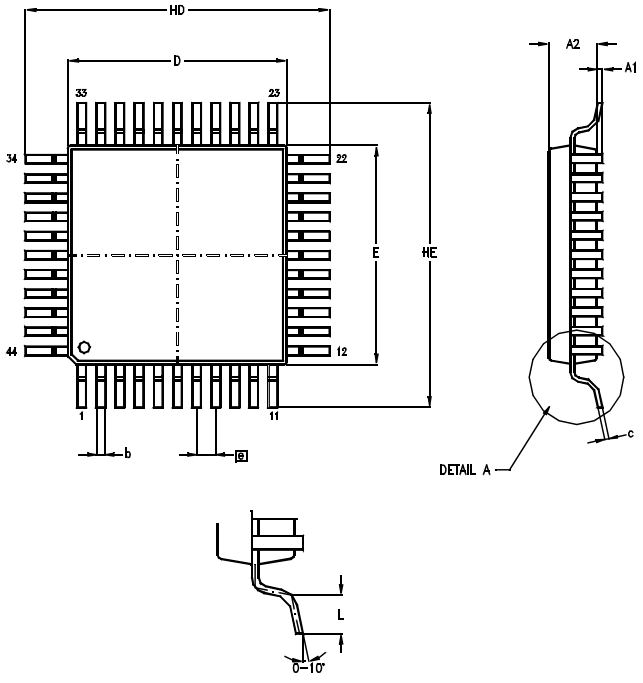
Package Information



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	1.02	.020	.040
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.40	1.91	.055	.075
S	1.52	2.29	.060	.090

CONTROLLING DIMENSIONS : INCH

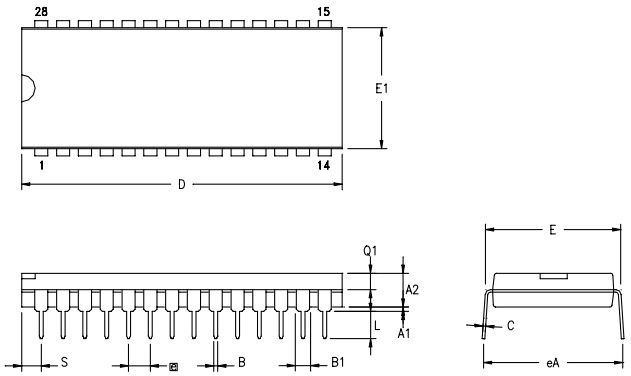
Figure 56. 40-PIN DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.15	.539	.557
D	9.90	10.10	.390	.398
HE	13.70	14.15	.539	.557
E	9.90	10.10	.390	.398
e	0.80 BSC		.0315 BSC	
L	0.60	1.20	.024	.047

NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 .004"

Figure 57. 44-PIN LQFP Package Diagram

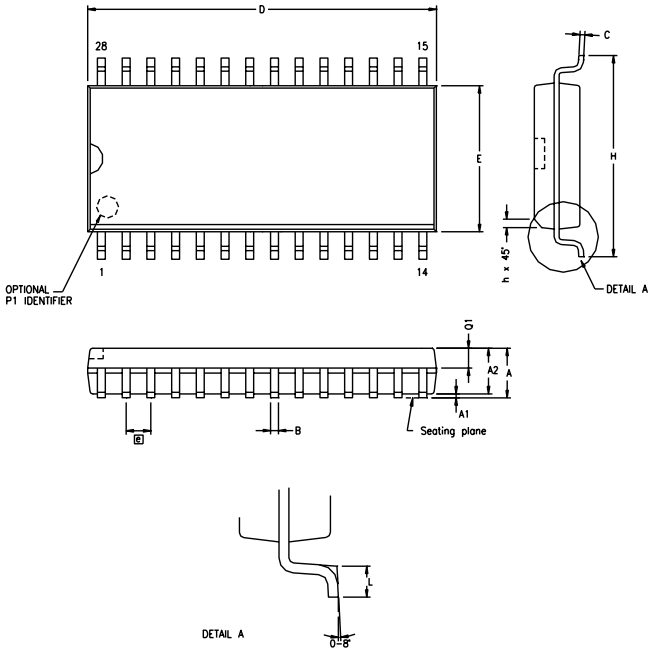


SYMBOL	OPT #	MILLIMETER		INCH	
		MIN	MAX	MIN	MAX
A1		0.38	1.02	.015	.040
A2		3.18	4.19	.125	.165
B		0.38	0.53	.015	.021
B1	01	1.40	1.65	.055	.065
	02	1.14	1.40	.045	.055
C		0.23	0.38	.009	.015
D	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
e		2.54 TYP		.100 TYP	
eA		15.49	16.76	.610	.660
L		3.05	3.81	.120	.150
Q1	01	1.40	1.91	.055	.075
	02	1.40	1.78	.055	.070
S	01	1.52	2.29	.060	.090
	02	1.02	1.52	.040	.060

CONTROLLING DIMENSIONS : INCH

OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

Figure 58. 28-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.64	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	17.78	18.00	.700	.710
E	7.40	7.60	.291	.299
e	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.71	.012	.028
L	0.61	1.00	.024	.039
Q1	0.97	1.09	.038	.043

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 59. 28-Pin SOIC Package Diagram