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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	EBI/EMI
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e3312ssg

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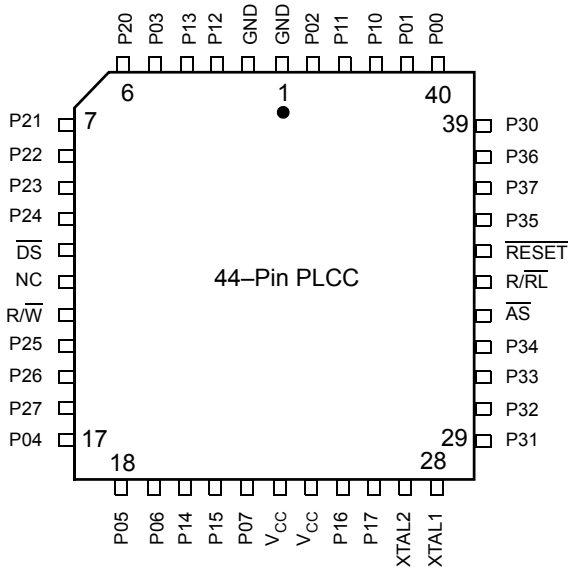

Figure 4. 44-Pin PLCC Pin Configuration Standard Mode

Table 3. 44-Pin PLCC Pin Identification

Pin No	Symbol	Function	Direction
1-2	GND	Ground	
3-4	P12-P13	Port 1, Pins 2,3	Input/Output
5	P03	Port 0, Pin 3	Input/Output
6-10	P20-P24	Port 2, Pins 0,1,2,3,4	Input/Output
11	DS	Data Strobe	Output
12	NC	No Connection	
13	R/$\overline{W}$	Read/Write	Output
14-16	P25-P27	Port 2, Pins 5,6,7	Input/Output
17-19	P04-P06	Port 0, Pins 4,5,6	Input/Output
20-21	P14-P15	Port 1, Pins 4,5	Input/Output
22	P07	Port 0, Pin 7	Input/Output
23-24	V_{CC}	Power Supply	
25-26	P16-P17	Port 1, Pins 6,7	Input/Output

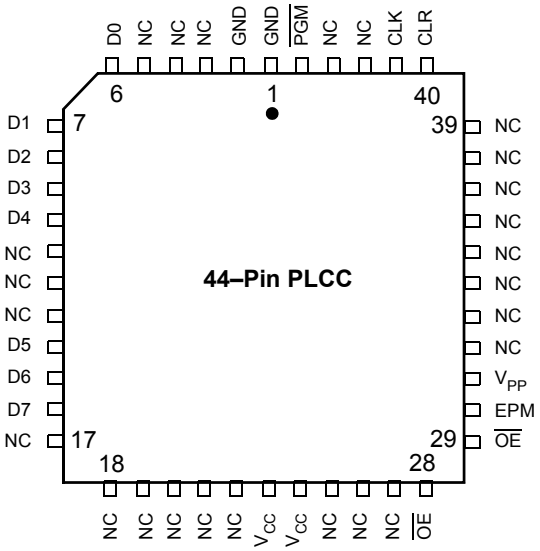

Figure 7. 44-Pin PLCC Pin Configuration EPROM Programming Mode

Table 6. 44-Pin PLCC Pin Configuration EPROM Programming Mode

Pin No	Symbol	Function	Direction
1-2	GND	Ground	
3-5	NC	No Connection	
6-10	D0-D4	Data 0,1,2,3,4	Input/Output
11-13	NC	No Connection	
14-16	D5-D7	Data 5,6,7	Input/Output
17-22	NC	No Connection	
23-24	V_{CC}	Power Supply	
25-27	NC	No Connection	
28	CE	Chip Select	Input
29	OE	Output Enable	Input
30	EPM	EPROM Prog. Mode	Input
31	V_{PP}	Prog. Voltage	Input

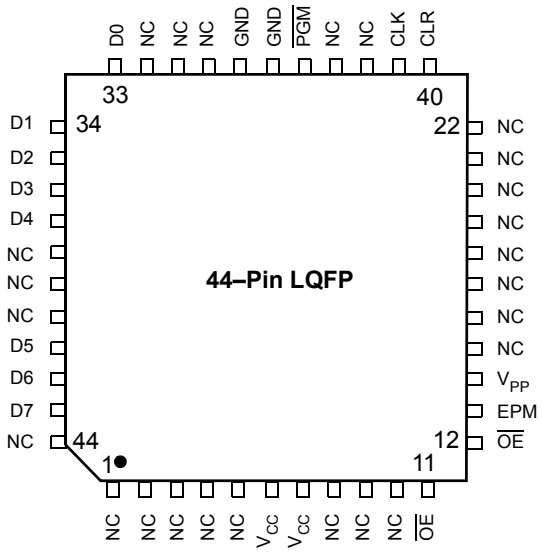

Figure 8. 44-Pin LQFP Pin Configuration EPROM Programming Mode

Table 7. 44-Pin LQFP Pin Identification EPROM Programming Mode

Pin No	Symbol	Function	Direction
1-5	NC	No Connection	
6-7	V_{CC}	Power Supply	
8-10	NC	No Connection	
11	CE	Chip Select	Input
12	OE	Output Enable	Input
13	EPM	EPROM Prog. Mode	Input
14	V_{PP}	Prog. Voltage	Input
15-22	NC	No Connection	
23	CLR	Clear	Input
24	CLK	Clock	Input
25-26	NC	No Connection	
27	/PGM	Prog. Mode	Input
28-29	GND	Ground	
30-32	NC	No Connection	

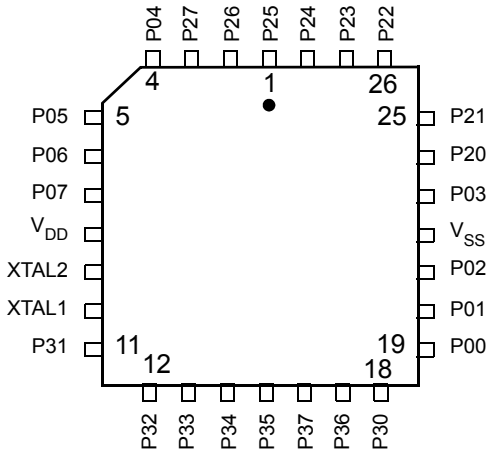

Figure 10. Standard Mode 28-Pin PLCC Pin Configuration

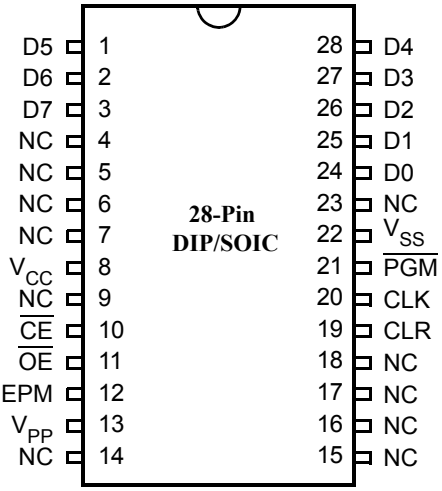

Figure 11. EPROM Programming Mode 28-Pin DIP/SOIC Pin Configuration

Electrical Characteristics

Absolute Maximum Ratings

Table 10. Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
Ambient Temperature under Bias	–40	+105	C	
Storage Temperature	–65	+150	C	
Voltage on any Pin with Respect to V_{SS}	–0.6	+7	V	1
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V	
Voltage on XTAL1, P32, P33 and $\overline{\text{RESET}}$ Pins with Respect to V_{SS}	–0.6	V_{DD}+1	V	2
Total Power Dissipation		1.21	W	
Maximum Allowable Current out of V_{SS}		220	mA	
Maximum Allowable Current into V_{DD}		180	mA	
Maximum Allowable Current into an Input Pin	–600	+600	µA	3
Maximum Allowable Current into an Open-Drain Pin	–600	+600	µA	4
Maximum Allowable Output Current Sunk by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sourced by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sunk by $\overline{\text{RESET}}$ Pin		3	mA	

Notes
1. This applies to all pins except XTAL pins and where otherwise noted.
2. There is no input protection diode from pin to V_{DD}.
3. This excludes XTAL pins.
4. Device pin is not at an output Low state.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Table 11. DC Electrical Characteristics T_A = 0 °C to +70 °C (Continued)

Symbol	Parameter	V_{CC}[1]	Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{OFFSET}	Comparator Input Offset Voltage	3.5V		25	10	mV		
		5.5V		25	10	mV		
V_{ICR}	Input Common Mode Voltage Range	3.5V	0	V_{CC} -1.0V		V		4
		5.5V	0	V_{CC} -1.0V		V		4
I_{IL}	Input Leakage	3.5V	-1	2	0.032	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	2	0.032	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.5V	-1	2	0.032	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	2	0.032	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	3.5V	-20	-130	-65	µA		
		5.5V	-20	-180	-112	µA		
I_{CC}	Supply Current	3.5V		15	5	mA	@ 12 MHz	5,6
		5.5V		20	15	mA	@ 12 MHz	5,6
I_{CC1}	Standby Current HALT Mode	3.5V		4	2	mA	V_{IN} = 0V, V_{CC} @ 12 MHz	5,6
		5.5V		6	4	mA		5,6
		3.5V		3	1.5	mA	Clock Divide by 16 @ 12 MHz	5,6
		5.5V		5	3	mA		5,6
I_{CC2}	Standby Current STOP Mode	3.5V		10	2	µA	V_{IN} = 0V, V_{CC}	7,8,9
		5.5V		10	3	µA	V_{IN} = 0V, V_{CC}	7,8,9
		3.5V		15	7	µA	V_{IN} = 0V, V_{CC}	7,8
		5.5V		30	10	µA	V_{IN} = 0V, V_{CC}	7,8
I_{ALL}	Auto Latch Low Current	3.0V	0.7	8	2.4	µA	0V < V_{IN} < V_{CC}	10
		5.5V	1.4	15	4.7	µA	0V < V_{IN} < V_{CC}	10
I_{ALH}	Auto Latch High Current	3.5V	-0.6	-5	-1.8	µA	0V < V_{IN} < V_{CC}	10
		5.5V	-1	-8	-3.8	µA	0V < V_{IN} < V_{CC}	10

Table 12. DC Electrical Characteristics T_A= -40 °C to +105 °C (Continued)

Symbol	Parameter	V_{CC} [1]	Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{OH1}	Output High Voltage	4.5V	V_{CC} -0.4		4.8	V	I_{OH} = -2.0 mA	2
		5.5V	V_{CC} -0.4		4.8	V	I_{OH} = -2.0 mA	2
V_{OL}	Output Low Voltage Low EMI Mode	4.5V		0.4	0.2	V	I_{OL} = 1.0 mA	
		5.5V		0.4	0.2	V	I_{OL} = 1.0 mA	
V_{OL1}	Output Low Voltage	4.5V		0.4	0.1	V	I_{OL} = +4.0 mA	2
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	2
V_{OL2}	Output Low Voltage	4.5V		1.2	0.5	V	I_{OL} = +12 mA	2
		5.5V		1.2	0.5	V	I_{OL} = +12 mA	2
V_{RH}	Reset Input High Voltage	4.5V	.8 V_{CC}	V_{CC}	1.7	V		3
		5.5V	.8 V_{CC}	V_{CC}	2.1	V		3
V_{OLR}	Reset Output Low Voltage	4.5V		0.6	0.3	V	I_{OL} = 1.0 mA	3
		5.5V		0.6	0.2	V	I_{OL} = 1.0 mA	3
V_{OFFSET}	Comparator Input Offset Voltage	4.5V		25	10	mV		
		5.5V		25	10	mV		
V_{ICR}	Input Common Mode Voltage Range	4.5V	0	V_{CC} -1.5V		V		4
		5.5V	0	V_{CC} -1.5V		V		4
I_{IL}	Input Leakage	4.5V	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	4.5V	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	4.5V	-18	-180	-112	µA		3
		5.5V	-18	-180	-112	µA		3
I_{CC}	Supply Current	4.5V		20	15	mA	@ 12 MHz	5,6
		5.5V		20	15	mA	@ 12 MHz	5,6
I_{CC1}	Standby Current HALT Mode	4.5V		6	2	mA	V_{IN} = 0V, V_{CC} @ 12 MHz	5,6
		5.5V		6	4	mA	V_{IN} = 0V, V_{CC} @ 12 MHz	5,6

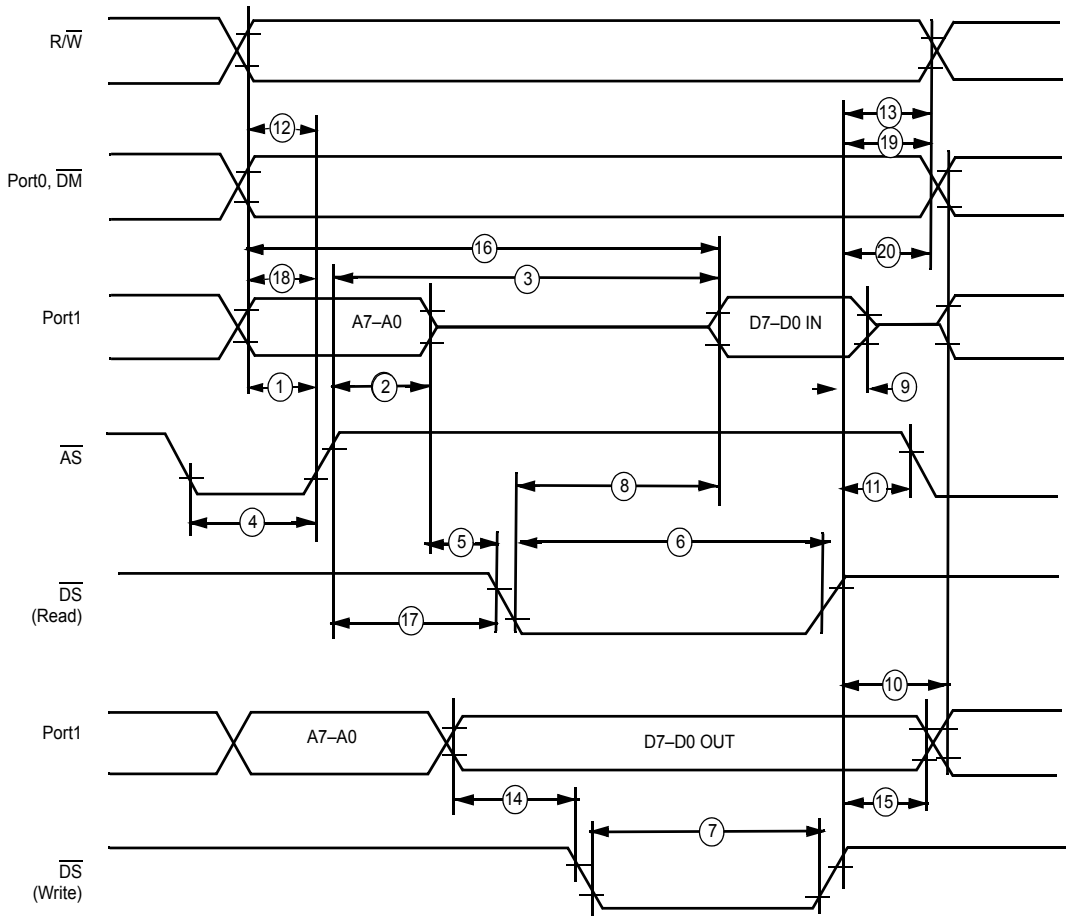

Figure 14. External I/O or Memory Read/Write Timing (Z86E43/743/E44 Only)

Table 13. DC Electrical Characteristics T_A = 0 °C to +70 °C, 12 MHz

No.	Symbol	Parameter	V_{CC} [1]	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to $\overline{AS}$ Rise Delay	3.5V	35		ns	2
			5.5V	35		ns	2
2	TdAS(A)	$\overline{AS}$ Rise to Address Float Delay	3.5V	45		ns	2
			5.5V	45		ns	2
3	TdAS(DR)	$\overline{AS}$ Rise to Read Data Req'd Valid	3.5V		250	ns	2,3
			5.5V		250	ns	2,3

CLR Clear (active High). This pin resets the internal address counter at the High Level.

CLK Address Clock. This pin is a clock input. The internal address counter increases by one for each clock cycle.

Application Precaution

The production test-mode environment may be enabled accidentally during normal operation if excessive noise surges above V_{CC} occur on pins P31 and $\overline{\text{RESET}}$.

In addition, processor operation of Z8 OTP devices may be affected by excessive noise surges on the V_{PP}, EPM, $\overline{\text{OE}}$ pins while the microcontroller is in Standard Mode.

Recommendations for dampening voltage surges in both test and OTP mode include the following:

- Using a clamping diode to V_{CC}
- Adding a capacitor to the affected pin
- Enable EPROM/Test Mode Disable OTP option bit.

Standard Mode

XTAL Crystal 1 (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC, RC network, or external single-phase clock to the on-chip oscillator input.

XTAL2 Crystal 2 (time-based output). This pin connects a parallel-resonant crystal, ceramic resonator, LC, or RC network to the on-chip oscillator output.

R/$\overline{\text{W}}$ Read/Write (output, write Low). The R/$\overline{\text{W}}$ signal is Low when the CCP is writing to the external program or data memory (Z86E43/743/E44 only).

$\overline{\text{RESET}}$ Reset (input, active Low). Reset will initialize the MCU. Reset is accomplished either through Power-On, Watchdog Timer reset, Stop Mode Recovery, or external reset. During Power-On Reset and Watchdog Timer Reset, the internally generated reset drives the reset pin low for the POR time. Any devices driving the reset line must be open-drain in order to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally. After the POR time, $\overline{\text{RESET}}$ is a Schmitt-triggered input. ($\overline{\text{RESET}}$ is available on Z86E43/743/E44 only.)

To avoid asynchronous and noisy reset problems, the Z86E43/743/E44 is equipped with a reset filter of four external clocks (4TpC). If the external reset signal is less than 4TpC in duration, no reset occurs. On the fifth clock after the reset is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external reset, whichever is longer. During the reset cycle, $\overline{\text{DS}}$ is held active Low while $\overline{\text{AS}}$ cycles at a rate of TpC/2. Program execution begins at location 000CH, 5-10 TpC cycles after $\overline{\text{RESET}}$ is released. For Power-On Reset, the reset output time is 5 ms.

The Z86E43/743/E44 does not reset WDTMR, SMR, P2M, and P3M registers on a Stop-Mode Recovery operation.

$\overline{\text{ROMless}}$ (input, active Low). This pin, when connected to GND, disables the internal ROM and forces the device to function as a Z86C90/C89 ROMless Z8. (Note that, when left unconnected or pulled High to V_{CC}, the device functions nor

Note: *When using in ROM Mode in High EMI (noisy) environment, the ROMless pins should be connected directly to V_{CC}.*

$\overline{\text{DS}}$ (output, active Low). Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of $\overline{\text{DS}}$. For WRITE operations, the falling edge of $\overline{\text{DS}}$ indicates that output data is valid.

$\overline{\text{AS}}$ (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle for external memory transfer. Address output is from Port 0/Port 1 for all external programs. Memory address transfers are valid at the trailing edge of $\overline{\text{AS}}$. Under program control, $\overline{\text{AS}}$ is placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

Port 0 (P07-P00). Port 0 is an 8-bit, bidirectional, CMOS-compatible I/0 port. These eight I/O lines can be configured under software control as a nibble I/0 port, or as an address port for interfacing external memory. The input buffers are Schmitt-triggered and nibble programmed. Either nibble output that can be globally programmed as push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 0 can be placed under handshake control. In Handshake Mode, Port 3 lines P32 and P35 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to Port 0's upper nibble. The lower nibble must have the same direction as the upper nibble.

For external memory references, Port 0 provides address bits A11-A8 (lower nibble) or Al 5-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. In ROMless mode, after a hardware reset, Port 0 is configured as address lines Al 5-A8, and extended timing is set to accommodate slow memory access. The initialization routine can include re-configuration to eliminate this extended timing mode. In ROM mode, Port 0 is defined as input after reset.

Port 0 can be set in the High-Impedance Mode if selected as an address output state, along with Port 1 and the control signals $\overline{\text{AS}}$, $\overline{\text{DS}}$, and R/$\overline{\text{W}}$ (Figure 18).

Functional Description

The MCU incorporates the following special functions to enhance the standard Z8 architecture to provide the user with increased design flexibility.

RESET. The device is reset in one of three ways:

1. Power-On Reset
2. Watchdog Timer
3. Stop Mode Recovery Source

Note: *Having the Auto Power-On Reset circuitry built-in, the MCU does not need to be connected to an external power-on reset circuit. The reset time is T_{POR}. The MCU does not re-initialize WDTMR, SMR, P2M, and P3M registers to their reset values on a Stop Mode Recovery operation.*

Note: *The device V_{CC} must rise up to the operating V_{CC} specification before the T_{POR} expires.*

Program Memory. The MCU can address up to 4/8/16 KB of Internal Program Memory (see Figure 22). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For EPROM mode, byte 12 (000Ch) to address 4095 (0FFFh)/8191 (1FFFh)/16384 (3FFFh), consists of programmable EPROM. After reset, the program counter points at the address 000Ch, which is the starting address of the user program.

In ROMless mode, the Z86E43/743/E44 can address up to 64 KB of External Program Memory. The ROM/ROMless option is only available on the 44-pin devices.

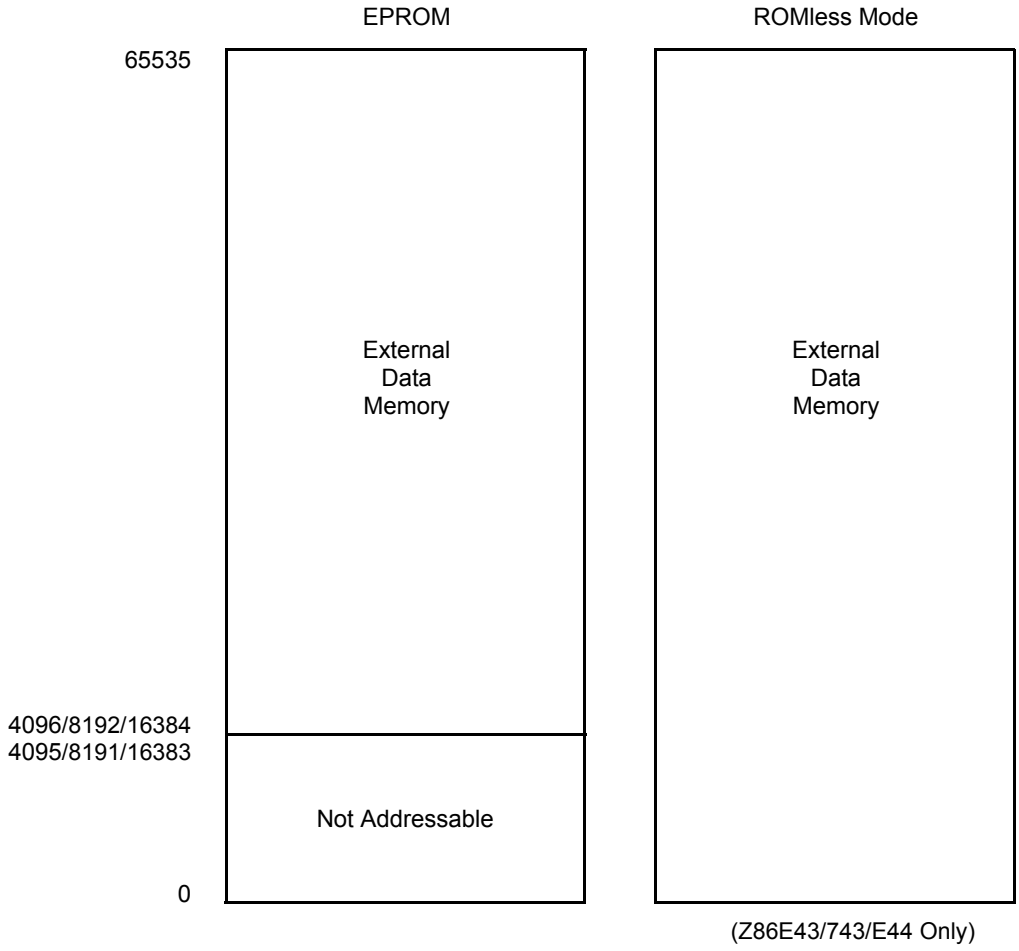

Figure 23. Data Memory Map

Register File. The register file consists of three I/O port registers, 236/125 general-purpose registers, 15 control and status registers, and three system configuration registers in the expanded register group. The instructions can access registers directly or indirectly through an 8-bit address field. This allows a short 4-bit register address using the Register Pointer (see Figure 24). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

Note: *Register Group E0-EF can only be accessed through working register and indirect addressing modes.*

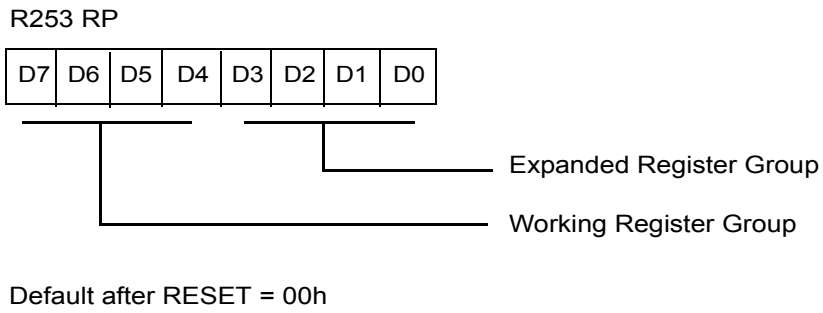

Figure 24. Register Pointer Register

Expanded Register File (ERF). The register file has been expanded to allow for additional system control registers, mapping of additional peripheral devices and input/output ports into the register address area. The Z8 register address space RO through R15 is implemented as 16 groups of 16 registers per group (see Figure 26). These register banks are known as the Expanded Register File (ERF).

The low nibble (D3-D0) of the Register Pointer (RP) select the active ERF Bank, and the high nibble (D7-D4) of register RP select the working register group. Three system configuration registers reside in the Expanded Register File at bank FH: PCON, SMR, and WDTMR. The rest of the Expanded Register is not physically implemented and is reserved for future expansion.

RAM Protect. The upper portion of the RAM's address spaces 80h to EFh (excluding the control registers) can be protected from reading and writing. This option can be selected during the EPROM Programming Mode. After this option is selected, the user can activate this feature from the internal EPROM. D6 of the IMR control register (R251) is used to turn off/on the RAM protect by loading a 0 or 1, respectively. A "1" in D6 indicates RAM Protect enabled.

Stack. The Z86E43/743/E44 external data memory or the internal register file can be used for the stack. The 16-bit Stack Pointer (R254-R255) is used for the external stack, which can reside anywhere in the data memory for ROMless mode, but only from 4096/8192/16384 to 65535 in ROM mode. An 8-bit Stack Pointer (R255) is used for the internal stack on the Z8 that resides within the 236 general-purpose registers (R4-R239). SPH (R254) can be used as a general-purpose register when using internal stack only. R254 and R255 are set to 00H after any reset or Stop Mode Recovery.

Counter/Timers. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The Ti prescaler is driven by internal or external clock sources; however, the TO prescaler is driven by the internal clock only (see Figure 27).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256), that has been loaded into the counter. When the counter reaches the end of count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counters can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching one (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, can be read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3 line P36 serves as a timer output (T_{OUT}) through which T0, T1, or the internal clock can be output. The counter/timers can be cascaded by connecting the T0 output to the input of T1.

from STOP mode when programmed as analog inputs. When the Stop Mode Recovery sources are selected in this register then SMR2 register bits D0, D1 must be set to zero.

Note: *If the Port 2 pin is configured as an output, this output level will be read by the SMR circuitry.*

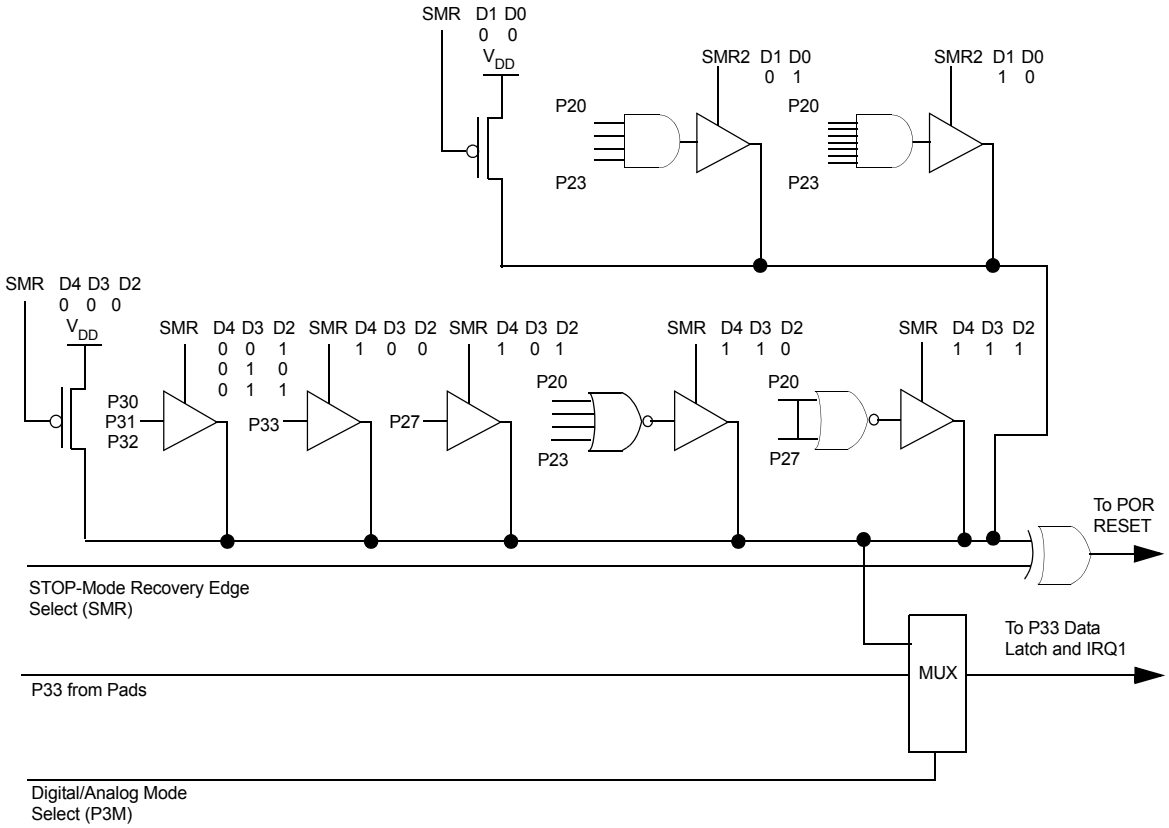

Figure 32. Stop Mode Recovery Source

Table 22. Stop Mode Recovery Source

D4	D3	D2	SMR Source selection
0	0	0	POR recovery only
0	0	1	P30 transition
0	1	0	P31 transition (Not in analog mode)
0	1	1	P32 transition (Not in analog mode)
1	0	0	P33 transition (Not in analog mode)
1	0	1	P27 transition
1	1	0	Logical NOR of Port 2 bits 0-3
1	1	1	Logical NOR of Port 2 bits 0-7

Stop Mode Recovery Delay Select (D5). The 5 ms RESET delay after Stop Mode Recovery is disabled by programming this bit to a zero. A "1" in this bit will cause a 5 ms RESET delay after Stop Mode Recovery. The default condition of this bit is 1. If the fast wake up mode is selected, the Stop Mode Recovery source needs to be kept active for at least 5TpC.

Stop Mode Recovery Level Select (D6). A "1" in this bit defines that a high level on any one of the recovery sources wakes the MCU from STOP Mode. A 0 defines low level recovery. The default value is 0.

Cold or Warm Start (D7). This bit is set by the device upon entering STOP Mode. A "0" in this bit indicates that the device has been reset by POR (cold). A "1" in this bit indicates the device was awakened by a SMR source (warm).

Stop Mode Recovery Register 2 (SMR2). This register contains additional Stop Mode Recovery sources. When the Stop Mode Recovery sources are selected in this register then SMR Register Bits D2, D3, and D4 must be 0.

SMR:10		Operation
D1	DO	Description of Action
0	0	POR and/or external reset recovery
0	1	Logical AND of P20 through P23
1	0	Logical AND of P20 through P27

Watchdog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is disabled after Power-On

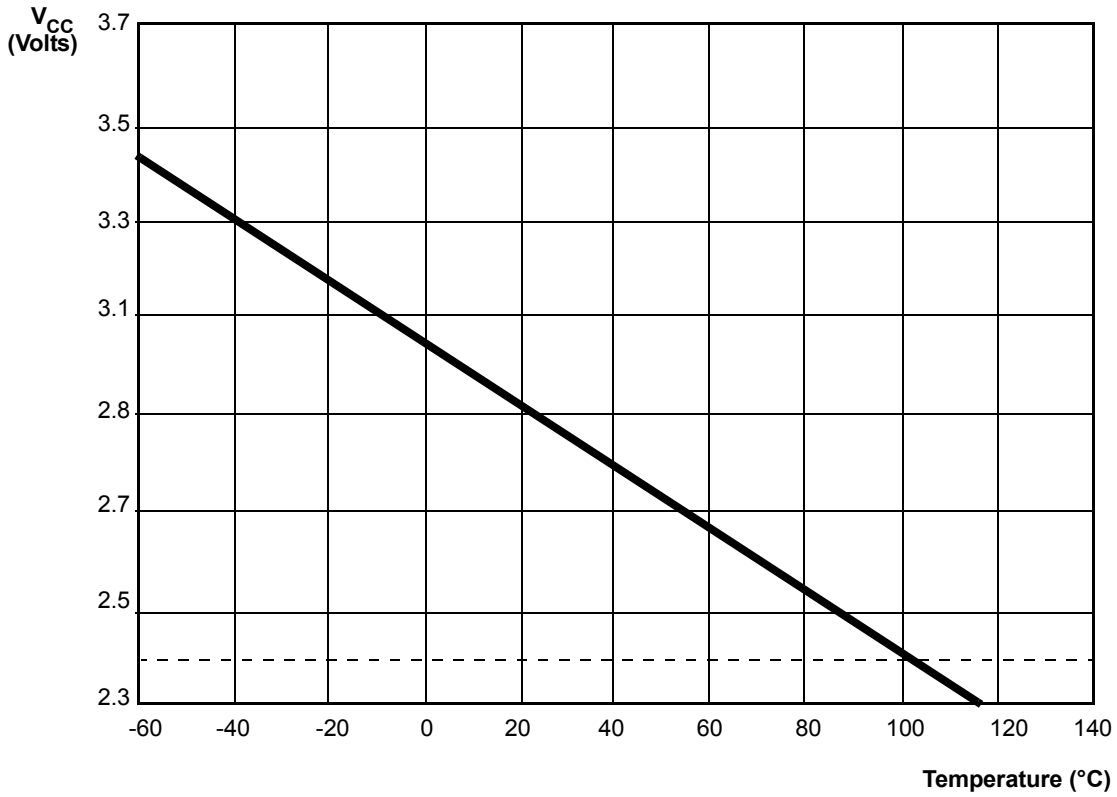

Figure 35. Typical V_{LV} Voltage vs. Temperature

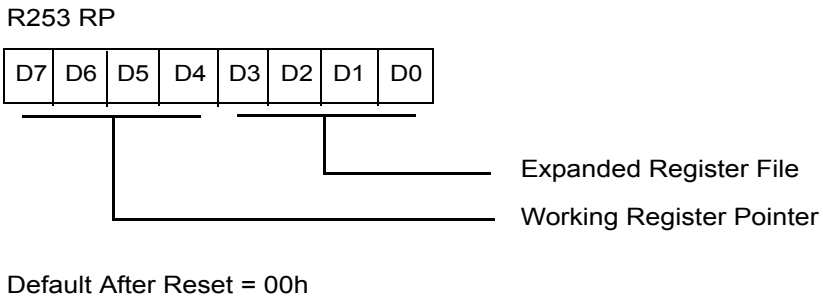

Figure 53. Register Pointer (FD_h: Read/Write)

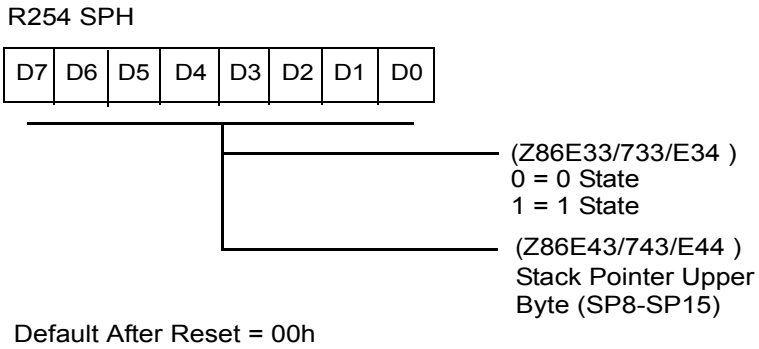

Figure 54. Stack Pointer High (FE_h: Read/Write)

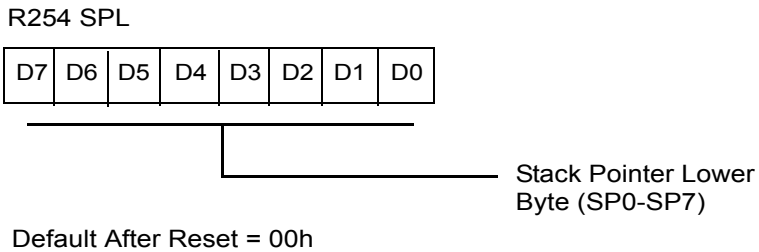

Figure 55. Stack Pointer Low (FF_h: Read/Write)

Ordering Information

Table 24.Ordering Information

Product	Speed (MHz)	Package Type	Pin Count
Z86E3312PSC	12	PDIP	28
Z86E3312SCC	12	SOIC	28
Z86E3312PSC	12	PLCC	28
Z86E3412PEC	12	PDIP	28
Z86E3412PSC	12	PDIP	28
Z86E3412SSC	12	SOIC	28
Z86E3412VSC	12	PLCC	28
Z86E4312FSC	12	LQFP	44
Z86E4312PSC	12	PDIP	40
Z86E4312VSC	12	PLCC	44
Z86E4412FSC	12	LQFP	44
Z86E4412PEC	12	PDIP	40
Z86E4412PSC	12	PDIP	40
Z86E4412VSC	12	PLCC	44
Z8673312PSC	12	PDIP	28
Z8673312SSC	12	SOIC	28
Z8673312VSC	12	PLCC	28
Z8674312FSC	12	LQFP	44
Z8674312PSC	12	PDIP	40
Z8674312VSC	12	PLCC	44