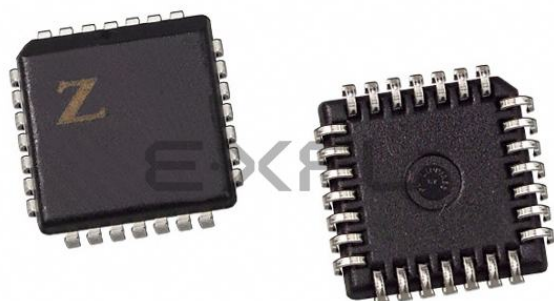




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Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	EBI/EMI
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e3312vsc

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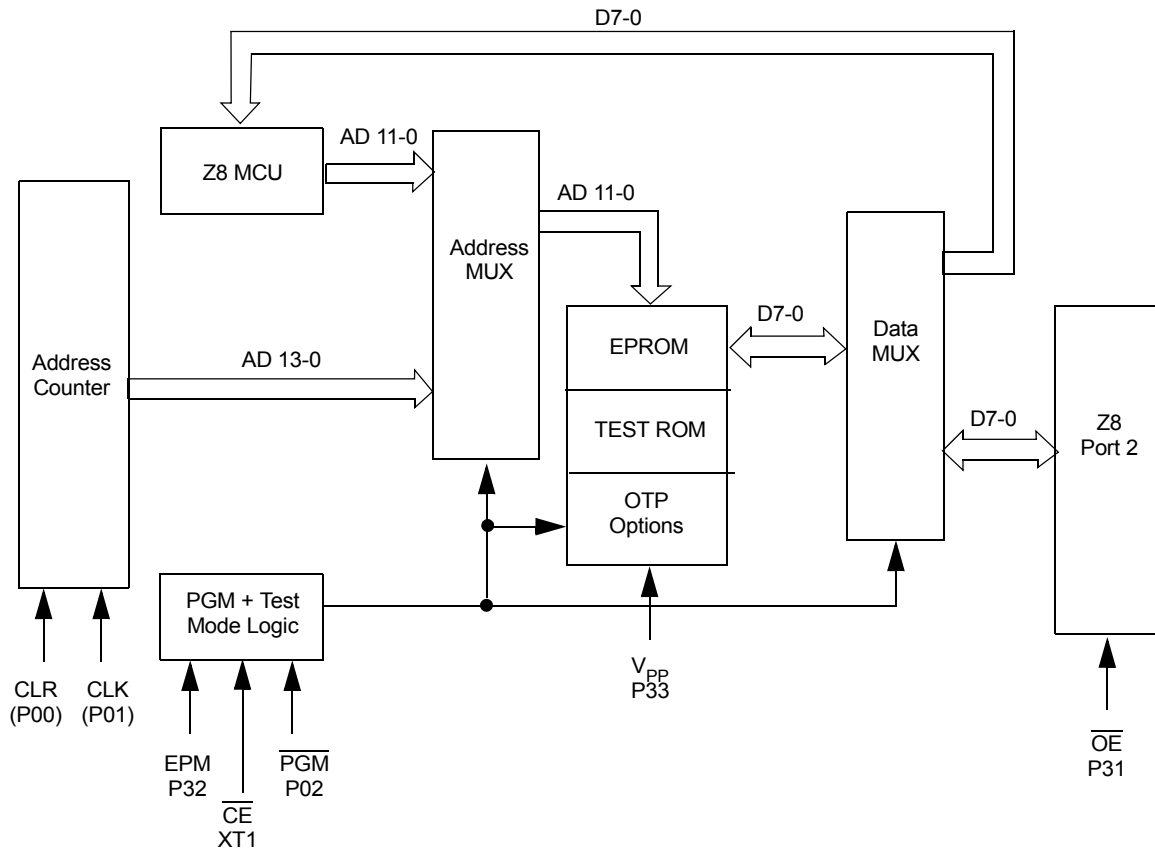
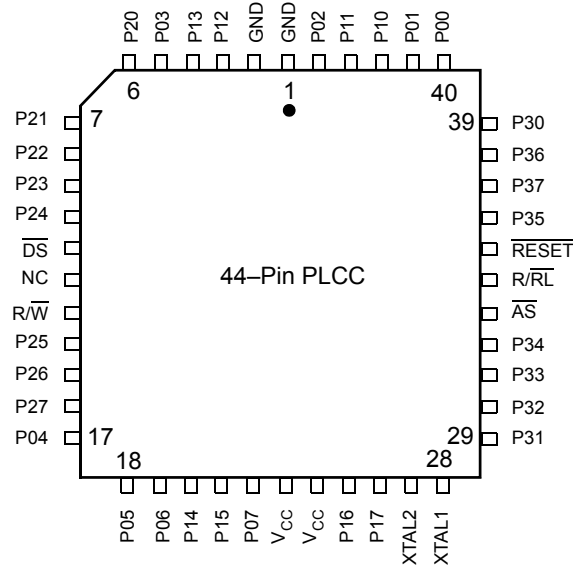


Figure 2. EPROM Programming Block Diagram

Table 2. 40-Pin DIP Pin Identification Standard Mode (Continued)

Pin No	Symbol	Function	Direction
15	XTAL1	Crystal Oscillator	Input
16-18	P31-P33	Port 3, Pins 1,2,3	Input
19	P34	Port 3, Pin 4	Output
20	AS	Address Strobe	Output
21	RESET	Reset	Input
22	P35	Port 3, Pin 5	Output
23	P37	Port 3, Pin 7	Output
24	P36	Port 3, Pin 6	Output
25	P30	Port 3, Pin 0	Input
26-27	P00-P01	Port 0, Pins 0,1	Input/Output
28-29	P10-P11	Port 1, Pins 0,1	Input/Output
30	P02	Port 0, Pin 2	Input/Output
31	GND	Ground	
32-33	P12-P13	Port 1, Pins 2,3	Input/Output
34	P03	Port 0, Pin 3	Input/Output
35-39	P20-P24	Port 2, Pins 0, 1,2,3,4	Input/Output
40	DS	Data Strobe	Output



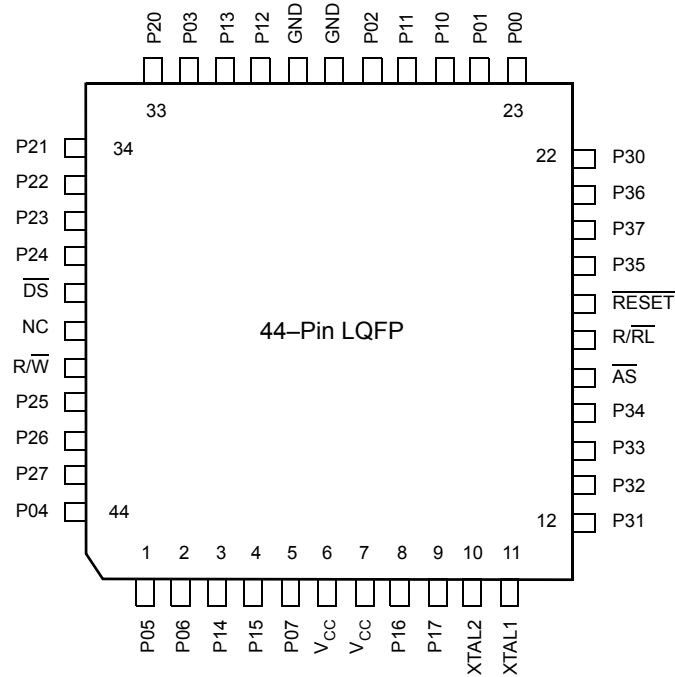


Figure 5. 44-Pin LQFP Pin Configuration Standard Mode

Table 4. 44-Pin LQFP Pin Identification

Pin No	Symbol	Function	Direction
1-2	P05-P06	Port 0, Pins 5,6	Input/Output
3-4	P14-P15	Port 1, Pins 4,5	Input/Output
5	P07	Port 0, Pin 7	Input/Output
6-7	V _{CC}	Power Supply	
8-9	P16-P17	Port 1, Pins 6,7	Input/Output
10	XTAL2	Crystal Oscillator	Output
11	XTAL1	Crystal Oscillator	Input
12-14	P31-P33	Port 3, Pins 1,2,3	Input
15	P34	Port 3, Pin 4	Output
16	AS	Address Strobe	Output
17	R//RL	ROM/ROMless select	Input

Table 4. 44-Pin LQFP Pin Identification (Continued)

Pin No	Symbol	Function	Direction
18	RESET	Reset	Input
19	P35	Port 3, Pin 5	Output
20	P37	Port 3, Pin 7	Output
21	P36	Port 3, Pin 6	Output
22	P30	Port 3, Pin 0	Input
23-24	P00-P01	Port 0, Pin 0,1	Input/Output
25-26	P10-P11	Port 1, Pins 0,1	Input/Output
27	P02	Port 0, Pin 2	Input/Output
28-29	GND	Ground	
30-31	P12-P13	Port 1, Pins 2,3	Input/Output
32	P03	Port 0, Pin 3	Input/Output
33-37	P20-24	Port 2, Pins 0,1,2,3,4	Input/Output
38	DS	Data Strobe	Output
39	NC	No Connection	
40	$\overline{R/W}$	Read/Write	Output
41-43	P25-P27	Port 2, Pins 5,6,7	Input/Output
44	P04	Port 0, Pin 4	Input/Output

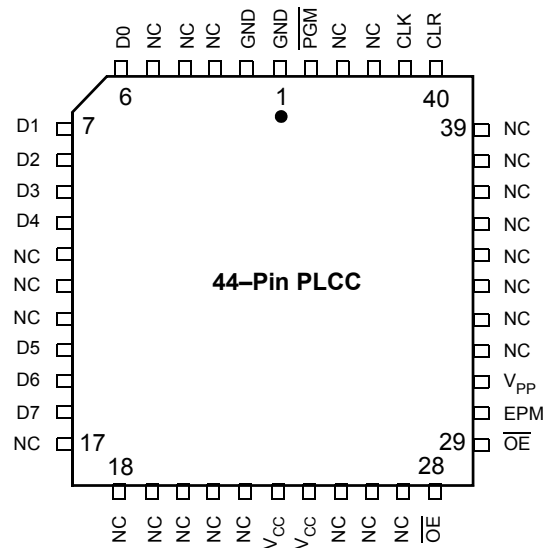


Figure 7. 44-Pin PLCC Pin Configuration EPROM Programming Mode

Table 6. 44-Pin PLCC Pin Configuration EPROM Programming Mode

Pin No	Symbol	Function	Direction
1-2	GND	Ground	
3-5	NC	No Connection	
6-10	D0-D4	Data 0,1,2,3,4	Input/Output
11-13	NC	No Connection	
14-16	D5-D7	Data 5,6,7	Input/Output
17-22	NC	No Connection	
23-24	V _{CC}	Power Supply	
25-27	NC	No Connection	
28	CE	Chip Select	Input
29	OE	Output Enable	Input
30	EPM	EPROM Prog. Mode	Input
31	V _{PP}	Prog. Voltage	Input

**Table 7. 44-Pin LQFP Pin Identification EPROM Programming Mode
(Continued)**

Pin No	Symbol	Function	Direction
33-37	D0-D4	Data 0,1,2,3,4	Input/Output
38-40	NC	No Connection	
41-43	D5-D7	Data 5,6,7	Input/Output
44	NC	No Connection	

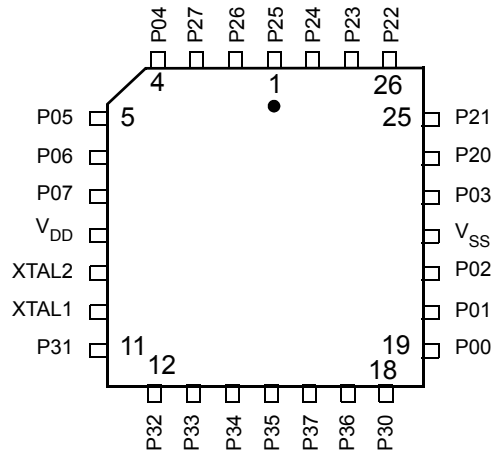


Figure 10. Standard Mode 28-Pin PLCC Pin Configuration

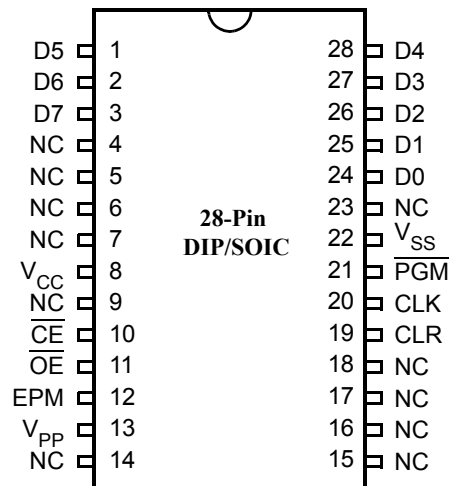


Figure 11. EPROM Programming Mode 28-Pin DIP/SOIC Pin Configuration

Table 11. DC Electrical Characteristics $T_A = 0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$ (Continued)

Symbol	Parameter	V_{CC}^1	Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{OFFSET}	Comparator Input Offset Voltage	3.5V		25	10	mV		
		5.5V		25	10	mV		
V_{ICR}	Input Common Mode Voltage Range	3.5V	0	$V_{CC}-1.0V$		V		4
		5.5V	0	$V_{CC}-1.0V$		V		4
I_{IL}	Input Leakage	3.5V	-1	2	0.032	μA	$V_{IN} = 0V, V_{CC}$	
		5.5V	-1	2	0.032	μA	$V_{IN} = 0V, V_{CC}$	
I_{OL}	Output Leakage	3.5V	-1	2	0.032	μA	$V_{IN} = 0V, V_{CC}$	
		5.5V	-1	2	0.032	μA	$V_{IN} = 0V, V_{CC}$	
I_{IR}	Reset Input Current	3.5V	-20	-130	-65	μA		
		5.5V	-20	-180	-112	μA		
I_{CC}	Supply Current	3.5V		15	5	mA	@ 12 MHz	5,6
		5.5V		20	15	mA	@ 12 MHz	5,6
I_{CC1}	Standby Current HALT Mode	3.5V		4	2	mA	$V_{IN} = 0V, V_{CC}$	5,6
		5.5V		6	4	mA	@ 12 MHz	5,6
		3.5V		3	1.5	mA	Clock Divide by	5,6
		5.5V		5	3	mA	16 @ 12 MHz	5,6
I_{CC2}	Standby Current STOP Mode	3.5V		10	2	μA	$V_{IN} = 0V, V_{CC}$	7,8,9
		5.5V		10	3	μA	$V_{IN} = 0V, V_{CC}$	7,8,9
		3.5V		15	7	μA	$V_{IN} = 0V, V_{CC}$	7,8
		5.5V		30	10	μA	$V_{IN} = 0V, V_{CC}$	7,8
I_{ALL}	Auto Latch Low Current	3.0V	0.7	8	2.4	μA	$0V < V_{IN} < V_{CC}$	10
		5.5V	1.4	15	4.7	μA	$0V < V_{IN} < V_{CC}$	10
I_{ALH}	Auto Latch High Current	3.5V	-0.6	-5	-1.8	μA	$0V < V_{IN} < V_{CC}$	10
		5.5V	-1	-8	-3.8	μA	$0V < V_{IN} < V_{CC}$	10

Table 17. Additional Timing Table (Divide by Two Mode) $T_A = 0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$ (Continued)

No	Symbol	Parameter	V_{CC}^1	Min	Max	Min	Max	Units	Conditions	Notes
4	TwTinL	Timer Input Low Width	3.5V	70		70		ns		2,6,4
			5.5V	70		70		ns		2,6,4
5	TwTinH	Timer Input High Width	3.5V	5TpC		5TpC				2,6,4
			5.5V	5TpC		5TpC				2,6,4
6	TpTin	Timer Input Period	3.5V	8TpC		8TpC				2,6,4
			5.5V	8TpC		8TpC				2,6,4
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.5V		100		100	ns		2,6,4
			5.5V		100		100	ns		2,6,4
8A	TwIL	Int. Request Low Time	3.5V	70		70		ns		2,6,4,5
			5.5V	70		70		ns		2,6,4,5
8B	TwIL	Int. Request Low Time	3.5V	5TpC		5TpC				2,6,4,5
			5.5V	5TpC		5TpC				2,6,4,5
9	TwIH	Int. Request Input High Time	3.5V	5TpC		5TpC				2,6,4,5
			5.5V	5TpC		5TpC				2,6,4,5
10	Twsm	Stop Mode Recovery Width Spec	3.5V	12		12		ns		6,7
			5.5V	12		12		ns		6,7
11	Tost	Oscillator Startup Time	3.5V		5TpC		5TpC			6,7
			5.5V		5TpC		5TpC			6,7
12	Twdt	Watchdog Timer Delay Time Before Timeout	3.5V	7		10		ms	D0 = 0	8,9
			5.5V	3.5		5		ms	D1 = 0	5,11
			3.5V	14		20		ms	D0 = 1	5,11
			5.5V	7		10		ms	D1 = 0	5,11
			3.5V	28		40		ms	D1 = 0	5,11
			5.5V	14		20		ms	D1 = 1	5,11
			3.5V	112		160		ms	D0 = 1	5,11
			5.5V	56		80		ms	D1 = 1	5,11

Notes

1. The V_{CC} voltage specification of 5.5 V guarantees $5.0\text{ V} \pm 0.5\text{ V}$ and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V.
2. Timing Reference uses 0.7 V_{C0} for a logic 1 and 0.2 V_{GC} for a logic 0.
3. SMR D1 = 0.
4. SMR-D5 = 1, POR STOP Mode Delay is on
5. Interrupt request via Port 3 (P31-P33)
6. Interrupt request via Port 3 (P30).
7. Maximum frequency for internal system clock is 2 MHz when using Low EMI OSC PCON Bit D7 = 0
8. Reg. WDTMR.
9. Using internal RC.

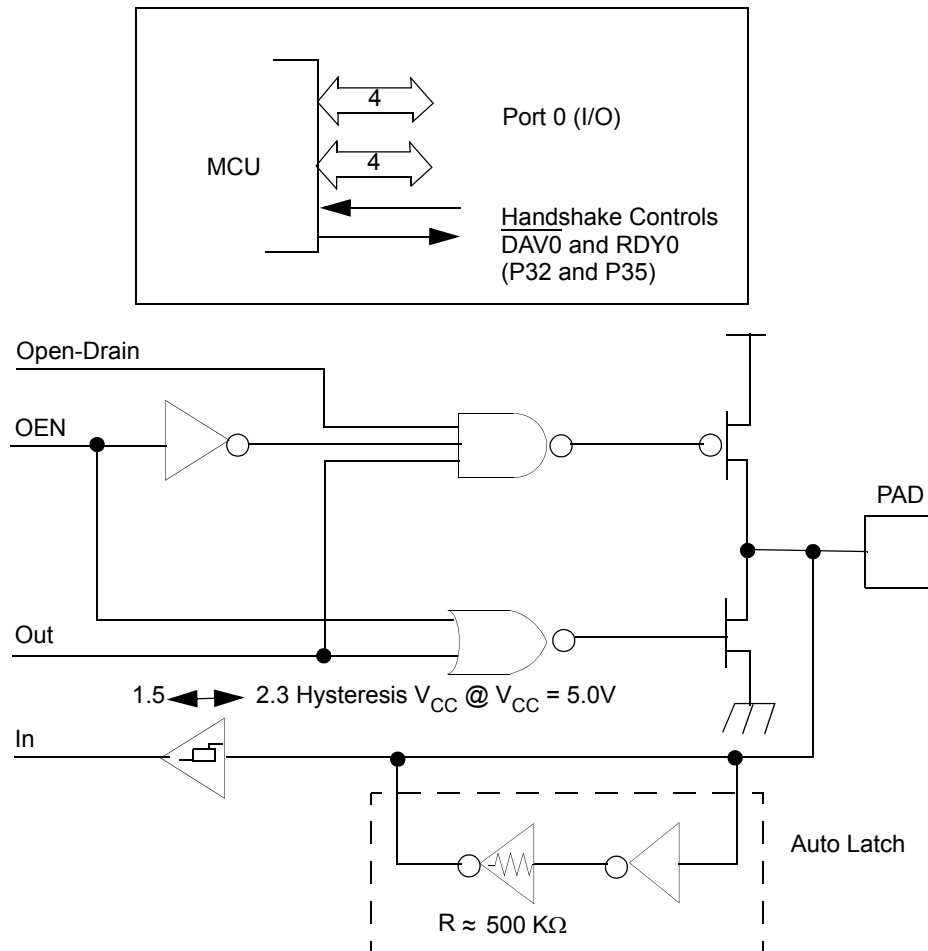


Figure 18. Port 0 Configuration

Port 1 (P17-P10). Port 1 is an 8-bit, bidirectional, CMOS-compatible port with multiplexed Address (A7-A0) and Data (D7-D0) ports. These eight I/O lines can be programmed as inputs or outputs or can be configured under software control as an Address/Data port for interfacing external memory. The input buffers are Schmitt-triggered and the output buffers can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 1 can be placed under handshake control. In this configuration, Port 3, lines P33 and P34 are used as the handshake controls RDY1 and $\overline{\text{DAV1}}$ (Ready and Data Available). To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 outputs the additional lines (see [Figure 19](#)).

Port 1 can be placed in the high-impedance state along with Port 0, $\overline{AS}$, $\overline{DS}$, and $R/\overline{W}$, allowing the Z86E43/743/E44 to share common resources in multiprocessor and DMA applications. In ROM mode, Port 1 is defined as input after reset.

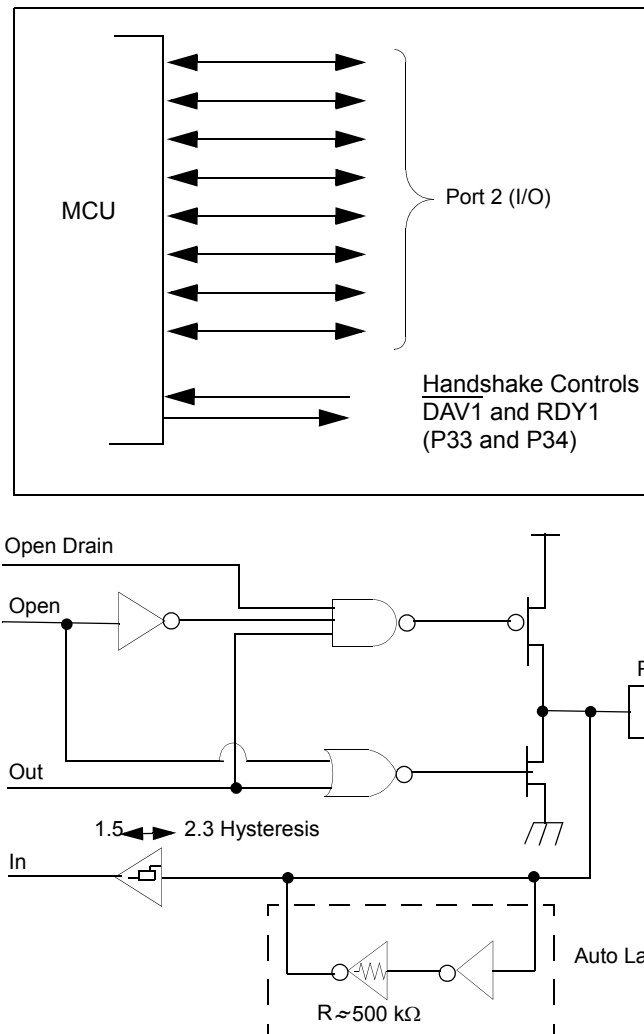


Figure 19. Port 1 Configuration (Z86E43/743/E44 Only)

Port 2 (P27-P20). Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port. These eight I/O lines can be configured under software control as an input or output, independently. All input buffers are Schmitt-triggered. Bits programmed as outputs can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. When used as an I/O port, Port 2 can be placed under handshake control. After reset, Port 2 is defined as an input.

In Handshake Mode, Port 3 lines P31 and P36 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to bit 7 of Port 2 (see [Figure 20](#)).

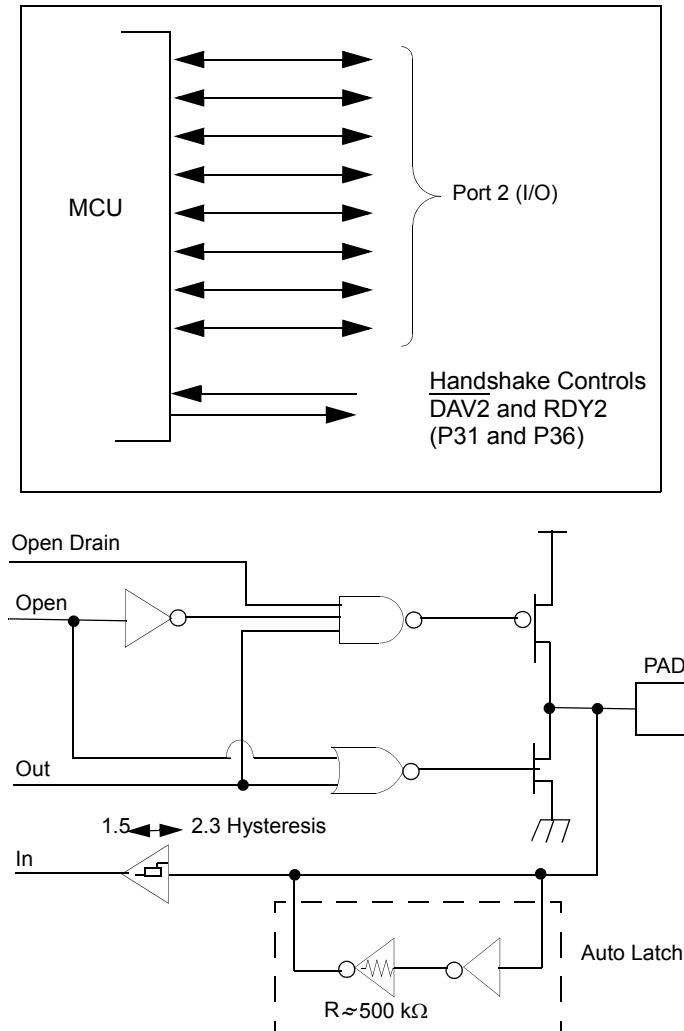


Figure 20. Port 2 Configuration

Port 3 (P37-P30). Port 3 is an 8-bit, CMOS-compatible port with four fixed inputs (P33-P30) and four fixed outputs (P37-P34). These eight lines can be configured by software for interrupt and handshake control functions. Port 3, Pin 0 is Schmitt-triggered. P31, P32, and P33 are standard CMOS inputs with single trip point (no Auto Latches) and P34, P35, P36, and P37 are push-pull output lines. Low EMI output buffers can be globally programmed by the software. Two on-board comparators can process analog signals on P31

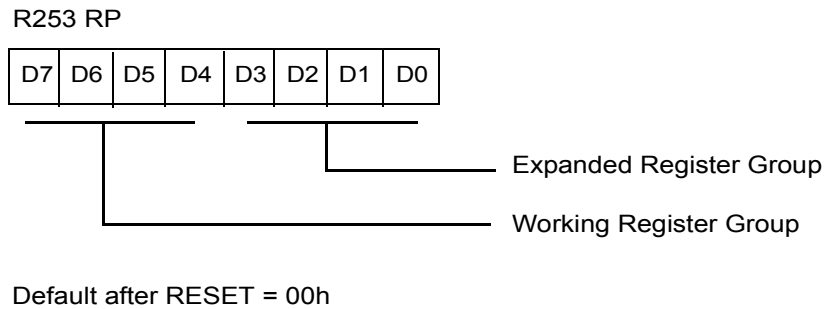


Figure 24. Register Pointer Register

Expanded Register File (ERF). The register file has been expanded to allow for additional system control registers, mapping of additional peripheral devices and input/output ports into the register address area. The Z8 register address space R0 through R15 is implemented as 16 groups of 16 registers per group (see [Figure 26](#)). These register banks are known as the Expanded Register File (ERF).

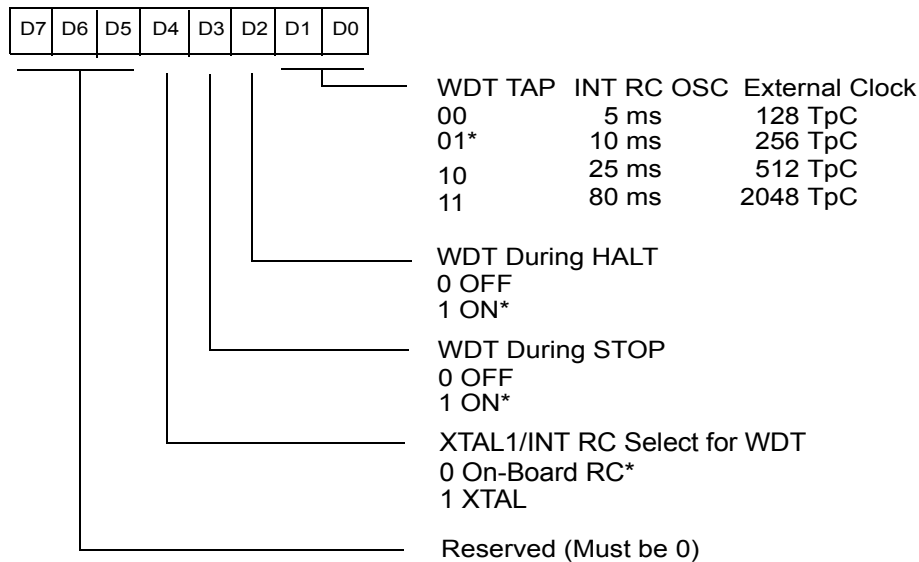
The low nibble (D3-D0) of the Register Pointer (RP) select the active ERF Bank, and the high nibble (D7-D4) of register RP select the working register group. Three system configuration registers reside in the Expanded Register File at bank FH: PCON, SMR, and WDTMR. The rest of the Expanded Register is not physically implemented and is reserved for future expansion.

- **Note:** *WDT time-out in STOP Mode will not reset SMR, SMR2, PCON, WDTMR, P2M, P3M, Ports 2 & 3 Data Registers, but will activate the T_{POR} delay.*

WDTMR Register Accessibility. The WDTMR register is accessible only during the first 60 internal system clock cycles from the execution of the first instruction after Power-On Reset, Watchdog reset or a Stop Mode Recovery (Figure 33 and Figure 34). After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register File at address location 0Fh.

Clock Free WDT Reset. The WDT will enable the Z8 to reset the I/O pins whenever the WDT times out, even without a clock source running on the XTAL1 and XTAL2 pins. WDTMR Bit D4 must be 0 for the clock Free WDT to work. The I/O pins will default to their default settings.

WDTMR (F) 0F



* Default setting after RESET

Figure 33. Watchdog Timer Mode Register Write Only

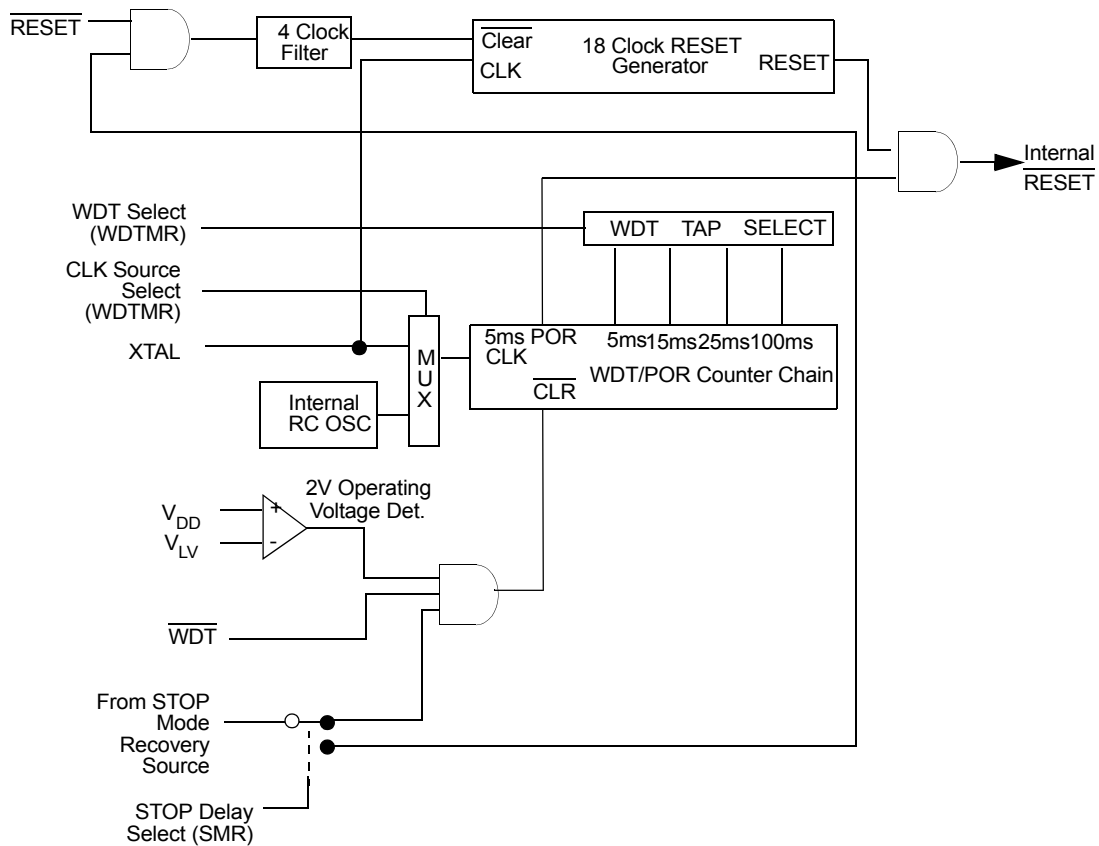
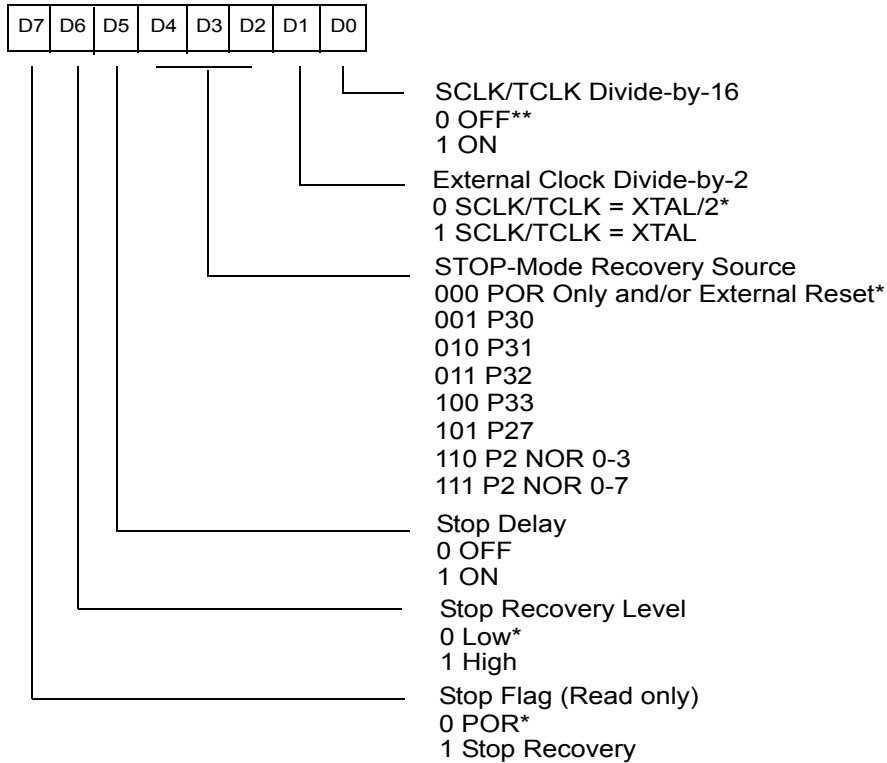


Figure 34. Resets and WDT

Auto Reset Voltage. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. Reset is globally driven if V_{CC} is below VLV (Figure 35).

SMR (Fh) 0B



Note: Note used in conjunction with SMR2 Source

* Default setting after RESET

** Default setting after RESET and STOP-Mode Recovery

Figure 37. Stop Mode Recovery Register (Write Only Except Bit D7, Which is Read Only)

R240

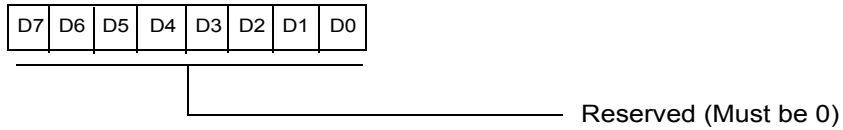
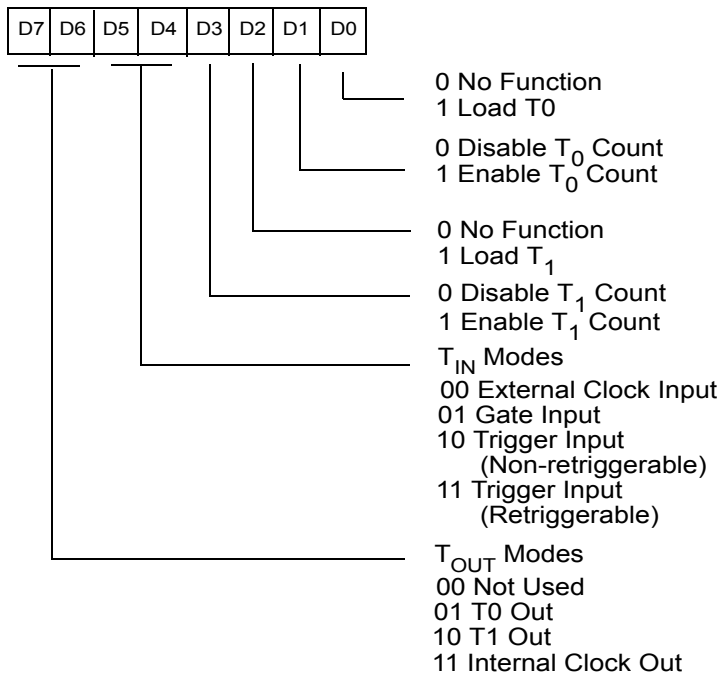


Figure 40. Reserved

R241 Timer



Default After Reset = 00h

Figure 41. Timer Mode Register (F1_n: Read/Write)

R249 IPR

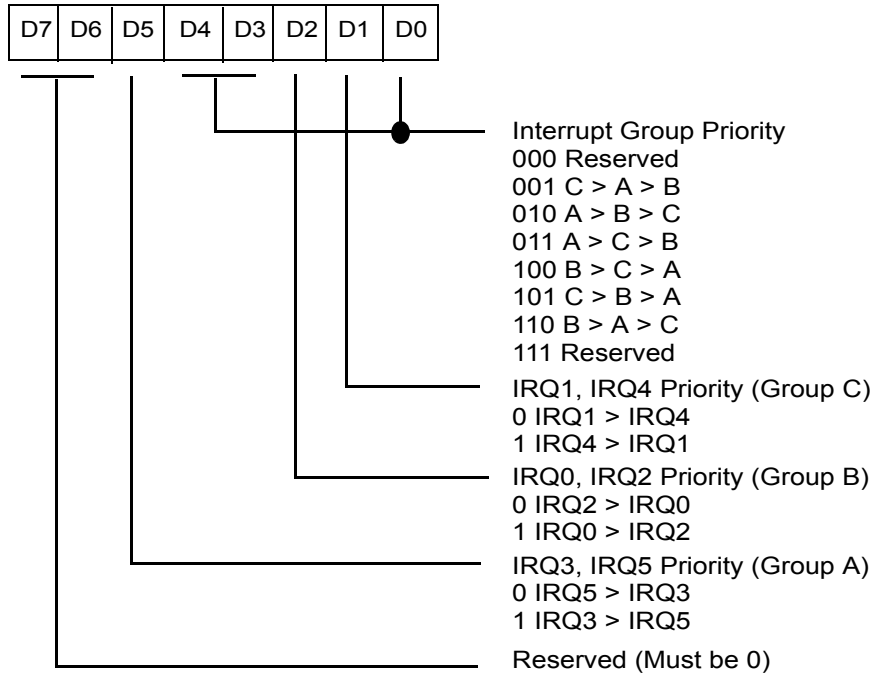


Figure 49. Interrupt Priority Register (F9_h: Write Only)

R250 IRQ

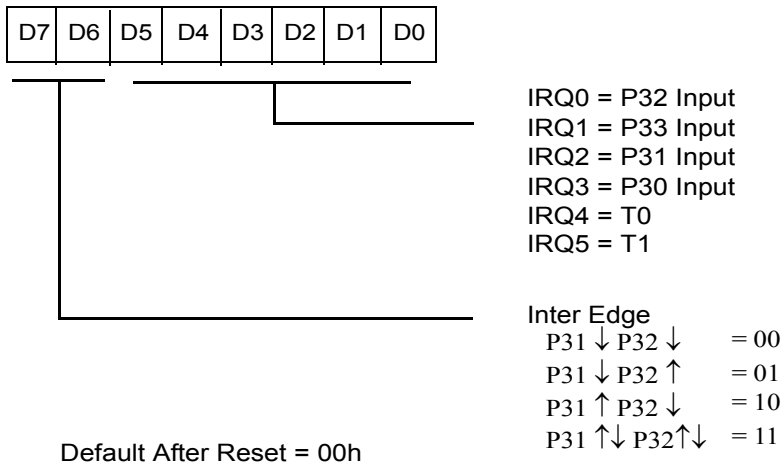


Figure 50. Interrupt Request Register (FA_h: Read/Write)