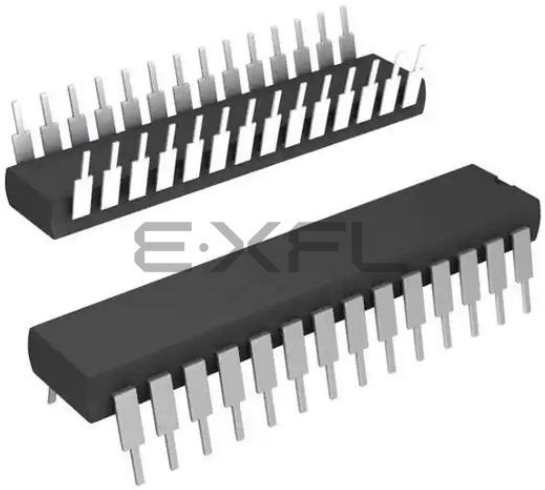

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	EBI/EMI
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e3412psg

Table of Contents

Pin Description

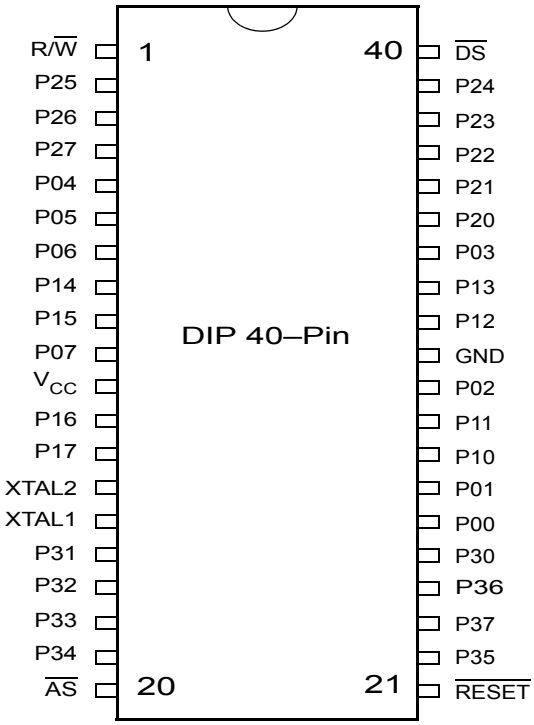

Figure 3. 40-Pin DIP Pin Configuration Standard Mode

Table 2. 40-Pin DIP Pin Identification Standard Mode

Pin No	Symbol	Function	Direction
1	R/$\overline{W}$	Read/Write	Output
2-4	P25-P27	Port 2, Pins 5,6,7	Input/Output
5-7	P04-P06	Port 0, Pins 4,5,6	Input/Output
8-9	P14-P15	Port 1, Pins 4,5	Input/Output
10	P07	Port 0, Pin 7	Input/Output
11	V_{CC}	Power Supply	
12-13	P16-P17	Port 1, Pins 6,7	Input/Output
14	XTAL2	Crystal Oscillator	Output

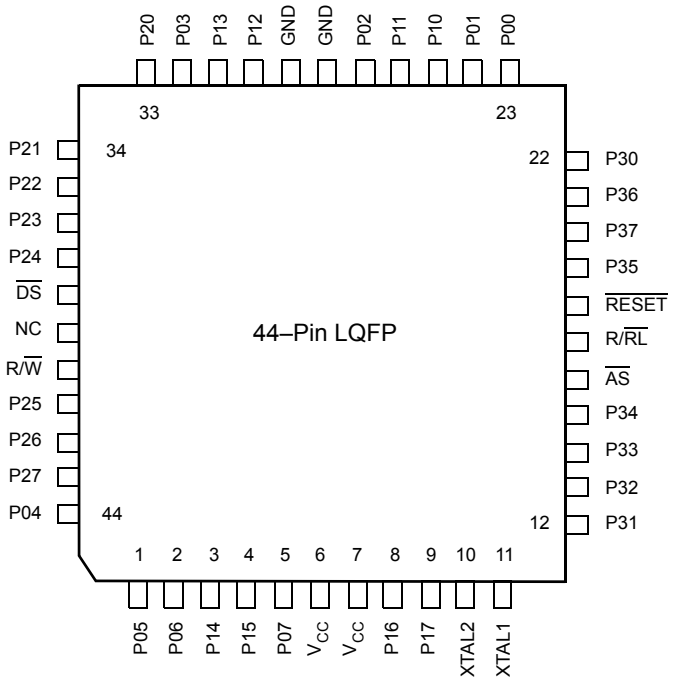

Figure 5. 44-Pin LQFP Pin Configuration Standard Mode

Table 4. 44-Pin LQFP Pin Identification

Pin No	Symbol	Function	Direction
1-2	P05-P06	Port 0, Pins 5,6	Input/Output
3-4	P14-P15	Port 1, Pins 4,5	Input/Output
5	P07	Port 0, Pin 7	Input/Output
6-7	V_{CC}	Power Supply	
8-9	P16-P17	Port 1, Pins 6,7	Input/Output
10	XTAL2	Crystal Oscillator	Output
11	XTAL1	Crystal Oscillator	Input
12-14	P31-P33	Port 3, Pins 1,2,3	Input
15	P34	Port 3, Pin 4	Output
16	AS	Address Strobe	Output
17	R//RL	ROM/ROMless select	Input

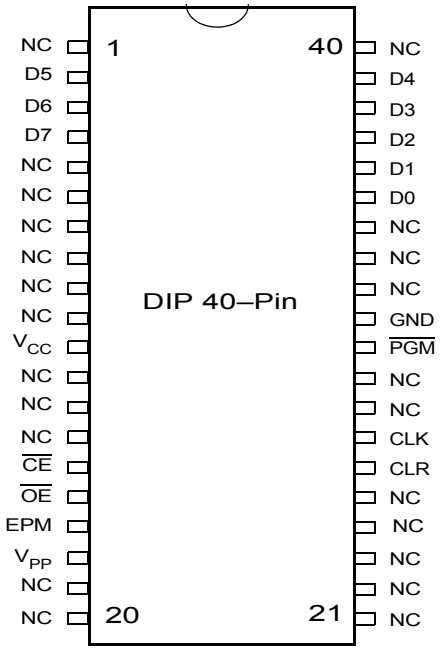

Figure 6. 40-Pin DIP Pin Configuration EPROM Mode

Table 5. 40-Pin DIP Package Pin Identification EPROM Mode

Pin No	Symbol	Function	Direction
1	NC	No Connection	
2-4	D5-D7	Data 5,6,7	Input/Output
5-10	NC	No Connection	
11	V_{CC}	Power Supply	
12-14	NC	No Connection	
15	CE	Chip Select	Input
16	OE	Output Enable	Input
17	EPM	EPROM Prog. Mode	Input
18	V_{PP}	Prog. Voltage	Input
19-25	NC	No Connection	
26	CLR	Clear	Input
27	CLK	Clock	Input
28-29	NC	No Connection	

Table 6. 44-Pin PLCC Pin Configuration EPROM Programming Mode (Continued)

Pin No	Symbol	Function	Direction
32-39	NC	No Connection	
40	CLR	Clear	Input
41	CLK	Clock	Input
42-43	NC	No Connection	
44	/PGM	Prog. Mode	Input

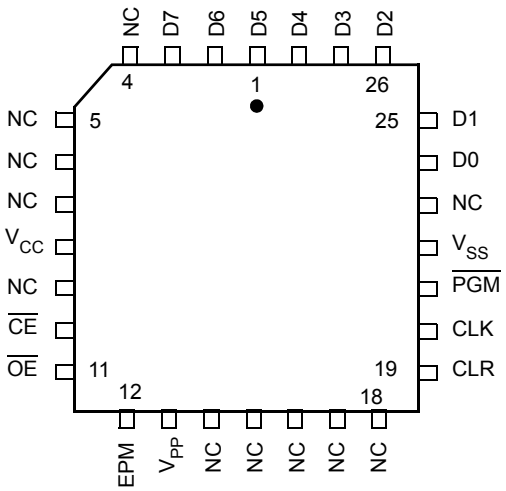

Figure 12. EPROM Programming Mode 28-Pin PLCC Pin Configuration

Table 9. 28-Pin EPROM Pin Identification EPROM Mode

Pin #	Symbol	Function	Direction
1-3	D5-D7	Data 5,6,7	Input/Output
4-7	NC	No Connection	
8	V_{CC}	Power Supply	
9	NC	No connection	
10	CE	Chip Select	Input
11	OE	Output Enable	Input
12	EPM	EPROM Prog. Mode	Input
13	V_{PP}	Prog. Voltage	Input
14-18	NC	No Connection	
19	CLR	Clear	
20	CLK	Clock	
21	/PGM	Prog. Mode	Input
22	V_{SS}	Ground	
23	NC	No Connection	
24-28	D0-D4	Data 0,1,2,3,4	Input/Output

DC Electrical Characteristics

Table 11. DC Electrical Characteristics T_A = 0 °C to +70 °C

Symbol	Parameter	V_{CC}[1]	Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.5V	0.7 V_{CC}	V_{CC} +0.3	1.8	V	Driven by External Clock Generator	
		5.5V	0.7 V_{CC}	V_{CC} +0.3	2.5	V		
V_{CL}	Clock Input Low Voltage	3.5V	GND -0.3	0.2 V_{CC}	0.9	V	Driven by External Clock Generator	
		5.5V	GND -0.3	0.2 V_{CC}	1.5	V		
V_{IH}	Input High Voltage	3.5V	0.7 V_{CC}	V_{CC} +0.3	2.5	V		
		5.5V	0.7 V_{CC}	V_{CC} +0.3	2.5	V		
V_{IL}	Input Low Voltage	3.5V	GND -0.3	0.2 V_{CC}	1.5	V		
		5.5V	GND -0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltage Low EMI Mode	3.5V	V_{CC} -0.4		3.3		I_{OH} = -0.5 mA	
		5.5V	V_{CC} -0.4		4.8			
V_{OH1}	Output High Voltage	3.5V	V_{CC} -0.4		3.3	V	I_{OH} = -2.0 mA	
		5.5V	V_{CC} -0.4		4.8	V	I_{OH} = -2.0 mA	
V_{OL}	Output Low Voltage Low EMI Mode	3.5V		0.4	0.2	V	I_{OL} = 1.0 mA	
		5.5V		0.4	0.2	V	I_{OL} = 1.0 mA	
V_{OL1}	Output Low Voltage	3.5V		0.4	0.1	V	I_{OL} = +4.0 mA	2
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	2
V_{OL2}	Output Low Voltage	3.5V		1.2	0.5	V	I_{OL} = +10 mA	2
		5.5V		1.2	0.5	V	I_{OL} = +10 mA	2
V_{RH}	Reset Input High Voltage	3.5V	.8 V_{CC}	V_{CC}	1.7	V		3
		5.5V	.8 V_{CC}	V_{CC}	2.1	V		3
V_{RL}	Reset Input Low Voltage	3.5V	GND -0.3	0.2 V_{CC}	1.3	V		3
		5.5V	GND -0.3	0.2 V_{CC}	1.7	V		3
V_{OLR}	Reset Output Low Voltage	3.5V		0.6	0.3	V	I_{OL} = 1.0 mA	3
		5.5V		0.6	0.2	V	I_{OL} = 1.0 mA	3

Table 18. Additional Timing Table (Divide by Two Mode) T_A = -40 °C to +105 °C (Continued)

No	Symbol	Parameter	V_{CC} [1]	Min	Max	Min	Max	Units	Conditions	Notes
12	Twdt	Watchdog Timer Delay Time Before Timeout	3.5V	7		10		ms	D0 =0	8,9
			5.5V	3.5		5		ms	D1 = 0	5,11
			3.5V	14		20		ms	D0 =1	5,11
			5.5V	7		10		ms	D1 = 0	5,11
			3.5V	28		40		ms	D1 = 0	5,11
			5.5V	14		20		ms	D1 = 1	5,11
			3.5V	112		160		ms	D0 = 1	5,11
			5.5V	56		80		ms	D1 = 1	5,11

Notes
1. The V_{CC} voltage specification of 5.5 V guarantees 5.0 V ± 0.5 V and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V.
2. Timing Reference uses 0.7 VC0 for a logic 1 and 0.2 VGC for a logic 0.
3. SMR D1 = 0.
4. SMR-D5 = 1, POR STOP Mode Delay is on
5. Interrupt request via Port 3 (P31-P33)
6. Interrupt request via Port 3 (P30).
7. Maximum frequency for internal system clock is 2 MHz when using Low EMI OSC PCON Bit D7 = 0
8. Reg. WDTMR.
9. Using internal RC.

Pin Functions

EPROM Programming Mode

D7-D0 Data Bus. The data can be read from or written to external memory through the data bus.

V_{CC} Power Supply. This pin must supply 5 V during the EPROM read mode and 6 V during other modes.

$\overline{CE}$ Chip Enable (active Low). This pin is active during EPROM Read Mode, Program Mode, and Program Verify Mode.

$\overline{OE}$ Output Enable (active Low). This pin drives the direction of the Data Bus. When this pin is Low, the Data Bus is output, when High, the Data Bus is input.

EPM EPROM Program Mode. This pin controls the different EPROM Program Mode by applying different voltages.

V_{PP} Program Voltage. This pin supplies the program voltage.

PGM Program Mode (active Low). When this pin is Low, the data is programmed to the EPROM through the Data Bus.

and P32 with reference to the voltage on P33. The analog function is enabled by setting the D1 of Port 3 Mode Register (P3M). The comparator output can be outputted from P34 and P37, respectively, by setting PCON register Bit D0 to 1 state. For the interrupt function, P30 and P33 are falling edge triggered interrupt inputs. P31 and P32 can be programmed as falling, rising or both edges triggered interrupt inputs (see Figure 21). Access to Counter/Timer 1 is made through P31 (T_{IN}) and P36 (T_{OUT}). Handshake tines for Port 0, Port 1, and Port 2 are also available on Port 3 (see Table 19).

Note: *When enabling or disabling analog mode, the following is recommended:*

1. Allow two NOP decays before reading this comparator output.
2. Disable global interrupts, switch to analog mode, clear interrupts, and then re-enable interrupts.
3. IRQ register bits 3 to 0 must be cleared after enabling analog mode.

Note: *P33-P30 differs from the Z86C33/C43/233/243 in that there is no clamping diode to V_{CC} due to the EPROM high-voltage circuits. Exceeding the V_{IH} maximum specification during standard operating mode may cause the device to enter EPROM mode.*

Table 19. Port 3 Pin Assignments

Pin	I/O	CTC1	Analog	Interrupt	P0 HS	P1 HS	P2 HS	Ext
P30	IN			IRQ3				
P31	IN	T_{IN}	AN1	IRQ2		D/R		
P32	IN		AN2	IRQ0	D/R			
P33	IN		REF	IRQ1		D/R		
P34	OUT		AN1-Out			R/D		DM
P35	OUT				R/D			
P36	OUT	T_{OUT}				R/D		
P37	OUT		An2-Out					

Comparator Inputs. Port 3, P31, and P32, each have a comparator front end. The comparator reference voltage P33 is common to both comparators. In analog mode, P31 and P32 are the positive input of the comparators and P33 is the reference voltage of the comparators.

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs (except P33-P31) that are not externally driven. Whether this level is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer. Auto Latches are available on Port 0, Port 1, Port 2, and P30. There are no Auto Latches on P31, P32, and P33.

Low EMI Emission. The Z86E43/743/E44 can be programmed to operate in a low EMI Emission Mode in the PCON register. The oscillator and all I/O ports can be programmed as low EMI emission mode independently. Use of this feature results in:

- The pre-drivers slew rate reduced to 10 ns typical.
- Low EMI output drivers have resistance of 200 Ohms (typical).
- Low EMI Oscillator.
- Internal SCLK/TCLK= XTAL operation limited to a maximum of 4 MHz - 250 ns cycle time, when Low EMI Oscillator is selected.

Note: *For emulation only:*
Do not set the emulator to emulate Port 1 in low EMI mode. Port 1 must always be configured in Standard Mode.

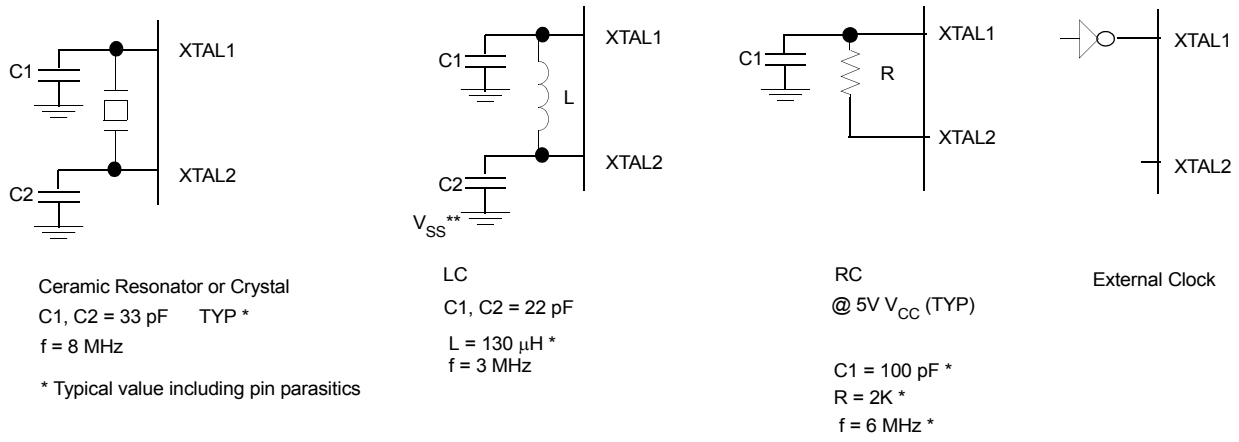

Figure 29. Oscillator Configuration

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR timer allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

1. Power fail to Power OK status
2. Stop Mode Recovery (if D5 of SMR=0)
3. WDT time-out

The POR time is a nominal 5 ms. Bit 5 of the STOP mode Register (SMR) determines whether the POR timer is by-passed after Stop Mode Recovery (typical for an external clock and RC/LC oscillators with fast start up times).

HALT. Turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupt IRQ0, IRQ1, and IRQ2 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT. In order to enter STOP or HALT Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, you must execute a NOP (Opcode = FFh) immediately before the appropriate sleep instruction, that is:

Comparator Output Port 3 (D0). Bit 0 controls the comparator output in Port 3. A "1" in this location brings the comparator outputs to P34 and P37, and a "0" releases the Port to its standard I/O configuration. The default value is 0.

Port 1 Open-Drain (D1). Port 1 can be configured as an open-drain by resetting this bit (D1=0) or configured as push-pull active by setting this bit (D1=1). The default value is 1.

Port 0 Open-Drain (D2). Port 0 can be configured as an open-drain by resetting this bit (D2=0) or configured as push-pull active by setting this bit (D2=1). The default value is 1.

Low EMI Port 0 (D3). Port 0 can be configured as a Low EMI Port by resetting this bit (D3=0) or configured as a Standard Port by setting this bit (D3=1). The default value is 1.

Low EMI Port 1 (D4). Port 1 can be configured as a Low EMI Port by resetting this bit (D4=0) or configured as a Standard Port by setting this bit (D4=1). The default value is 1.

Note: *The emulator does not support Port 1 low EMI mode and must be set D4 = 1.*

Low EMI Port 2 (D5). Port 2 can be configured as a Low EMI Port by resetting this bit (D5=0) or configured as a Standard Port by setting this bit (D5=1). The default value is 1.

Low EMI Port 3 (D6). Port 3 can be configured as a Low EMI Port by resetting this bit (D6=0) or configured as a Standard Port by setting this bit (D6=1). The default value is 1.

Low EMI OSC (D7). This bit of the PCON Register controls the low EMI noise oscillator. A "1" in this location configures the oscillator with standard drive. While a "0" configures the oscillator with low noise drive, however, it does not affect the relationship of SCLK and XTAL. The low EMI mode will reduce the drive of the oscillator (OSC). The default value is 1.

Note: *4 MHz is the maximum external clock frequency when running in the low EMI oscillator mode.*

Stop-Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of Stop Mode Recovery (Figure 31). All bits are Write Only except bit 7 which is a Read Only. Bit 7 is a flag bit that is hardware set on the condition of STOP Recovery and reset by a power-on cycle. Bit 6 controls whether a low or high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4 of the SMR register specify the Stop Mode Recovery Source. The SMR is located in Bank F of the Expanded Register File at address 0BH.

Table 22. Stop Mode Recovery Source

D4	D3	D2	SMR Source selection
0	0	0	POR recovery only
0	0	1	P30 transition
0	1	0	P31 transition (Not in analog mode)
0	1	1	P32 transition (Not in analog mode)
1	0	0	P33 transition (Not in analog mode)
1	0	1	P27 transition
1	1	0	Logical NOR of Port 2 bits 0-3
1	1	1	Logical NOR of Port 2 bits 0-7

Stop Mode Recovery Delay Select (D5). The 5 ms RESET delay after Stop Mode Recovery is disabled by programming this bit to a zero. A "1" in this bit will cause a 5 ms RESET delay after Stop Mode Recovery. The default condition of this bit is 1. If the fast wake up mode is selected, the Stop Mode Recovery source needs to be kept active for at least 5TpC.

Stop Mode Recovery Level Select (D6). A "1" in this bit defines that a high level on any one of the recovery sources wakes the MCU from STOP Mode. A 0 defines low level recovery. The default value is 0.

Cold or Warm Start (D7). This bit is set by the device upon entering STOP Mode. A "0" in this bit indicates that the device has been reset by POR (cold). A "1" in this bit indicates the device was awakened by a SMR source (warm).

Stop Mode Recovery Register 2 (SMR2). This register contains additional Stop Mode Recovery sources. When the Stop Mode Recovery sources are selected in this register then SMR Register Bits D2, D3, and D4 must be 0.

SMR:10		Operation
D1	DO	Description of Action
0	0	POR and/or external reset recovery
0	1	Logical AND of P20 through P23
1	0	Logical AND of P20 through P27

Watchdog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is disabled after Power-On

Reset and initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT is driven either by an on-board RC oscillator or an external oscillator from XTAL1 pin. The POR clock source is selected with bit 4 of the WDT register.

Note: *Execution of the WDT instruction affects the Z (Zero), S (Sign), and V (Overflow) flags.*

WDT Time-Out Period (D0 and D1). Bits 0 and 1 control a tap circuit that determines the time-out periods that can be obtained (Table 23). The default value of DO and Dl are 1 and 0, respectively.

Table 23. Time-out Period of WDT

D1	DO	Time-out of the Internal RC OSC	Time-out of the System Clock
0	0	5 ms	128 SCLK
0	1	10 ms[1]	256 SCLK[1]
1	0	20 ms	512 SCLK
1	1	80 ms	2048 SCLK

Note: The default setting is 10 ms.

WDT During HALT Mode (D2). This bit determines whether or not the WDT is active during HALT Mode. A “1” indicates that the WDT is active during HALT. A “0” disables the WDT in HALT Mode. The default value is “1 “. WDT During STOP Mode (D3). This bit determines whether or not the WDT is active during STOP mode. A “1” indicates active during STOP. A “0” disables the WDT during STOP Mode. This is applicable only when the WDT clock source is the internal RC oscillator.

Clock Source For WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1, and the WDT is stopped in STOP Mode. The default configuration of this bit is 0, which selects the RC oscillator.

Permanent WDT. When this feature is enabled, the WDT is enabled after reset and will operate in Run and HALT Mode. The control bits in the WDTMR do not affect the WDT operation. If the clock source of the WDT is the internal RC oscillator, then the WDT will run in STOP mode. If the clock source of the WDT is the XTAL1 pin, then the WDT will not run in STOP mode.

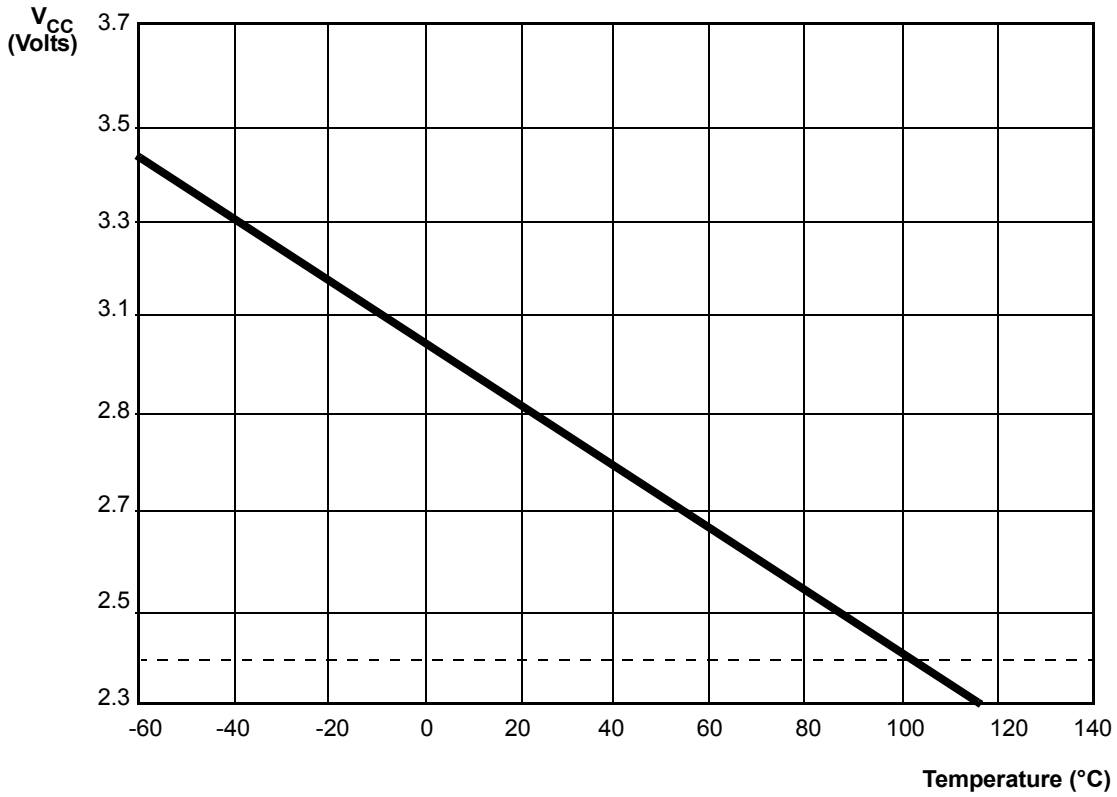

Figure 35. Typical V_{LV} Voltage vs. Temperature

Z8 Control Register Diagrams

Ordering Information

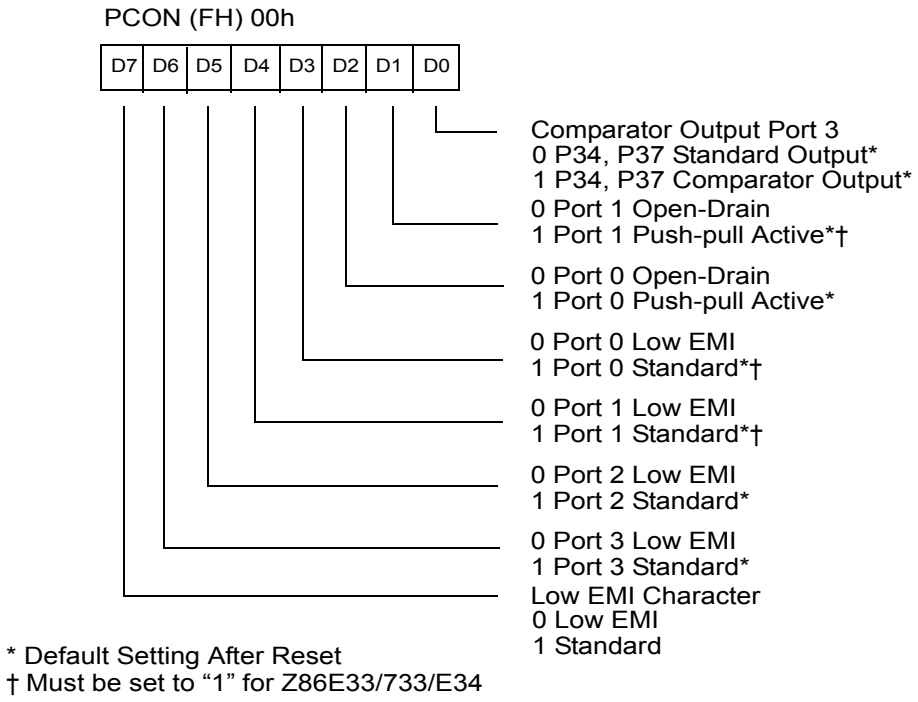

Figure 36. Port Configuration Register (PCON) (Write Only)

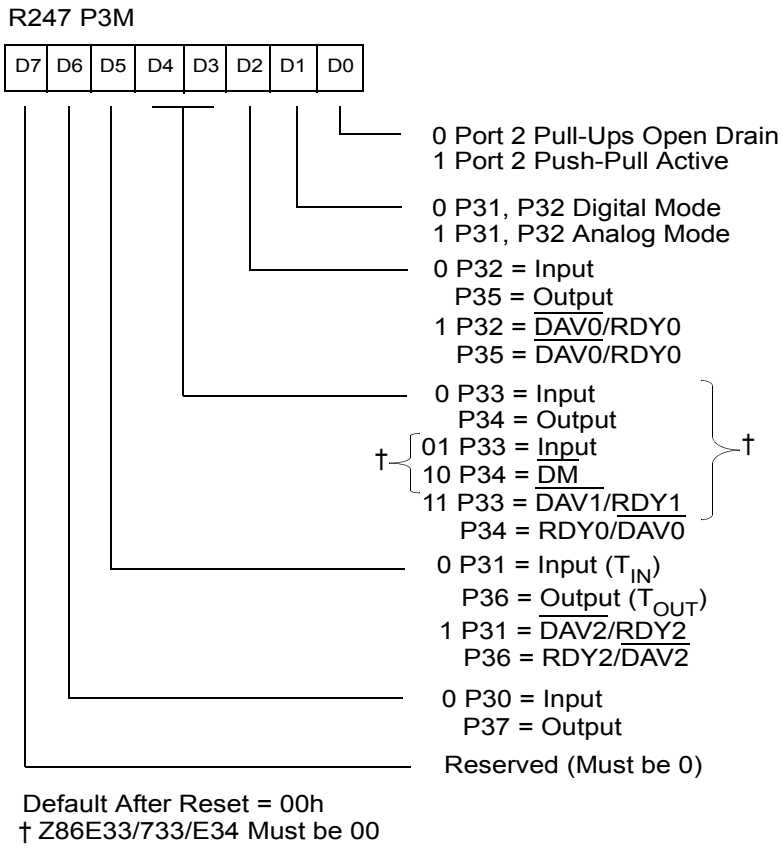

Figure 47. Port 3 Mode Register ($F7_h$: Write Only)

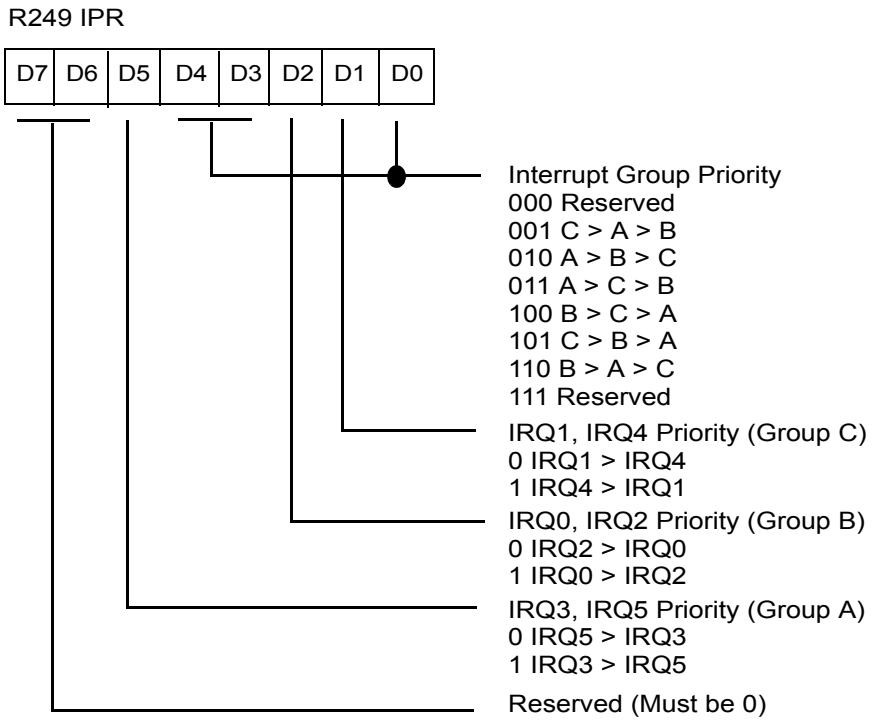

Figure 49. Interrupt Priority Register ($F9_h$: Write Only)

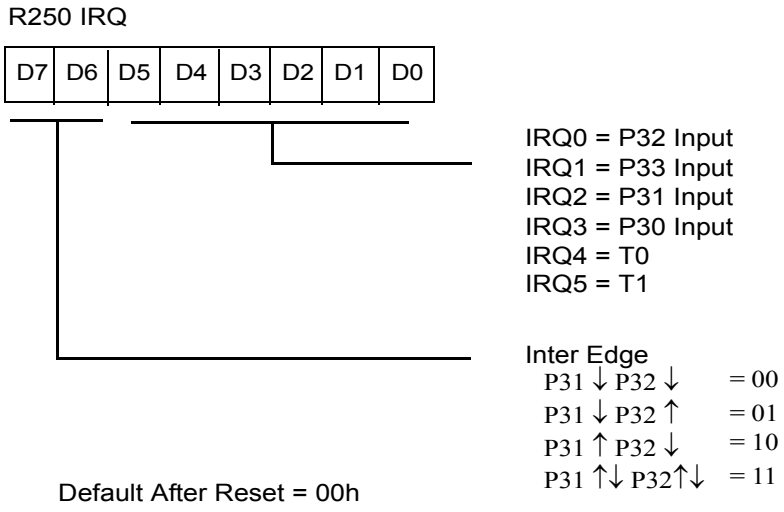

Figure 50. Interrupt Request Register (FA_h: Read/Write)

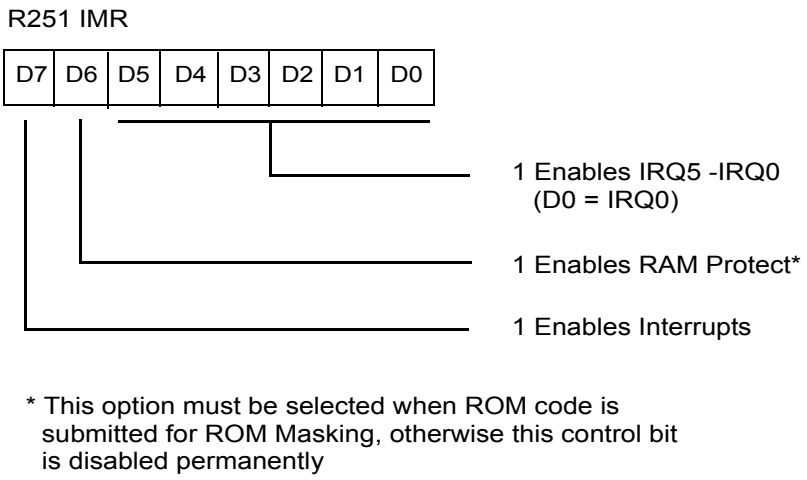

Figure 51. Interrupt Mask Register (FB_h: Read/Write)

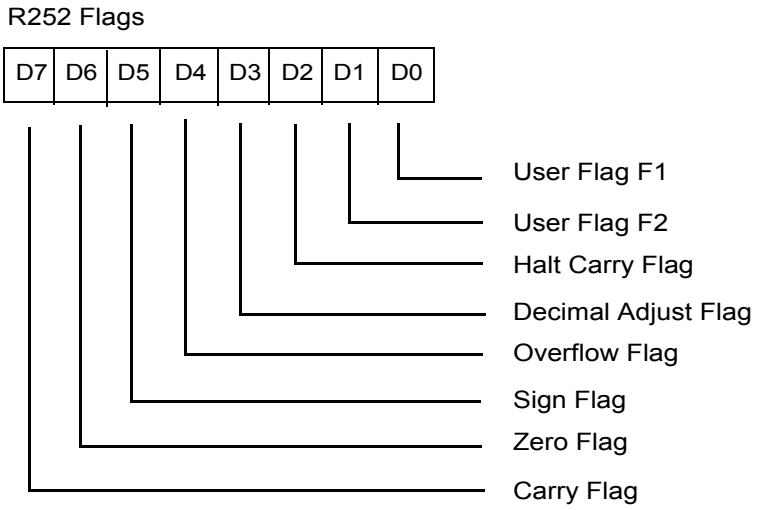

Figure 52. Flag Register (FC_h: Read/Write)

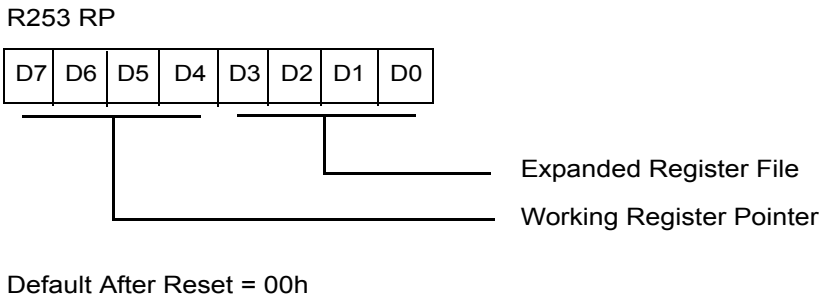

Figure 53. Register Pointer (FD_h: Read/Write)

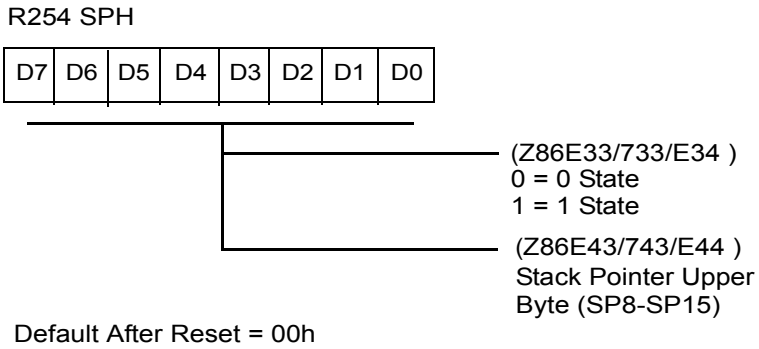

Figure 54. Stack Pointer High (FE_h: Read/Write)

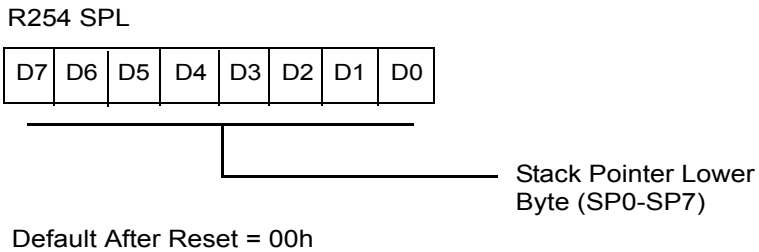

Figure 55. Stack Pointer Low (FF_h: Read/Write)