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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	EBI/EMI
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e3412ssc00tr

Table 1. Z86E33/733/E34, E43/743/E44 Features (Continued)

Device	ROM (KB)	RAM[1] (Bytes)	I/O Lines	Speed (MHz)
Z86E44	16	236	32	12

[1]General-Purpose

- Standard Temperature (V_{CC} = 3.5 V to 5.5 V)
- Extended Temperature (V_{CC} = 3.5 V to 5.5 V)
- Available Packages:
  - 28-Pin DIP/SOIC/PLCC OTP (E33/733/E34)
  - 40-Pin DIP OTP (E43/743/E44)
  - 44-Pin PLCC/LQFP OTP (E43/743/E44)
- Software Enabled Watchdog Timer (WDT)
- Push-Pull/Open-Drain Programmable on Port 0, Port 1, and Port 2
- 24/32 Input/Output Lines
- Clock-Free WDT Reset
- Auto Power-On Reset (POR)
- Programmable OTP Options:
  - RC Oscillator
  - EPROM Protect
  - Auto Latch Disable
  - Permanently Enabled WDT
  - Crystal Oscillator Feedback Resistor Disable
  - RAM Protect
- Low-Power Consumption: 60 mW
- Fast Instruction Pointer: 0.75 µs
- Two Standby Modes: STOP and HALT
- Digital Inputs CMOS Levels, Schmitt-Triggered
- Software Programmable Low EMI Mode
- Two Programmable 8-Bit Counter/Timers Each with a 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Six Different Sources
- Two Comparators

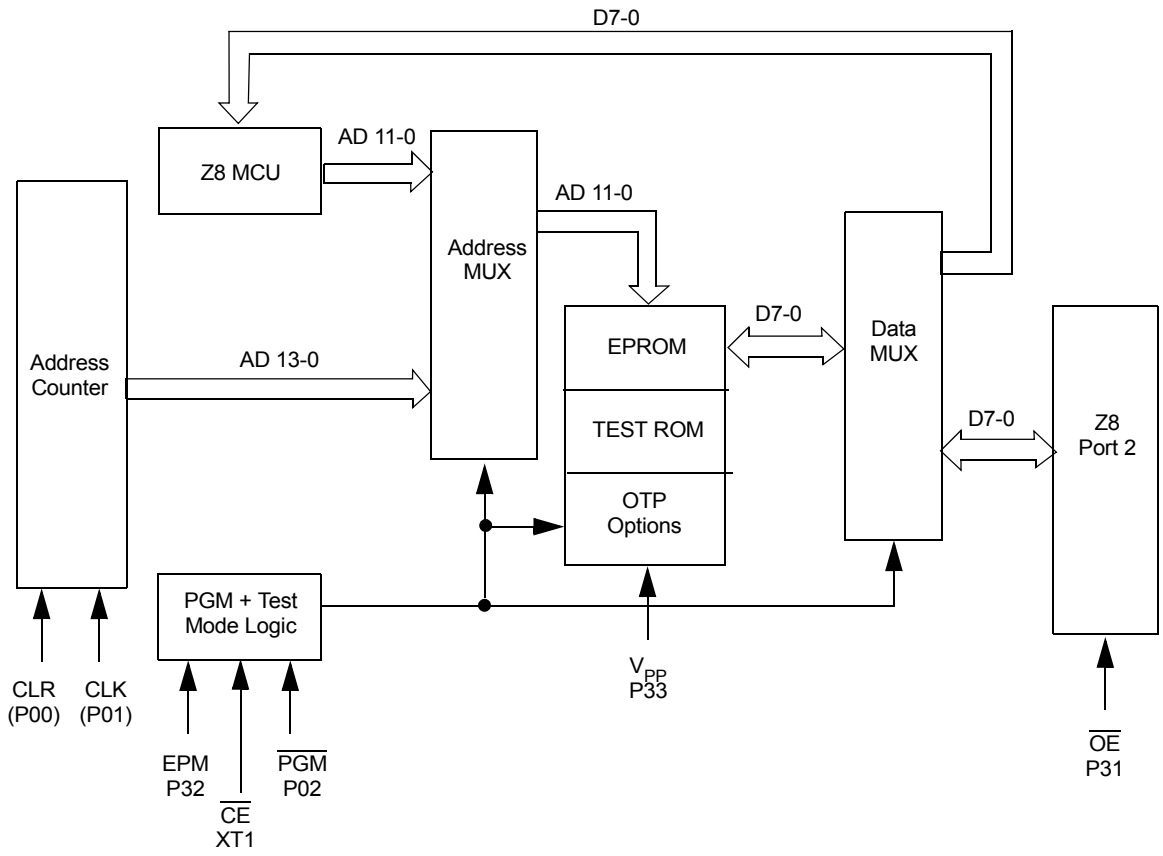


Figure 2. EPROM Programming Block Diagram

Pin Description

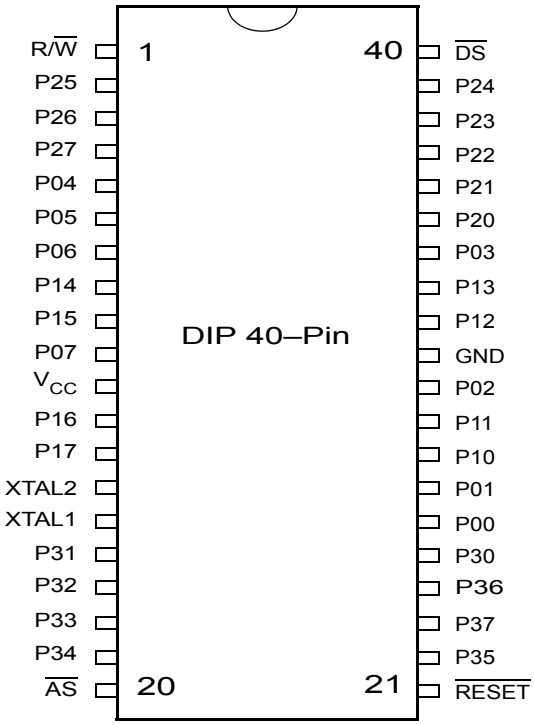


Figure 3. 40-Pin DIP Pin Configuration Standard Mode

Table 2. 40-Pin DIP Pin Identification Standard Mode

Pin No	Symbol	Function	Direction
1	R/$\overline{W}$	Read/Write	Output
2-4	P25-P27	Port 2, Pins 5,6,7	Input/Output
5-7	P04-P06	Port 0, Pins 4,5,6	Input/Output
8-9	P14-P15	Port 1, Pins 4,5	Input/Output
10	P07	Port 0, Pin 7	Input/Output
11	V_{CC}	Power Supply	
12-13	P16-P17	Port 1, Pins 6,7	Input/Output
14	XTAL2	Crystal Oscillator	Output

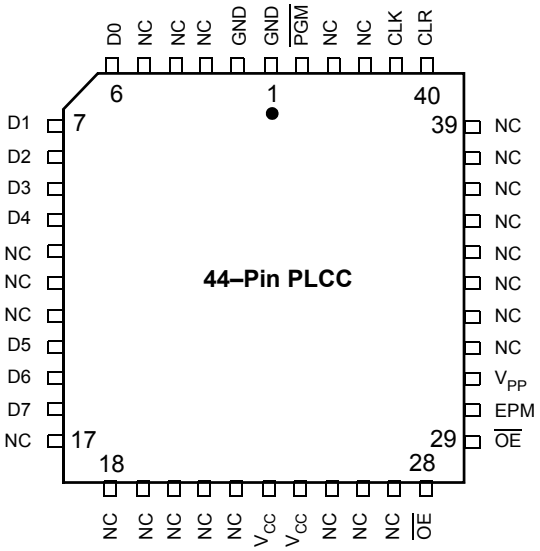


Figure 7. 44-Pin PLCC Pin Configuration EPROM Programming Mode

Table 6. 44-Pin PLCC Pin Configuration EPROM Programming Mode

Pin No	Symbol	Function	Direction
1-2	GND	Ground	
3-5	NC	No Connection	
6-10	D0-D4	Data 0,1,2,3,4	Input/Output
11-13	NC	No Connection	
14-16	D5-D7	Data 5,6,7	Input/Output
17-22	NC	No Connection	
23-24	V_{CC}	Power Supply	
25-27	NC	No Connection	
28	CE	Chip Select	Input
29	OE	Output Enable	Input
30	EPM	EPROM Prog. Mode	Input
31	V_{PP}	Prog. Voltage	Input

Table 6. 44-Pin PLCC Pin Configuration EPROM Programming Mode (Continued)

Pin No	Symbol	Function	Direction
32-39	NC	No Connection	
40	CLR	Clear	Input
41	CLK	Clock	Input
42-43	NC	No Connection	
44	/PGM	Prog. Mode	Input

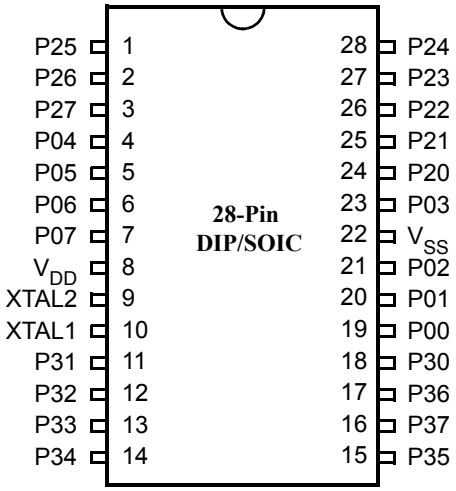


Figure 9. Standard Mode 28-Pin DIP/SOIC Pin Configuration

Table 8. 28-Pin DIP/SOIC/PLCC Pin Identification Standard Mode

Pin No	Symbol	Function	Direction
1-3	P25-P27	Port 2, Pins 5,6,	Input/Output
4-7	P04-P07	Port 0, Pins 4,5,6,7 In/Output	
8	V_{CC}	Power Supply	
9	XTAL2	Crystal Oscillator	Output
10	XTAL1	Crystal Oscillator	Input
11-13	P31-P33	Port 3, Pins 1,2,3	Input
14-15	P34-P35	Port 3, Pins 4,5	Output
16	P37	Port 3, Pin 7	Output
17	P36	Port 3, Pin 6	Output
18	P30	Port 3, Pin 0	Input
19-21	P00-P02	Port 0, Pins 0,1,2	Input/Output
22	V_{SS}	Ground	
23	P03	Port 0, Pin 3	Input/Output
24-28	P20-P24	Port 2, Pins 0,1,2,3,4	Input/Output

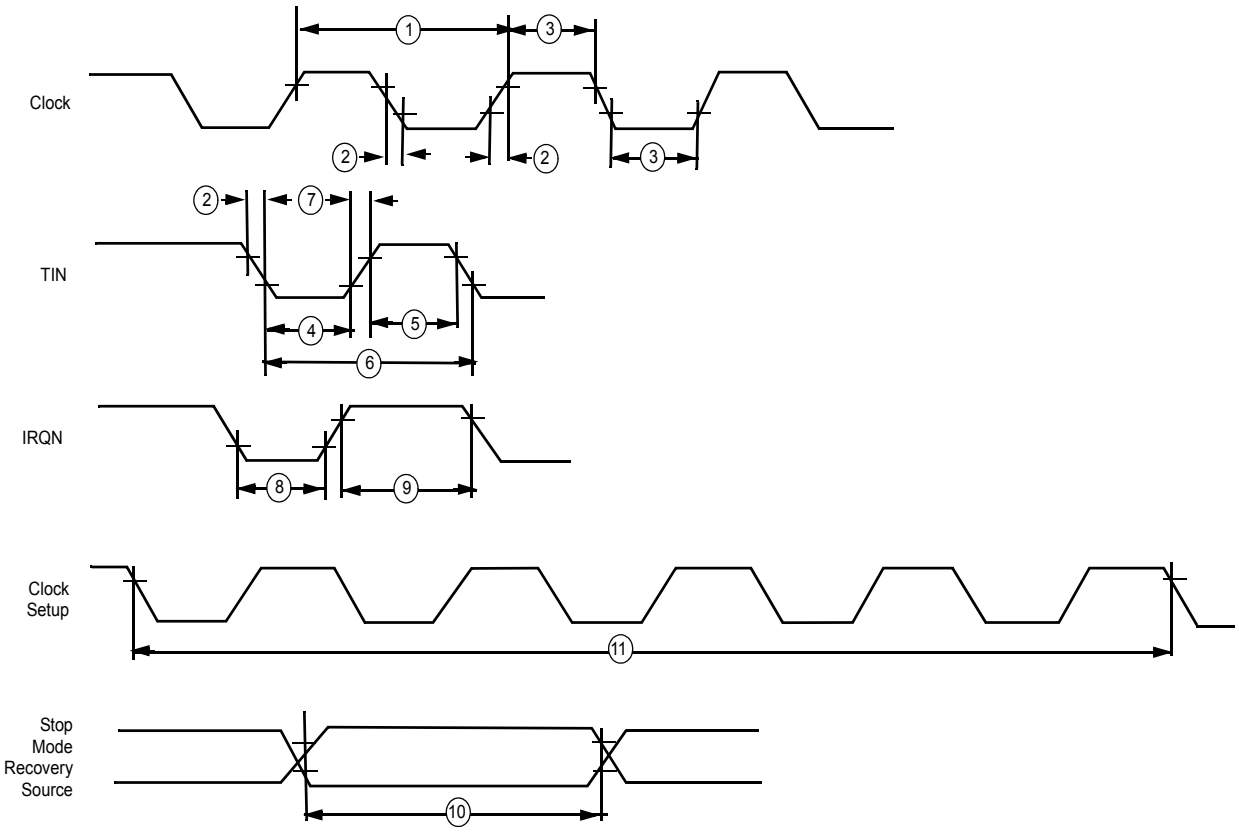


Figure 15. Additional Timing Diagram

Table 15. Additional Timing Table (Divide-By-One Mode) T_A = 0 °C to +70 °C

No	Symbol	Parameter	V_{CC} [1]	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.5V	250	DC	166	DC	ns	2,3,4
			5.5V	250	DC	166	DC	ns	2,3,4
2	TrC,TfC	Clock Input Rise & Fall Times	3.5V		25		25	ns	2,3,4
			5.5V		25		25	ns	2,3,4
3	TwC	Input Clock Width	3.5V	100		100		ns	2,3,4
			5.5V	100		100		ns	2,3,4
4	TwTinL	Timer Input Low Width	3.5V	100		100		ns	2,3,4
			5.5V	70		70		ns	2,3,4

Table 16. Additional Timing Table (Divide-By-One Mode) T_A = -40 °C to +105 °C (Continued)

No	Symbol	Parameter	V_{CC} [1]	Min	Max	Min	Max	Units	Notes
2	TrC,TfC	Clock Input Rise & Fall Times	4.5V		25		25	ns	2,3,4
			5.5V		25		25	ns	2,3,4
3	TwC	Input Clock Width	4.5V	100		100		ns	2,3,4
			5.5V	100		100		ns	2,3,4
4	TwTinL	Timer Input Low Width	4.5V	100		100		ns	2,3,4
			5.5V	70		70		ns	2,3,4
5	TwTinH	Timer Input High Width	4.5V	5TpC		5TpC			2,3,4
			5.5V	5TpC		5TpC			2,3,4
6	TpTin	Timer Input Period	4.5V	8TpC		8TpC			2,3,4
			5.5V	8TpC		8TpC			2,3,4
7	TrTin, TfTin	Timer Input Rise & Fall Timer	4.5V		100		100	ns	2,3,4
			5.5V		100		100	ns	2,3,4
8A	TwIL	Int. Request Low Time	4.5V	100		100		ns	2,3,4,5
			5.5V	70		70		ns	2,3,4,5
8B	TwIL	Int. Request Low Time	4.5V	5TpC		5TpC			2,3,4,6
			5.5V	5TpC		5TpC			2,3,4,6
9	TwIH	Int. Request Input High Time	4.5V	5TpC		5TpC			2,3,4,5
			5.5V	5TpC		5TpC			2,3,4,5
10	Twsm	Stop Mode Recovery Width Spec	4.5V	12		12		ns	4,7
			5.5V	12		12		ns	4,7
11	Tost	Oscillator Startup Time	4.5V		5TpC		5TpC		4,7,8
			5.5V		5TpC		5TpC		4,7,8

Notes

1. The V_{CC} voltage specification of 5.5 V guarantees 5.0 V ± 0.5 V and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V.
2. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC}; for a logic 0.
3. SMR D1 = 0.
4. Maximum frequency for internal system clock is 4 MHz when using Low EMI OSC PCON Bit D7=0.
5. Interrupt request via Port 3 (P31-P33).
6. Interrupt request via Port 3 (P30).
7. SMR-D5 = 1, POR STOP Mode Delay is on.
8. For RC and LC oscillator, and for oscillator driven by clock driver.

Table 18. Additional Timing Table (Divide by Two Mode) T_A = -40 °C to +105 °C

No	Symbol	Parameter	V_{CC}[1]	Min	Max	Min	Max	Units	Conditions	Notes
1	TpC	Input Clock Period	3.5V	62.5	DC	250	DC	ns		2,6,4
			5.5V	62.5	DC	250	DC	ns		2,6,4
2	TrC,TfC	Clock Input Rise & Fall Times	3.5V		15		25	ns		2,6,4
			5.5V		15		25	ns		2,6,4
3	TwC	Input Clock Width	3.5V	31		31		ns		2,6,4
			5.5V	31		31		ns		2,6,4
4	TwTinL	Timer Input Low Width	3.5V	70		70		ns		2,6,4
			5.5V	70		70		ns		2,6,4
5	TwTinH	Timer Input High Width	3.5V	5TpC		5TpC				2,6,4
			5.5V	5TpC		5TpC				2,6,4
6	TpTin	Timer Input Period	3.5V	8TpC		8TpC				2,6,4
			5.5V	8TpC		8TpC				2,6,4
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.5V		100		100	ns		2,6,4
			5.5V		100		100	ns		2,6,4
8A	TwIL	Int. Request Low Time	3.5V	70		70		ns		2,6,4,5
			5.5V	70		70		ns		2,6,4,5
8B	TwIL	Int. Request Low Time	3.5V	5TpC		5TpC				2,6,4,5
			5.5V	5TpC		5TpC				2,6,4,5
9	TwIH	Int. Request Input High Time	3.5V	5TpC		5TpC				2,6,4,5
			5.5V	5TpC		5TpC				2,6,4,5
10	Twsm	Stop Mode Recovery Width Spec	3.5V	12		12		ns		6,7
			5.5V	12		12		ns		6,7
11	Tost	Oscillator Startup Time	3.5V		5TpC		5TpC			6,7
			5.5V		5TpC		5TpC			6,7

The Z86E43/743/E44 does not reset WDTMR, SMR, P2M, and P3M registers on a Stop-Mode Recovery operation.

$\overline{\text{ROMless}}$ (input, active Low). This pin, when connected to GND, disables the internal ROM and forces the device to function as a Z86C90/C89 ROMless Z8. (Note that, when left unconnected or pulled High to V_{CC}, the device functions nor

Note: *When using in ROM Mode in High EMI (noisy) environment, the ROMless pins should be connected directly to V_{CC}.*

$\overline{\text{DS}}$ (output, active Low). Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of $\overline{\text{DS}}$. For WRITE operations, the falling edge of $\overline{\text{DS}}$ indicates that output data is valid.

$\overline{\text{AS}}$ (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle for external memory transfer. Address output is from Port 0/Port 1 for all external programs. Memory address transfers are valid at the trailing edge of $\overline{\text{AS}}$. Under program control, $\overline{\text{AS}}$ is placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

Port 0 (P07-P00). Port 0 is an 8-bit, bidirectional, CMOS-compatible I/0 port. These eight I/O lines can be configured under software control as a nibble I/0 port, or as an address port for interfacing external memory. The input buffers are Schmitt-triggered and nibble programmed. Either nibble output that can be globally programmed as push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 0 can be placed under handshake control. In Handshake Mode, Port 3 lines P32 and P35 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to Port 0's upper nibble. The lower nibble must have the same direction as the upper nibble.

For external memory references, Port 0 provides address bits A11-A8 (lower nibble) or Al 5-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. In ROMless mode, after a hardware reset, Port 0 is configured as address lines Al 5-A8, and extended timing is set to accommodate slow memory access. The initialization routine can include re-configuration to eliminate this extended timing mode. In ROM mode, Port 0 is defined as input after reset.

Port 0 can be set in the High-Impedance Mode if selected as an address output state, along with Port 1 and the control signals $\overline{\text{AS}}$, $\overline{\text{DS}}$, and R/$\overline{\text{W}}$ (Figure 18).

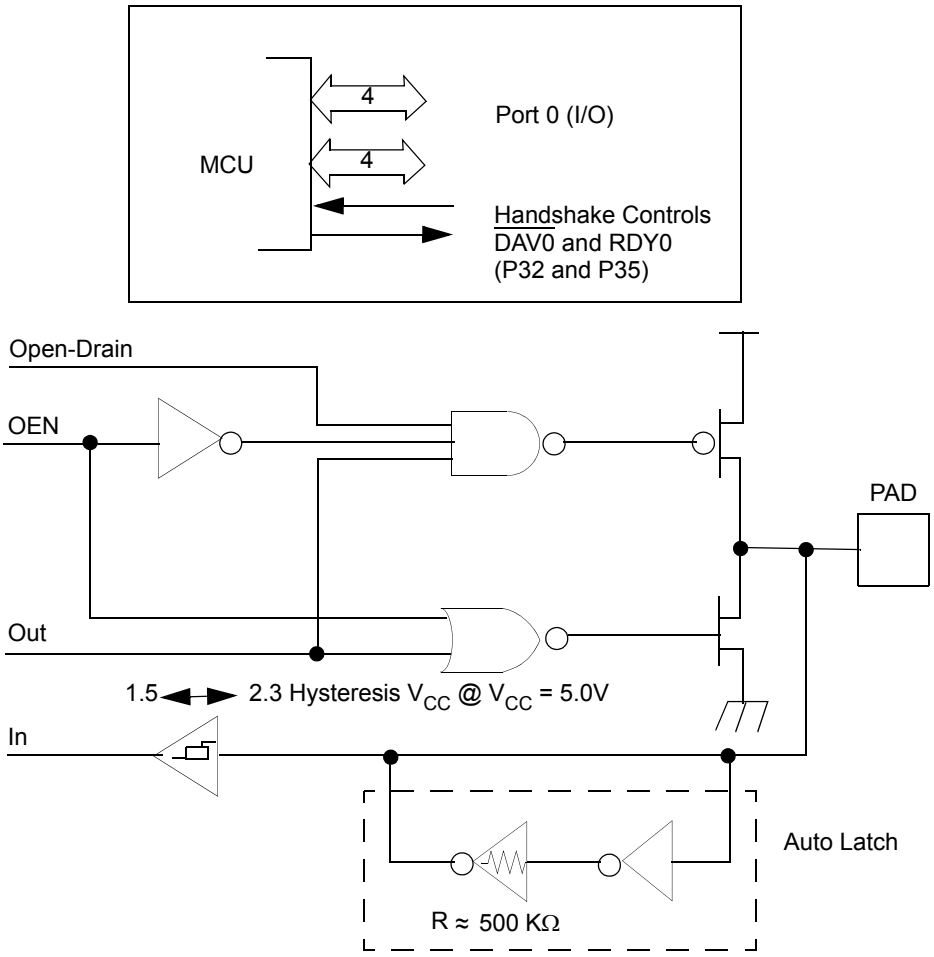


Figure 18. Port 0 Configuration

Port 1 (P17-P10). Port 1 is an 8-bit, bidirectional, CMOS-compatible port with multiplexed Address (A7-A0) and Data (D7-D0) ports. These eight I/O lines can be programmed as inputs or outputs or can be configured under software control as an Address/Data port for interfacing external memory. The input buffers are Schmitt-triggered and the output buffers can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 1 can be placed under handshake control. In this configuration, Port 3, lines P33 and P34 are used as the handshake controls RDY1 and $\overline{\text{DAV1}}$ (Ready and Data Available). To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 outputs the additional lines (see Figure 19).

Functional Description

The MCU incorporates the following special functions to enhance the standard Z8 architecture to provide the user with increased design flexibility.

RESET. The device is reset in one of three ways:

1. Power-On Reset
2. Watchdog Timer
3. Stop Mode Recovery Source

Note: *Having the Auto Power-On Reset circuitry built-in, the MCU does not need to be connected to an external power-on reset circuit. The reset time is T_{POR}. The MCU does not re-initialize WDTMR, SMR, P2M, and P3M registers to their reset values on a Stop Mode Recovery operation.*

Note: *The device V_{CC} must rise up to the operating V_{CC} specification before the T_{POR} expires.*

Program Memory. The MCU can address up to 4/8/16 KB of Internal Program Memory (see Figure 22). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For EPROM mode, byte 12 (000Ch) to address 4095 (0FFFh)/8191 (1FFFh)/16384 (3FFFh), consists of programmable EPROM. After reset, the program counter points at the address 000Ch, which is the starting address of the user program.

In ROMless mode, the Z86E43/743/E44 can address up to 64 KB of External Program Memory. The ROM/ROMless option is only available on the 44-pin devices.

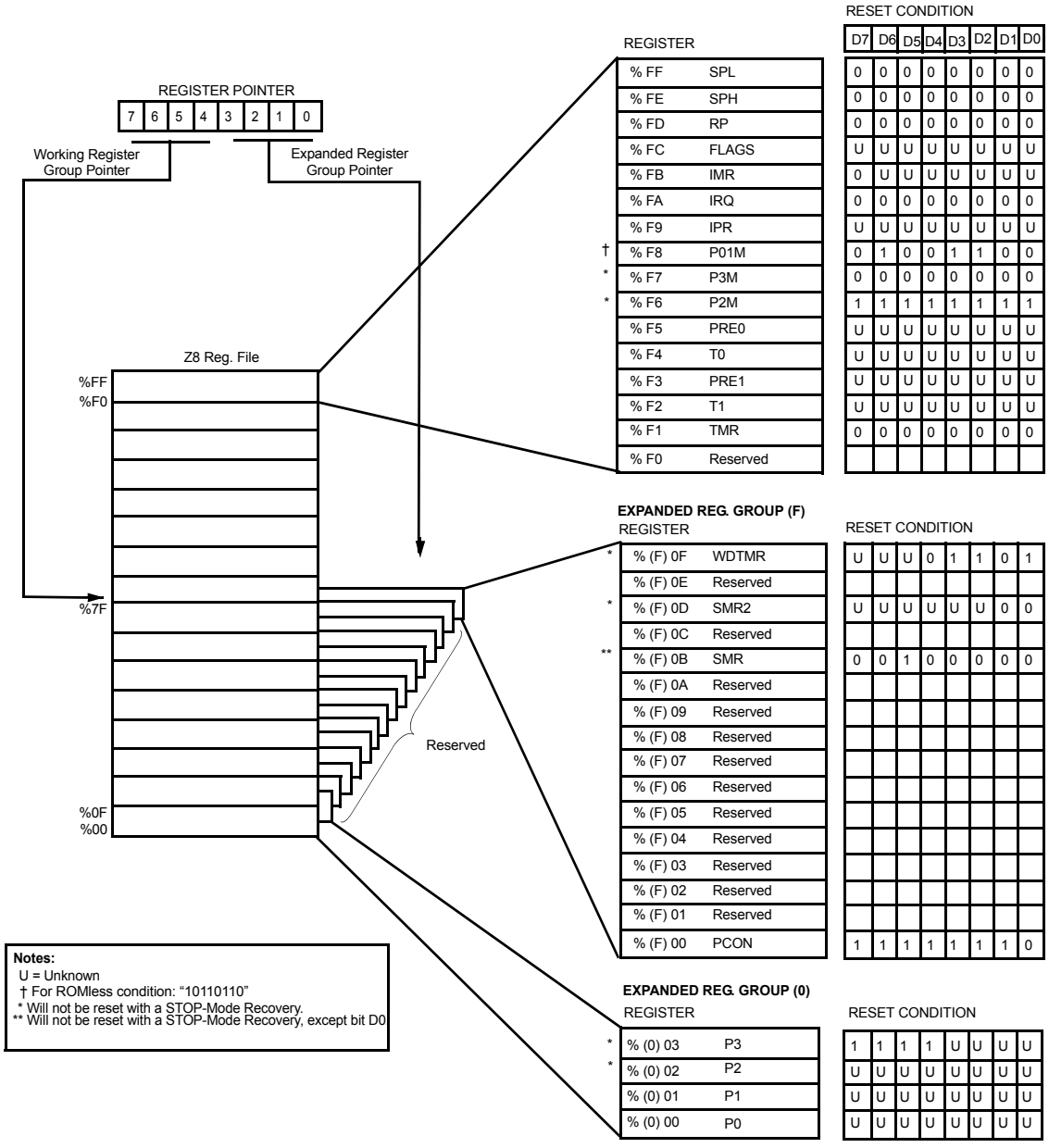


Figure 26. Expanded Register File Architecture

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. The register R254 is general-purpose on Z86E33/733/E34. R254 and R255 are set to 00h after any reset or Stop Mode Recovery.

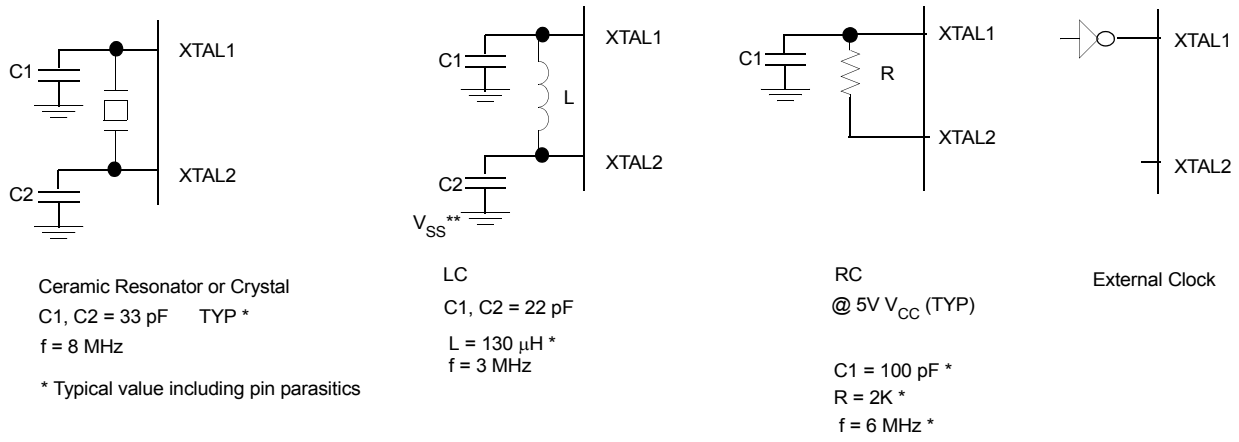


Figure 29. Oscillator Configuration

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR timer allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

1. Power fail to Power OK status
2. Stop Mode Recovery (if D5 of SMR=0)
3. WDT time-out

The POR time is a nominal 5 ms. Bit 5 of the STOP mode Register (SMR) determines whether the POR timer is by-passed after Stop Mode Recovery (typical for an external clock and RC/LC oscillators with fast start up times).

HALT. Turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupt IRQ0, IRQ1, and IRQ2 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT. In order to enter STOP or HALT Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, you must execute a NOP (Opcode = FFh) immediately before the appropriate sleep instruction, that is:

from STOP mode when programmed as analog inputs. When the Stop Mode Recovery sources are selected in this register then SMR2 register bits D0, D1 must be set to zero.

Note: *If the Port 2 pin is configured as an output, this output level will be read by the SMR circuitry.*

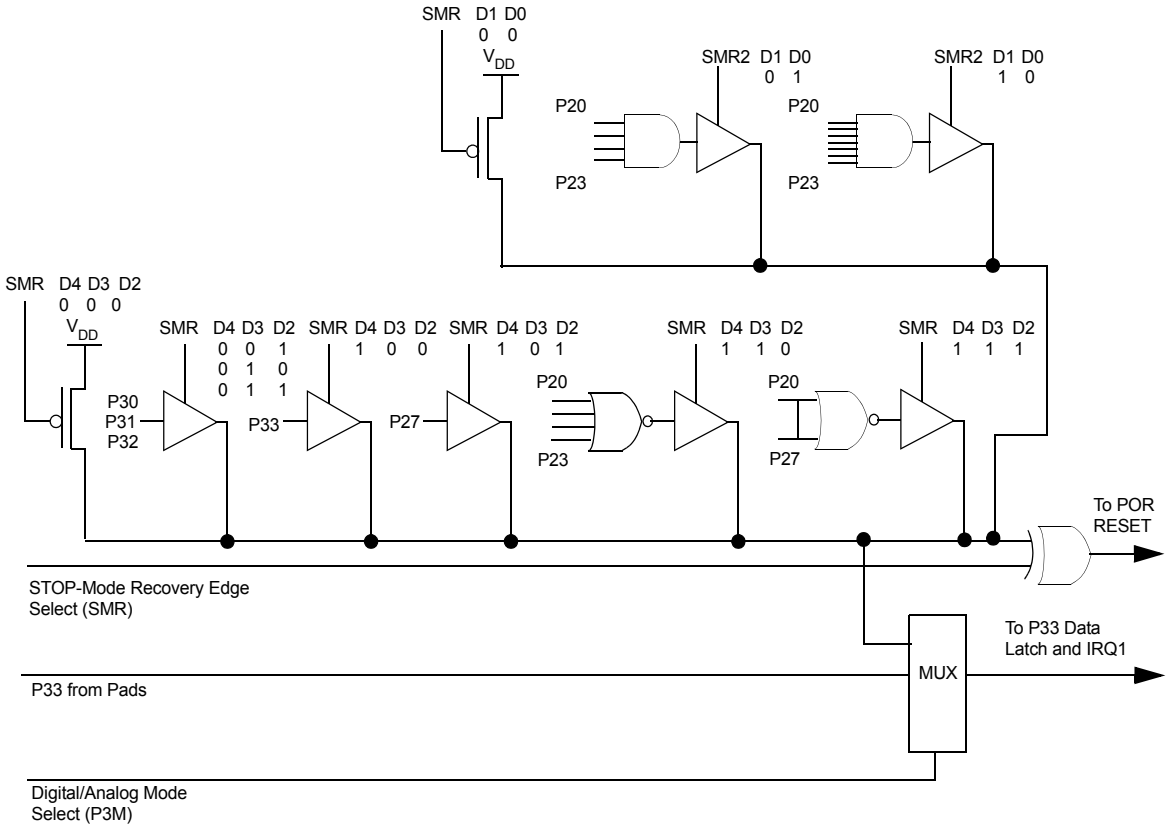


Figure 32. Stop Mode Recovery Source

Table 22. Stop Mode Recovery Source

D4	D3	D2	SMR Source selection
0	0	0	POR recovery only
0	0	1	P30 transition
0	1	0	P31 transition (Not in analog mode)
0	1	1	P32 transition (Not in analog mode)
1	0	0	P33 transition (Not in analog mode)
1	0	1	P27 transition
1	1	0	Logical NOR of Port 2 bits 0-3
1	1	1	Logical NOR of Port 2 bits 0-7

Stop Mode Recovery Delay Select (D5). The 5 ms RESET delay after Stop Mode Recovery is disabled by programming this bit to a zero. A "1" in this bit will cause a 5 ms RESET delay after Stop Mode Recovery. The default condition of this bit is 1. If the fast wake up mode is selected, the Stop Mode Recovery source needs to be kept active for at least 5TpC.

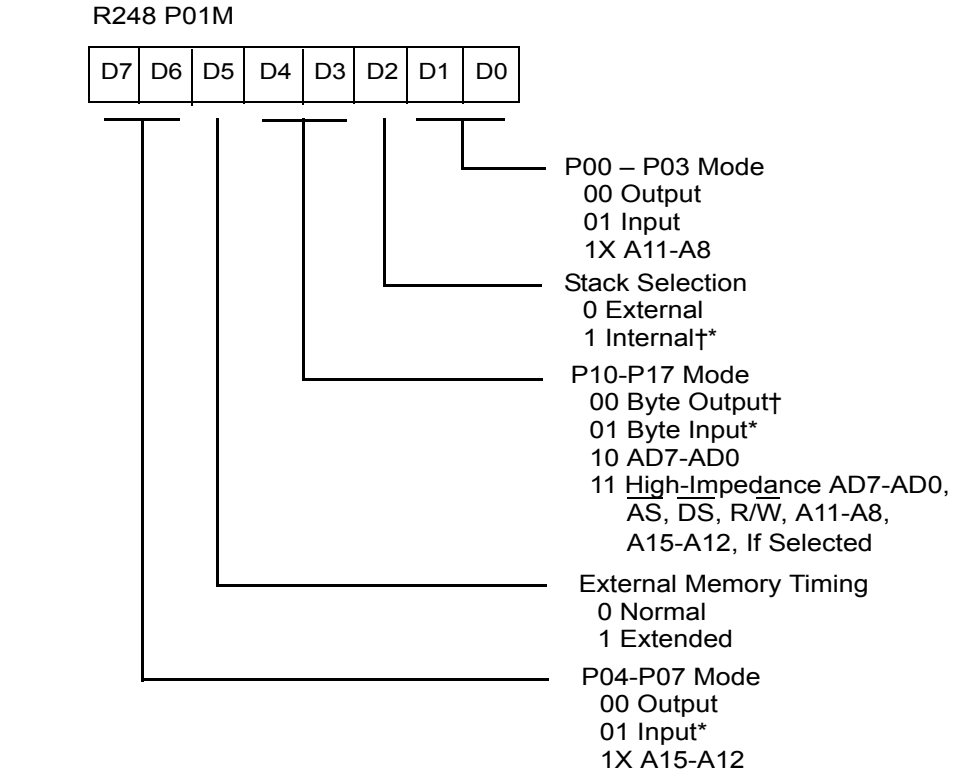
Stop Mode Recovery Level Select (D6). A "1" in this bit defines that a high level on any one of the recovery sources wakes the MCU from STOP Mode. A 0 defines low level recovery. The default value is 0.

Cold or Warm Start (D7). This bit is set by the device upon entering STOP Mode. A "0" in this bit indicates that the device has been reset by POR (cold). A "1" in this bit indicates the device was awakened by a SMR source (warm).

Stop Mode Recovery Register 2 (SMR2). This register contains additional Stop Mode Recovery sources. When the Stop Mode Recovery sources are selected in this register then SMR Register Bits D2, D3, and D4 must be 0.

SMR:10		Operation
D1	DO	Description of Action
0	0	POR and/or external reset recovery
0	1	Logical AND of P20 through P23
1	0	Logical AND of P20 through P27

Watchdog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is disabled after Power-On



Reset Condition = 0100 1101B
For ROMless Condition = 1011 0110B
† Z86E33/733/E34 Must be 00
* Default after Reset

Figure 48. Port 0 and 1 Mode Register ($F8_h$: Write Only)

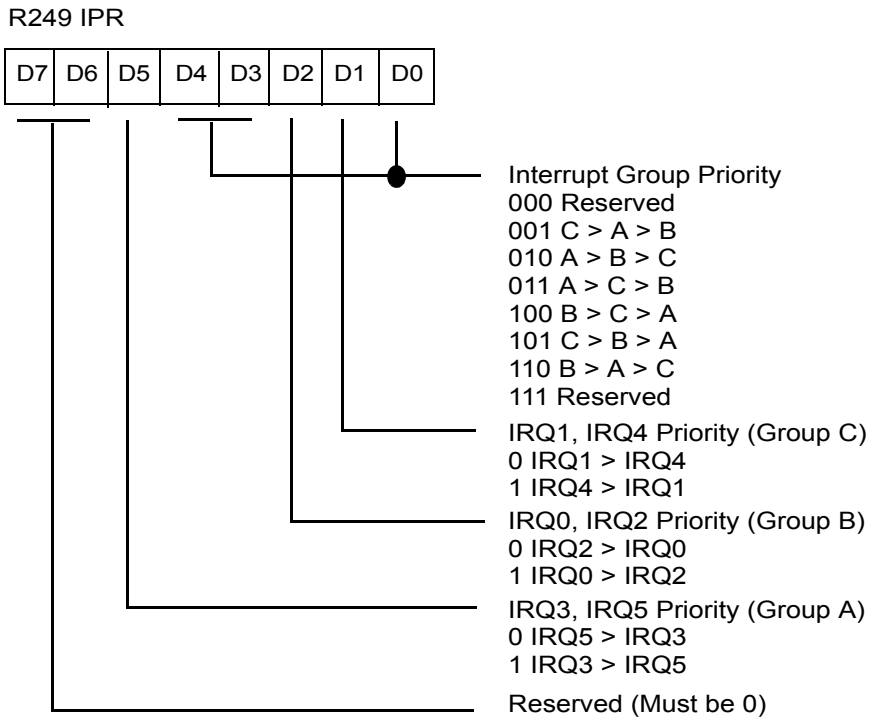


Figure 49. Interrupt Priority Register ($F9_h$: Write Only)

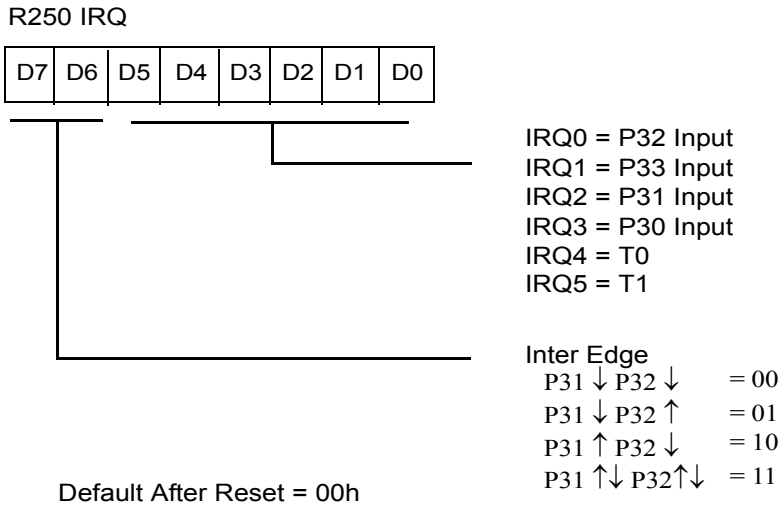


Figure 50. Interrupt Request Register (FA_h: Read/Write)

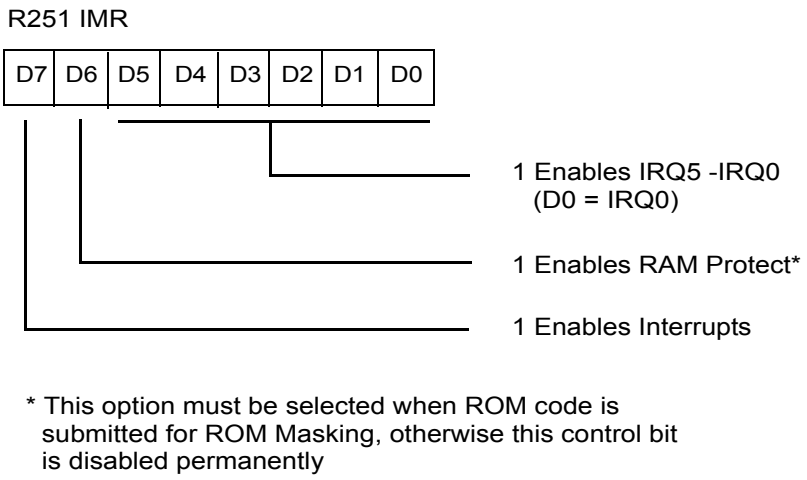


Figure 51. Interrupt Mask Register (FB_h: Read/Write)

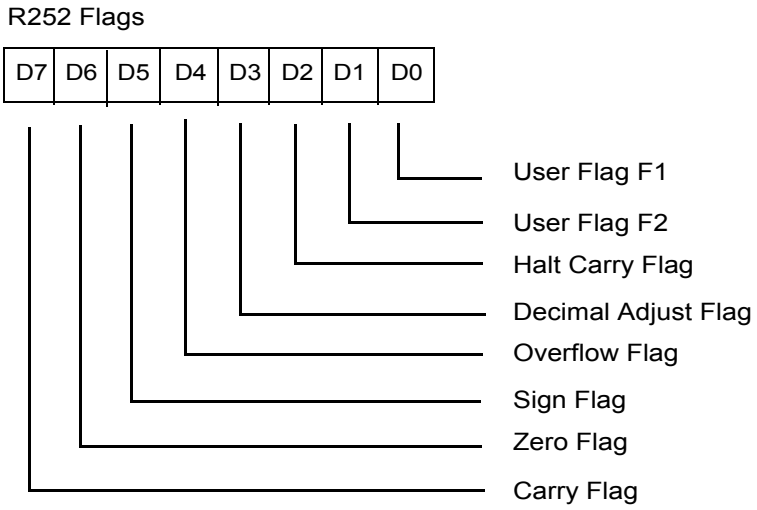
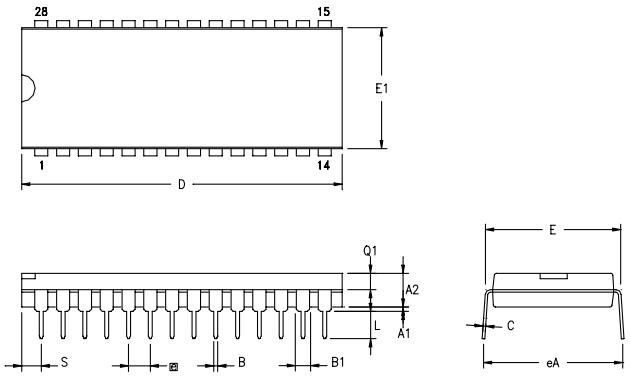


Figure 52. Flag Register (FC_h: Read/Write)

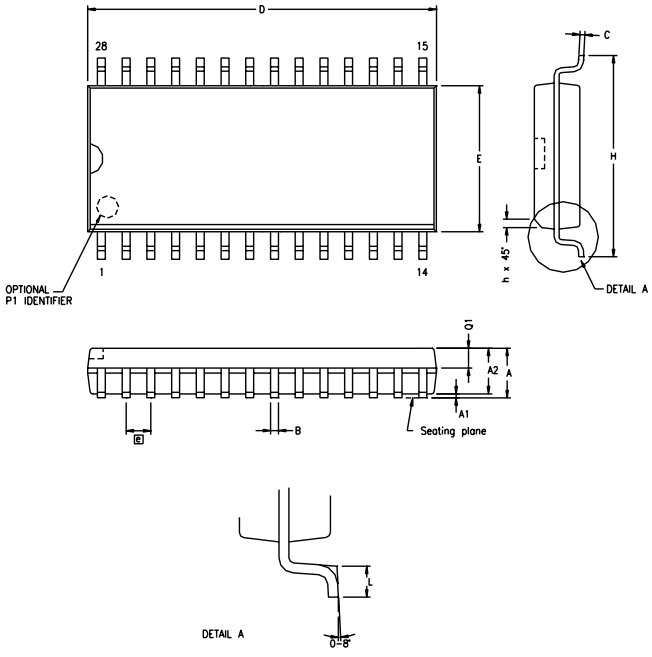


SYMBOL	OPT #	MILLIMETER		INCH	
		MIN	MAX	MIN	MAX
A1		0.38	1.02	.015	.040
A2		3.18	4.19	.125	.165
B		0.38	0.53	.015	.021
B1	01	1.40	1.65	.055	.065
	02	1.14	1.40	.045	.055
C		0.23	0.38	.009	.015
D	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
e		2.54 TYP		.100 TYP	
eA		15.49	16.76	.610	.660
L		3.05	3.81	.120	.150
Q1	01	1.40	1.91	.055	.075
	02	1.40	1.78	.055	.070
S	01	1.52	2.29	.060	.090
	02	1.02	1.52	.040	.060

CONTROLLING DIMENSIONS : INCH

OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

Figure 58. 28-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.64	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	17.78	18.00	.700	.710
E	7.40	7.60	.291	.299
e	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.71	.012	.028
L	0.61	1.00	.024	.039
Q1	0.97	1.09	.038	.043

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 59. 28-Pin SOIC Package Diagram