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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	EBI/EMI
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e3412ssg

Revision History

Each instance in Revision History reflects a change to this document from its previous revision. For more details, refer to the corresponding pages and appropriate links in the table below.

Date	Revision Level	Description	Page No
May 2008	01	Original issue.	All

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Table 2. 40-Pin DIP Pin Identification Standard Mode (Continued)

Pin No	Symbol	Function	Direction
15	XTAL1	Crystal Oscillator	Input
16-18	P31-P33	Port 3, Pins 1,2,3	Input
19	P34	Port 3, Pin 4	Output
20	AS	Address Strobe	Output
21	RESET	Reset	Input
22	P35	Port 3, Pin 5	Output
23	P37	Port 3, Pin 7	Output
24	P36	Port 3, Pin 6	Output
25	P30	Port 3, Pin 0	Input
26-27	P00-P01	Port 0, Pins 0,1	Input/Output
28-29	P10-P11	Port 1, Pins 0,1	Input/Output
30	P02	Port 0, Pin 2	Input/Output
31	GND	Ground	
32-33	P12-P13	Port 1, Pins 2,3	Input/Output
34	P03	Port 0, Pin 3	Input/Output
35-39	P20-P24	Port 2, Pins 0, 1,2,3,4	Input/Output
40	DS	Data Strobe	Output

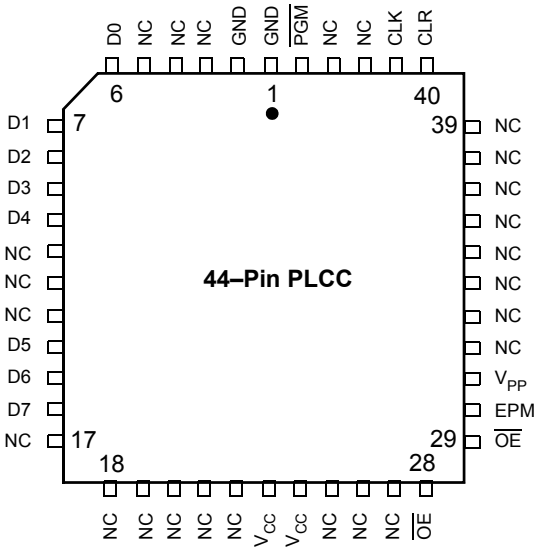


Figure 7. 44-Pin PLCC Pin Configuration EPROM Programming Mode

Table 6. 44-Pin PLCC Pin Configuration EPROM Programming Mode

Pin No	Symbol	Function	Direction
1-2	GND	Ground	
3-5	NC	No Connection	
6-10	D0-D4	Data 0,1,2,3,4	Input/Output
11-13	NC	No Connection	
14-16	D5-D7	Data 5,6,7	Input/Output
17-22	NC	No Connection	
23-24	V_{CC}	Power Supply	
25-27	NC	No Connection	
28	CE	Chip Select	Input
29	OE	Output Enable	Input
30	EPM	EPROM Prog. Mode	Input
31	V_{PP}	Prog. Voltage	Input

Table 6. 44-Pin PLCC Pin Configuration EPROM Programming Mode (Continued)

Pin No	Symbol	Function	Direction
32-39	NC	No Connection	
40	CLR	Clear	Input
41	CLK	Clock	Input
42-43	NC	No Connection	
44	/PGM	Prog. Mode	Input

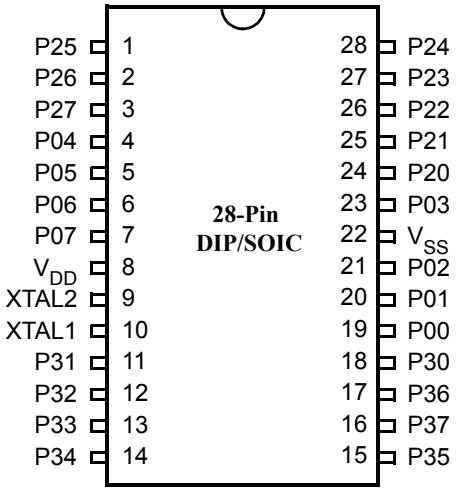


Figure 9. Standard Mode 28-Pin DIP/SOIC Pin Configuration

Table 8. 28-Pin DIP/SOIC/PLCC Pin Identification Standard Mode

Pin No	Symbol	Function	Direction
1-3	P25-P27	Port 2, Pins 5,6,	Input/Output
4-7	P04-P07	Port 0, Pins 4,5,6,7 In/Output	
8	V_{CC}	Power Supply	
9	XTAL2	Crystal Oscillator	Output
10	XTAL1	Crystal Oscillator	Input
11-13	P31-P33	Port 3, Pins 1,2,3	Input
14-15	P34-P35	Port 3, Pins 4,5	Output
16	P37	Port 3, Pin 7	Output
17	P36	Port 3, Pin 6	Output
18	P30	Port 3, Pin 0	Input
19-21	P00-P02	Port 0, Pins 0,1,2	Input/Output
22	V_{SS}	Ground	
23	P03	Port 0, Pin 3	Input/Output
24-28	P20-P24	Port 2, Pins 0,1,2,3,4	Input/Output

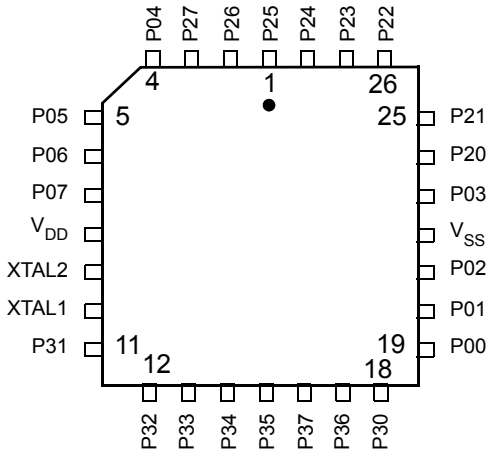


Figure 10. Standard Mode 28-Pin PLCC Pin Configuration

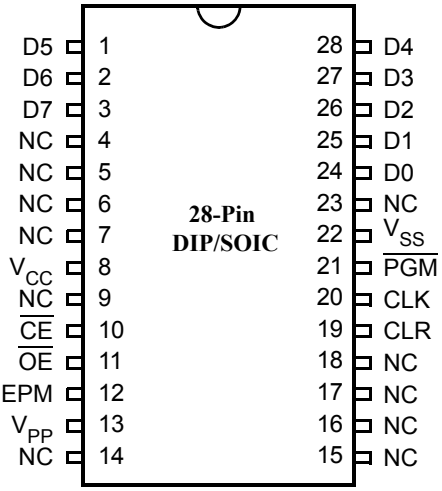


Figure 11. EPROM Programming Mode 28-Pin DIP/SOIC Pin Configuration

Total power dissipation should not exceed 1.21 W for the package. Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{DD} \times [I_{DD} - (\text{sum of } I_{OH}), + \text{sum of } [(V_{DD} - V_{OH}) \times I_{OH}] + \text{sum of } (V_{OL} \times I_{OL})$$

Standard Test Conditions

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Test Load).

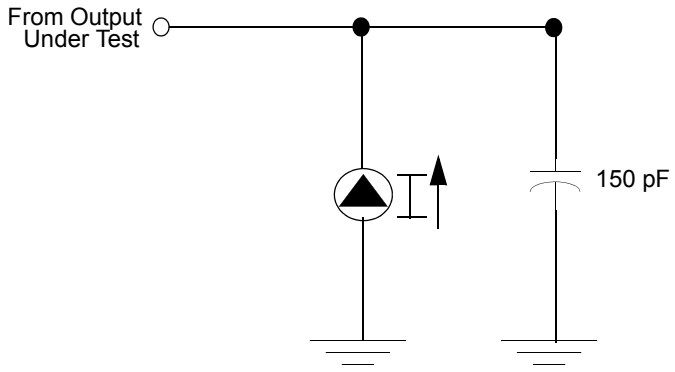


Figure 13. Test Load Diagram

Capacitance

T_A = 25 °C, V_{CC} = GND = 0 V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

Table 12. DC Electrical Characteristics T_A= -40 °C to +105 °C (Continued)

Symbol	Parameter	V_{CC} [1]	Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC2}	Standby Current STOP Mode	4.5V		10	2	µA	V_{IN} = 0V, V_{CC}	7,8,9
		5.5V		10	3	µA	V_{IN} = 0V, V_{CC}	7,8,9
		4.5V		40	10	µA	V_{IN} = 0V, V_{CC}	7,8
		5.5V		40	10	µA	V_{IN} = 0V, V_{CC}	7,8
I_{ALL}	Auto Latch Low Current	4.5V	1.4	20	4.7	µA	0V < V_{IN} < V_{CC}	10
		5.5V	1.4	20	4.7	µA	0V < V_{IN} < V_{CC}	10
I_{ALH}	Auto Latch High Current	4.5V	-1.0	-10	-3.8	µA	0V < V_{IN} < V_{CC}	10
		5.5V	-1.0	-10	-3.8	µA	0V < V_{IN} < V_{CC}	10
T_{POR}	Power-On Reset	4.5V	1.0	14	4	ms		
		5.5V	1.0	14	4	ms		
V_{LV}	Auto Reset Voltage		2.0	3.3	2.8	V		11

Notes

1. The V_{CC} voltage specification of 5.5 V guarantees 5.0 V ± 0.5 V and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V.
2. STD Mode (not Low EMI Mode).
3. Z86E43/743/E44 only.
4. For analog comparator inputs when analog comparators are enabled.
5. All outputs unloaded, I/O pins floating, inputs at rail.
6. CL1=CL2=22 pF.
7. Same as note 5 except inputs at V_{CC}.
8. Clock must be forced Low, when XTAL1 is clock driven and XTAL2.
9. WDT is not running.
10. Auto Latch (mask option) selected.
11. Device does function down to the Auto Reset voltage.

Table 13. DC Electrical Characteristics T_A = 0 °C to +70 °C, 12 MHz (Continued)

No.	Symbol	Parameter	V_{CC} [1]	Min	Max	Units	Notes
4	TwAS	$\overline{AS}$ Low Width	3.5V	55		ns	2
			5.5V	55		ns	2
5	TdAS(DS)	Address Float to $\overline{DS}$ Fall	3.5V	0		ns	
			5.5V	0		ns	
6	TwDSR	$\overline{DS}$ (Read) Low Width	3.5V	200		ns	2,3
			5.5V	200		ns	2,3
7	TwDSW	$\overline{DS}$ (Write) Low Width	3.5V	110		ns	2,3
			5.5V	110		ns	2,3
8	TdDSR(DR)	$\overline{DS}$ Fail to Read Data Req'd Valid	3.5V		150	ns	2,3
			5.5V		150	ns	2,3
9	ThDR(DS)	Read Data to $\overline{DS}$ Rise Hold Time	3.5V	0		ns	2
			5.5V	0		ns	2
10	TdDS(A)	$\overline{DS}$ Rise to Address Active Delay	3.5V	45		ns	2
			5.5V	55		ns	2
11	TdDS(AS)	$\overline{DS}$ Rise to $\overline{AS}$ Fall Delay	3.5V	30		ns	2
			5.5V	45		ns	2
12	TdR/W(AS)	R/$\overline{W}$ Valid to $\overline{AS}$ Rise Delay	3.5V	45		ns	2
			5.5V	45		ns	2
13	TdDS(R/W)	$\overline{DS}$ Rise to R/$\overline{W}$ Not Valid	3.5V	45		ns	2
			5.5V	45		ns	2
14	TdDW(DSW)	Write Data Valid to $\overline{DS}$ Fall (Write) Delay	3.5V	55		ns	2
			5.5V	55		ns	2
15	TdDS(DW)	$\overline{DS}$ Rise to Write Data Not Valid Delay	3.5V	45		ns	2
			5.5V	55		ns	2
16	TdA(DR)	Address Valid to Read Data Req'd Valid	3.5V		310	ns	2,3
			5.5V		310	ns	2,3
17	TdAS(DS)	$\overline{AS}$ Rise to $\overline{DS}$ Fall Delay	3.5V	65		ns	2
			5.5V	65		ns	2

Table 14. DC Electrical Characteristics T_A = -40 °C to +105 °C, 12 MHz (Continued)

No.	Symbol	Parameter	V_{CC}[1]	Min	Max	Units	Notes
10	TdDS(A)	$\overline{DS}$ Rise to Address Active Delay	4.5V	45		ns	2
			5.5V	55		ns	2
11	TdDS(AS)	$\overline{DS}$ Rise to $\overline{AS}$ Fall Delay	4.5V	45		ns	2
			5.5V	45		ns	2
12	TdR/W(AS)	R/$\overline{W}$ Valid to $\overline{AS}$ Rise Delay	4.5V	45		ns	2
			5.5V	45		ns	2
13	TdDS(R/W)	$\overline{DS}$ Rise to R/$\overline{W}$ Not Valid	4.5V	45		ns	2
			5.5V	45		ns	2
14	TdDW(DSW)	Write Data Valid to $\overline{DS}$ Fall (Write) Delay	4.5V	55		ns	2
			5.5V	55		ns	2
15	TdDS(DW)	$\overline{DS}$ Rise to Write Data Not Valid Delay	4.5V	55		ns	2
			5.5V	55		ns	2
16	TdA(DR)	Address Valid to Read Data Req'd Valid	4.5V		310	ns	2,3
			5.5V		310	ns	2,3
17	TdAS(DS)	$\overline{AS}$ Rise to $\overline{DS}$ Fall Delay	4.5V	65		ns	2
			5.5V	65		ns	2
18	TdDM(AS)	$\overline{DM}$ Valid to $\overline{AS}$ Rise Delay	4.5V	35		ns	2
			5.5V	35		ns	2
19	ThDS(AS)	$\overline{DS}$ Valid to Address Valid Hold Time	4.5V	35		ns	2
			5.5V	35		ns	2

Notes

1. The V_{CC} voltage specification of 5.5 V guarantees 5.0 V ± 0.5 V and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V.
2. Timing numbers given are for minimum TpC.
3. When using extended memory timing, add 2 TpC.

Standard Test Load

All timing references use 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

For Standard Mode (not Low-EMI Mode for outputs) with SMR, D1 = 0, D0 = 0.

Table 15. Additional Timing Table (Divide-By-One Mode) T_A = 0 °C to +70 °C (Continued)

No	Symbol	Parameter	V_{CC}[1]	Min	Max	Min	Max	Units	Notes
5	TwTinH	Timer Input High Width	3.5V	5TpC		5TpC			2,3,4
			5.5V	5TpC		5TpC			2,3,4
6	TpTin	Timer Input Period	3.5V	8TpC		8TpC			2,3,4
			5.5V	8TpC		8TpC			2,3,4
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.5V		100		100	ns	2,3,4
			5.5V		100		100	ns	2,3,4
8A	TwIL	Int. Request Low Time	3.5V	100		100		ns	2,3,4,5
			5.5V	70		70		ns	2,3,4,5
8B	TwIL	Int. Request Low Time	3.5V	5TpC		5TpC			2,3,4,6
			5.5V	5TpC		5TpC			2,3,4,6
9	TwIH	Int. Request Input High Time	3.5V	5TpC		5TpC			2,3,4,5
			5.5V	5TpC		5TpC			2,3,4,5
10	Twsm	Stop Mode Recovery Width Spec	3.5V	12		12		ns	4,7
			5.5V	12		12		ns	4,7
11	Tost	Oscillator Startup Time	3.5V		5TpC		5TpC		4,7,8
			5.5V		5TpC		5TpC		4,7,8

Notes

1. The V_{CC} voltage specification of 5.5 V guarantees 5.0 V ± 0.5 V and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V.
2. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC}; for a logic 0.
3. SMR D1 = 0.
4. Maximum frequency for internal system clock is 4 MHz when using Low EMI OSC PCON Bit D7 = 0.
5. Interrupt request via Port 3 (P31-P33).
6. Interrupt request via Port 3 (P30).
7. SMR-D5 = 1, POR STOP Mode Delay is on.
8. For RC and LC oscillator, and for oscillator driven by clock driver.

Table 16. Additional Timing Table (Divide-By-One Mode) T_A = -40 °C to +105 °C

No	Symbol	Parameter	V_{CC}[1]	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	4.5V	250	DC	166	DC	ns	2,3,4
			5.5V	250	DC	166	DC	ns	2,3,4

Table 16. Additional Timing Table (Divide-By-One Mode) T_A = -40 °C to +105 °C (Continued)

No	Symbol	Parameter	V_{CC} [1]	Min	Max	Min	Max	Units	Notes
2	TrC,TfC	Clock Input Rise & Fall Times	4.5V		25		25	ns	2,3,4
			5.5V		25		25	ns	2,3,4
3	TwC	Input Clock Width	4.5V	100		100		ns	2,3,4
			5.5V	100		100		ns	2,3,4
4	TwTinL	Timer Input Low Width	4.5V	100		100		ns	2,3,4
			5.5V	70		70		ns	2,3,4
5	TwTinH	Timer Input High Width	4.5V	5TpC		5TpC			2,3,4
			5.5V	5TpC		5TpC			2,3,4
6	TpTin	Timer Input Period	4.5V	8TpC		8TpC			2,3,4
			5.5V	8TpC		8TpC			2,3,4
7	TrTin, TfTin	Timer Input Rise & Fall Timer	4.5V		100		100	ns	2,3,4
			5.5V		100		100	ns	2,3,4
8A	TwIL	Int. Request Low Time	4.5V	100		100		ns	2,3,4,5
			5.5V	70		70		ns	2,3,4,5
8B	TwIL	Int. Request Low Time	4.5V	5TpC		5TpC			2,3,4,6
			5.5V	5TpC		5TpC			2,3,4,6
9	TwIH	Int. Request Input High Time	4.5V	5TpC		5TpC			2,3,4,5
			5.5V	5TpC		5TpC			2,3,4,5
10	Twsm	Stop Mode Recovery Width Spec	4.5V	12		12		ns	4,7
			5.5V	12		12		ns	4,7
11	Tost	Oscillator Startup Time	4.5V		5TpC		5TpC		4,7,8
			5.5V		5TpC		5TpC		4,7,8

Notes

1. The V_{CC} voltage specification of 5.5 V guarantees 5.0 V ± 0.5 V and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V.
2. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC}; for a logic 0.
3. SMR D1 = 0.
4. Maximum frequency for internal system clock is 4 MHz when using Low EMI OSC PCON Bit D7=0.
5. Interrupt request via Port 3 (P31-P33).
6. Interrupt request via Port 3 (P30).
7. SMR-D5 = 1, POR STOP Mode Delay is on.
8. For RC and LC oscillator, and for oscillator driven by clock driver.

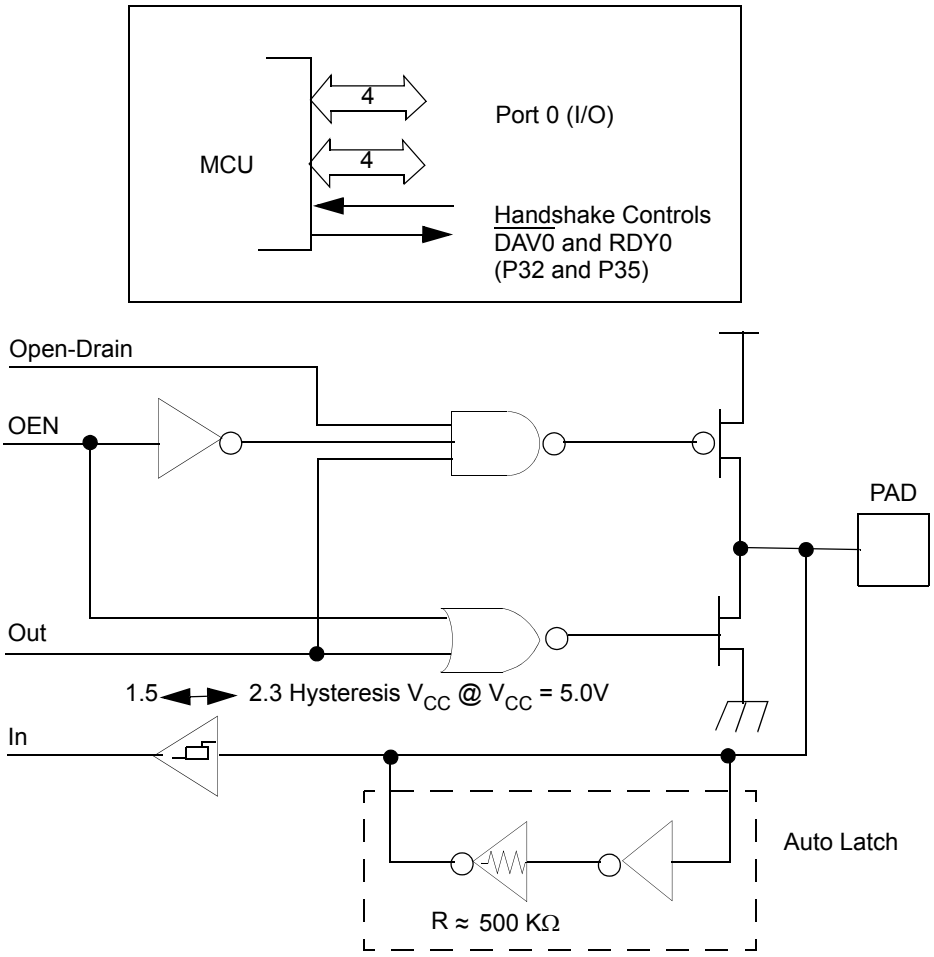


Figure 18. Port 0 Configuration

Port 1 (P17-P10). Port 1 is an 8-bit, bidirectional, CMOS-compatible port with multiplexed Address (A7-A0) and Data (D7-D0) ports. These eight I/O lines can be programmed as inputs or outputs or can be configured under software control as an Address/Data port for interfacing external memory. The input buffers are Schmitt-triggered and the output buffers can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 1 can be placed under handshake control. In this configuration, Port 3, lines P33 and P34 are used as the handshake controls RDY1 and $\overline{\text{DAV1}}$ (Ready and Data Available). To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 outputs the additional lines (see Figure 19).

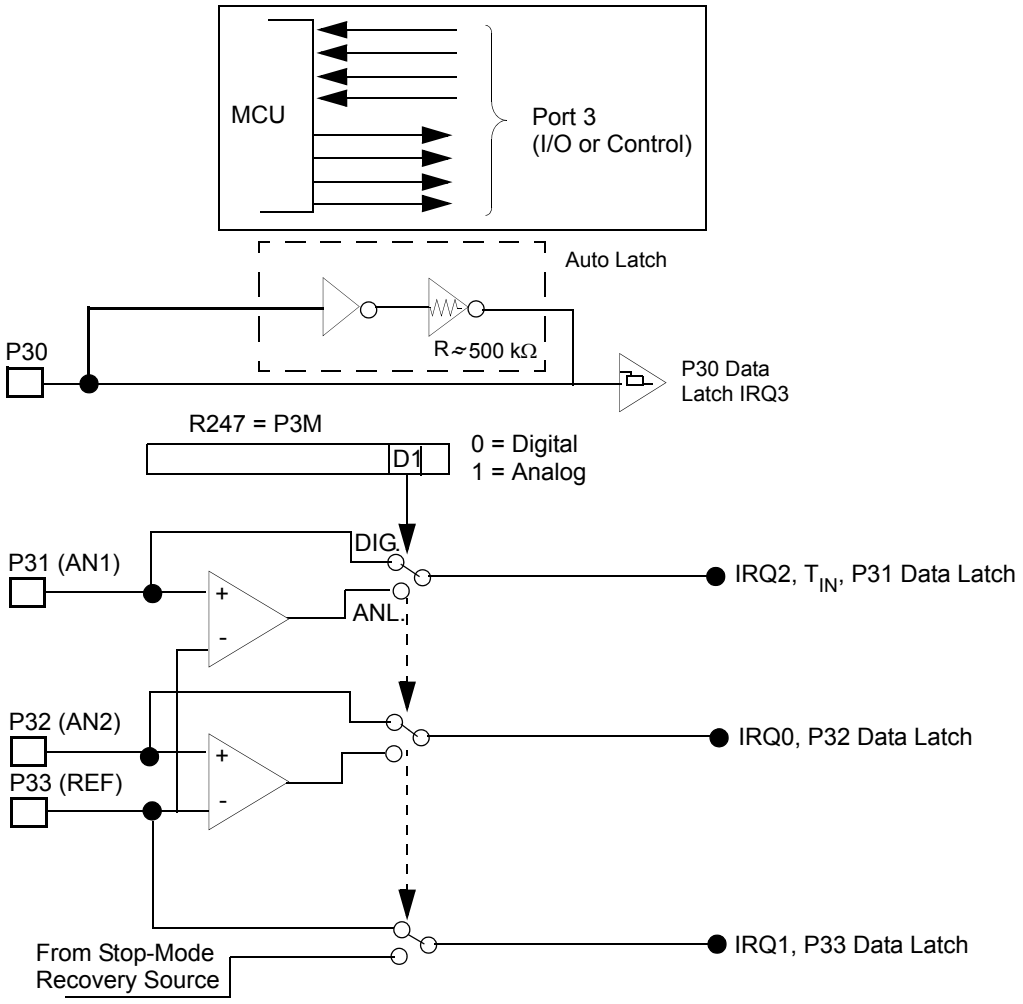


Figure 21. Port 3 Configuration

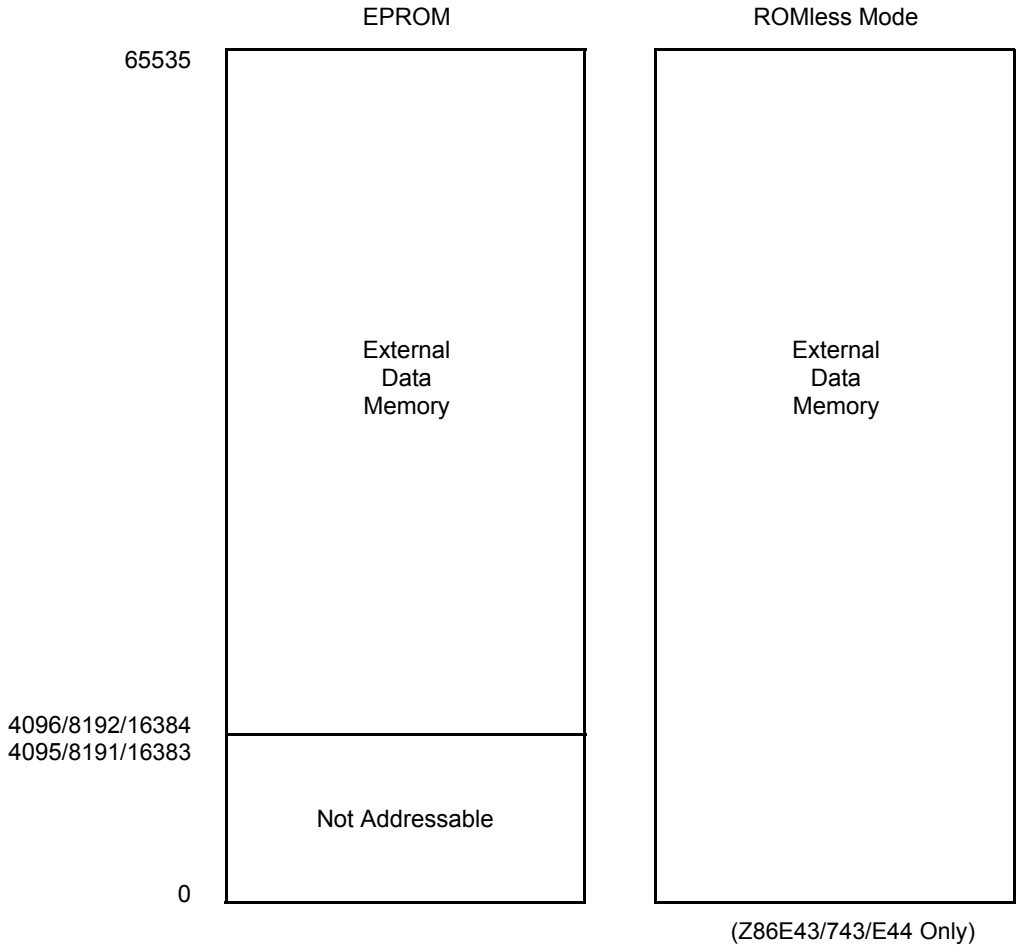


Figure 23. Data Memory Map

Register File. The register file consists of three I/O port registers, 236/125 general-purpose registers, 15 control and status registers, and three system configuration registers in the expanded register group. The instructions can access registers directly or indirectly through an 8-bit address field. This allows a short 4-bit register address using the Register Pointer (see Figure 24). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

Note: *Register Group E0-EF can only be accessed through working register and indirect addressing modes.*

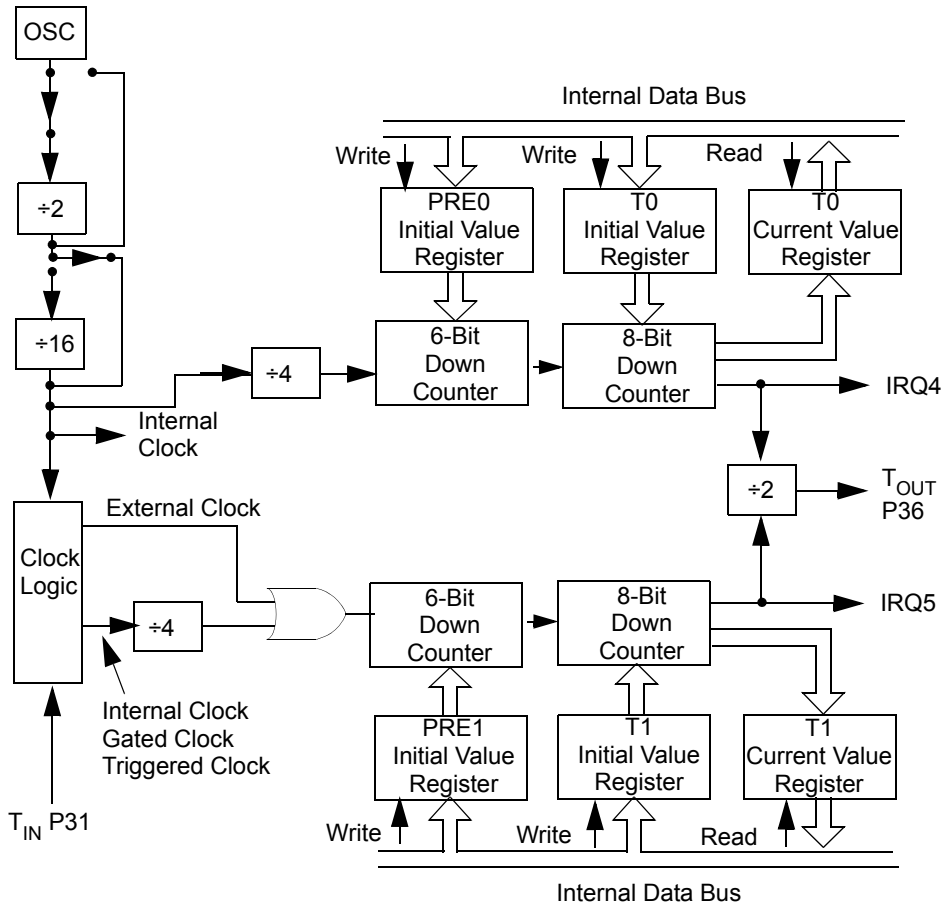


Figure 27. Counter/Timer Block Diagram

Interrupts. The MCU has six different interrupts from six different sources. The interrupts are maskable and prioritized (Figure 28). The six sources are divided as follows: four sources are claimed by Port 3 lines P33-P30) and two in counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 20).

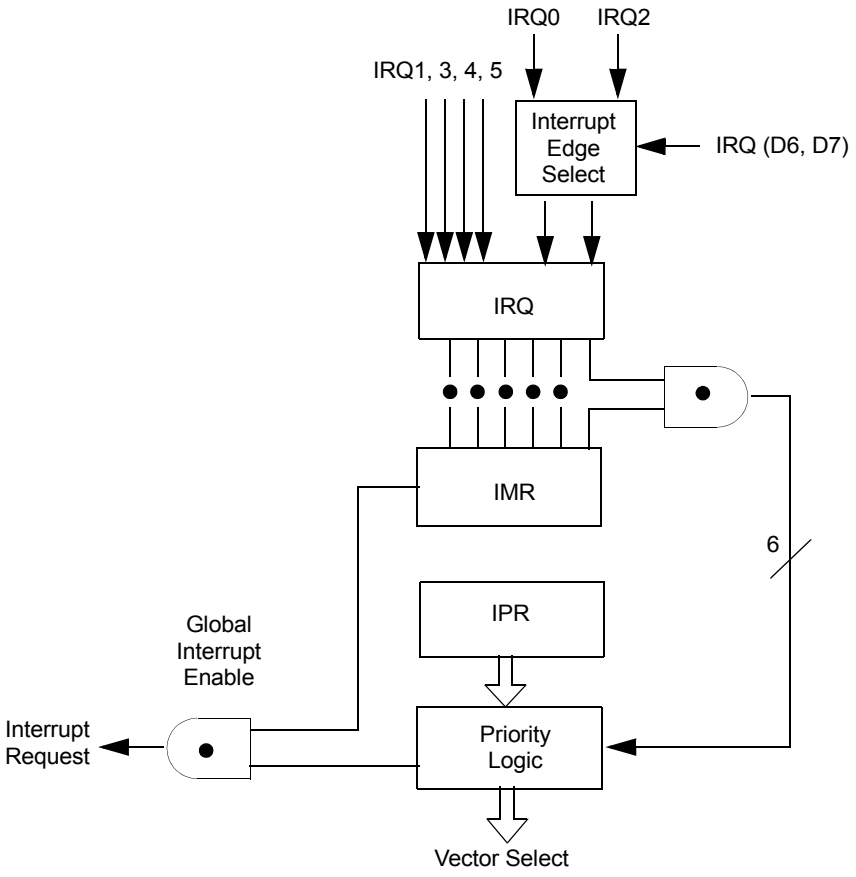
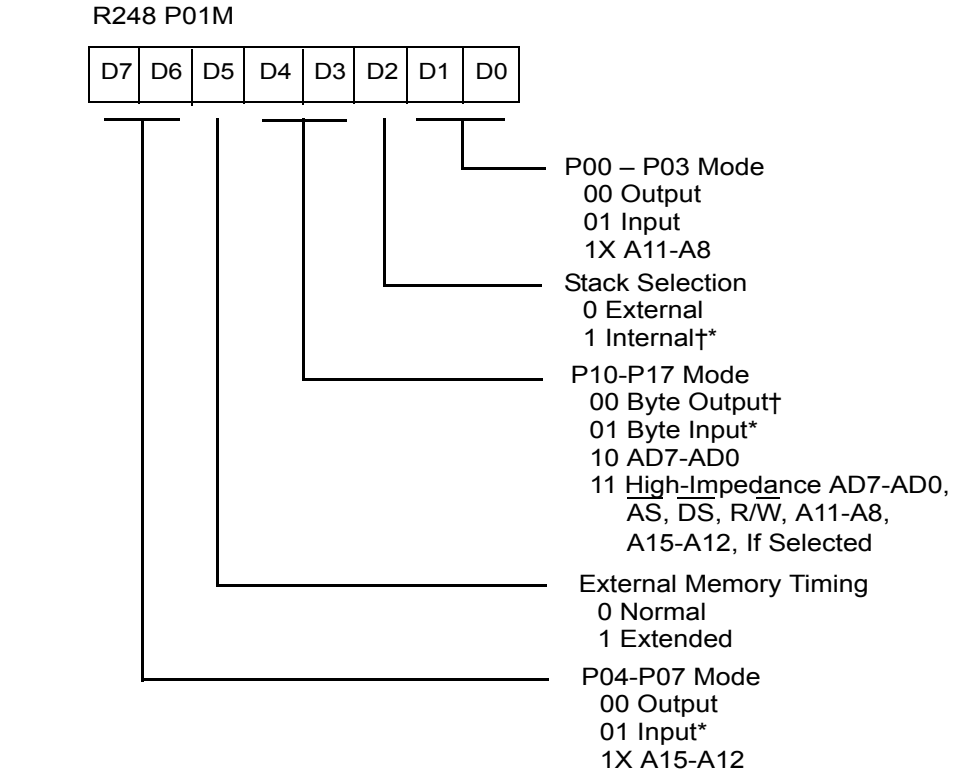


Figure 28. Interrupt Block Diagram

Table 20. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	$\overline{\text{DAV0}}$, IRQ0	0,1	External (P32), Rising/Falling Edge Triggered
IRQ1	IRQ1	2,3	External (P33), Falling Edge Triggered
IRQ2	$\overline{\text{DAV2}}$, IRQ2, T_{IN}	4,5	External (P31), Rising/Falling Edge Triggered
IRQ3	IRQ3	6,7	External (P30), Falling Edge Triggered
1RQ4	T0	8,9	Internal
IRQ5	T1	10,11	Internal



Reset Condition = 0100 1101B
For ROMless Condition = 1011 0110B
† Z86E33/733/E34 Must be 00
* Default after Reset

Figure 48. Port 0 and 1 Mode Register ($F8_h$: Write Only)

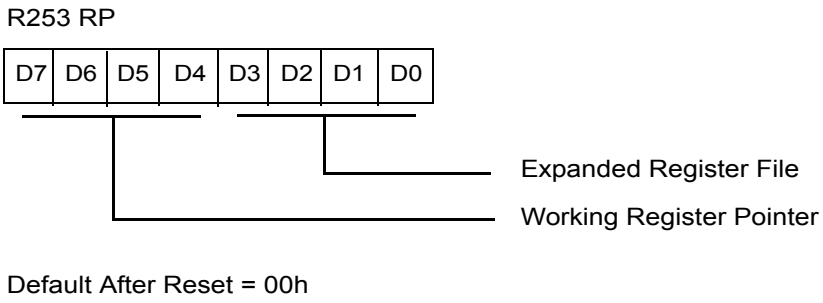


Figure 53. Register Pointer (FD_h: Read/Write)

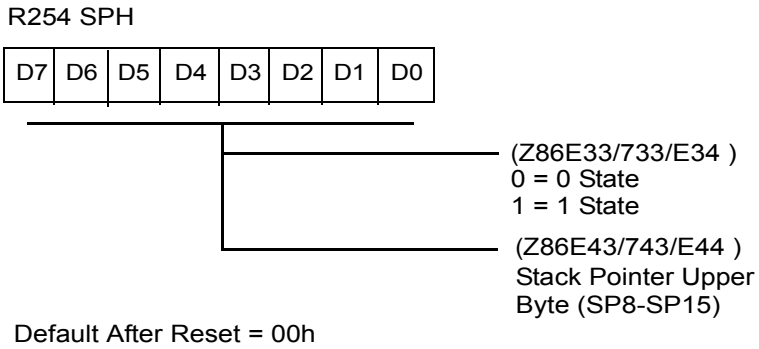


Figure 54. Stack Pointer High (FE_h: Read/Write)

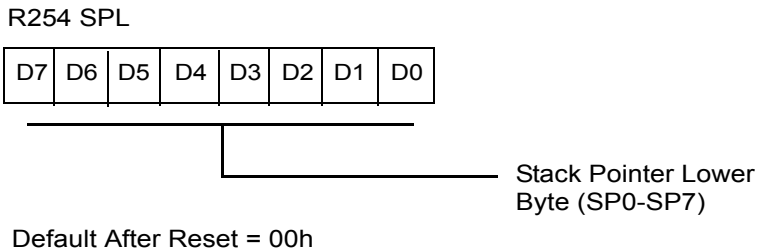


Figure 55. Stack Pointer Low (FF_h: Read/Write)