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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	EBI/EMI
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e3412vsc00tr

Architectural Overview

Zilog's Z86E33/733/E34, E43/743/E44 8-Bit One-Time Programmable (OTP) Microcontrollers are members of Zilog's single-chip Z8® MCU family featuring enhanced wake-up circuitry, programmable Watchdog Timers, Low Noise EMI options, and easy hardware/software system expansion capability.

Four basic address spaces support a wide range of memory configurations. The designer has access to three additional control registers that allow easy access to register mapped peripheral and I/O circuits.

For applications demanding powerful I/O capabilities, the Z86E33/733/E34 have 24 pins, and the Z86E43/743/E44 have 32 pins of dedicated input and output. These lines are grouped into four ports, eight lines per port, and are configurable under software control to provide timing, status signals, and parallel I/O with or without handshake, and address/data bus for interfacing external memory.

Note: *All signals with an overline are active Low. For example, B/$\overline{W}$, for which WORD is active Low, and $\overline{B}$/W, for which BYTE is active Low.*

Power connections follow these conventional descriptions:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Features

Table 1 lists the features of Z86E33/733/E34, E43/743/E44.

Table 1. Z86E33/733/E34, E43/743/E44 Features

Device	ROM (KB)	RAM[1] (Bytes)	I/O Lines	Speed (MHz)
Z86E33	4	237	24	12
Z86733	8	237	24	12
Z86E34	16	237	24	12
Z86E43	4	236	32	12
Z86743	8	236	32	12

Table 2. 40-Pin DIP Pin Identification Standard Mode (Continued)

Pin No	Symbol	Function	Direction
15	XTAL1	Crystal Oscillator	Input
16-18	P31-P33	Port 3, Pins 1,2,3	Input
19	P34	Port 3, Pin 4	Output
20	AS	Address Strobe	Output
21	RESET	Reset	Input
22	P35	Port 3, Pin 5	Output
23	P37	Port 3, Pin 7	Output
24	P36	Port 3, Pin 6	Output
25	P30	Port 3, Pin 0	Input
26-27	P00-P01	Port 0, Pins 0,1	Input/Output
28-29	P10-P11	Port 1, Pins 0,1	Input/Output
30	P02	Port 0, Pin 2	Input/Output
31	GND	Ground	
32-33	P12-P13	Port 1, Pins 2,3	Input/Output
34	P03	Port 0, Pin 3	Input/Output
35-39	P20-P24	Port 2, Pins 0, 1,2,3,4	Input/Output
40	DS	Data Strobe	Output

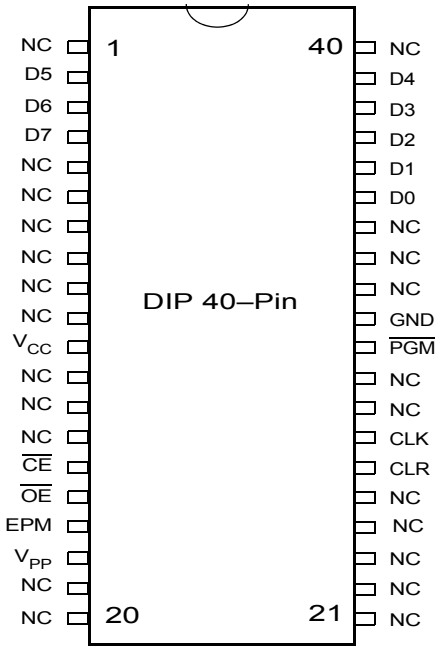


Figure 6. 40-Pin DIP Pin Configuration EPROM Mode

Table 5. 40-Pin DIP Package Pin Identification EPROM Mode

Pin No	Symbol	Function	Direction
1	NC	No Connection	
2-4	D5-D7	Data 5,6,7	Input/Output
5-10	NC	No Connection	
11	V_{CC}	Power Supply	
12-14	NC	No Connection	
15	CE	Chip Select	Input
16	OE	Output Enable	Input
17	EPM	EPROM Prog. Mode	Input
18	V_{PP}	Prog. Voltage	Input
19-25	NC	No Connection	
26	CLR	Clear	Input
27	CLK	Clock	Input
28-29	NC	No Connection	

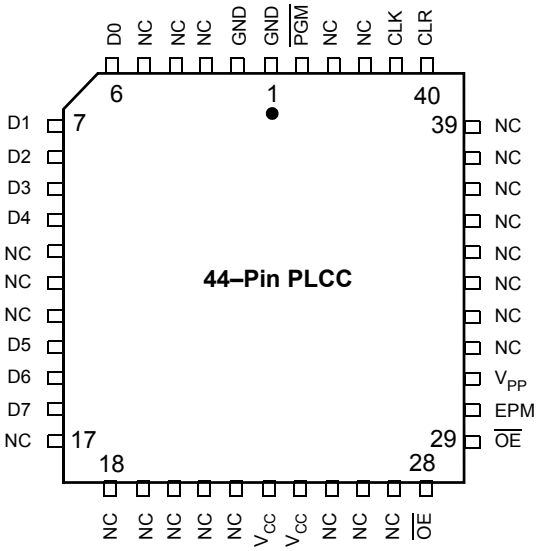


Figure 7. 44-Pin PLCC Pin Configuration EPROM Programming Mode

Table 6. 44-Pin PLCC Pin Configuration EPROM Programming Mode

Pin No	Symbol	Function	Direction
1-2	GND	Ground	
3-5	NC	No Connection	
6-10	D0-D4	Data 0,1,2,3,4	Input/Output
11-13	NC	No Connection	
14-16	D5-D7	Data 5,6,7	Input/Output
17-22	NC	No Connection	
23-24	V_{CC}	Power Supply	
25-27	NC	No Connection	
28	CE	Chip Select	Input
29	OE	Output Enable	Input
30	EPM	EPROM Prog. Mode	Input
31	V_{PP}	Prog. Voltage	Input

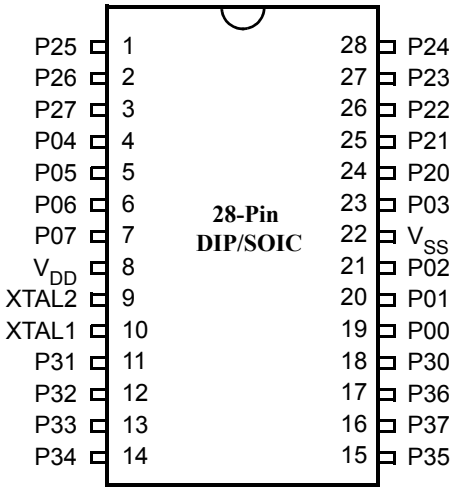


Figure 9. Standard Mode 28-Pin DIP/SOIC Pin Configuration

Table 8. 28-Pin DIP/SOIC/PLCC Pin Identification Standard Mode

Pin No	Symbol	Function	Direction
1-3	P25-P27	Port 2, Pins 5,6,	Input/Output
4-7	P04-P07	Port 0, Pins 4,5,6,7 In/Output	
8	V_{CC}	Power Supply	
9	XTAL2	Crystal Oscillator	Output
10	XTAL1	Crystal Oscillator	Input
11-13	P31-P33	Port 3, Pins 1,2,3	Input
14-15	P34-P35	Port 3, Pins 4,5	Output
16	P37	Port 3, Pin 7	Output
17	P36	Port 3, Pin 6	Output
18	P30	Port 3, Pin 0	Input
19-21	P00-P02	Port 0, Pins 0,1,2	Input/Output
22	V_{SS}	Ground	
23	P03	Port 0, Pin 3	Input/Output
24-28	P20-P24	Port 2, Pins 0,1,2,3,4	Input/Output

The Z86E43/743/E44 does not reset WDTMR, SMR, P2M, and P3M registers on a Stop-Mode Recovery operation.

$\overline{\text{ROMless}}$ (input, active Low). This pin, when connected to GND, disables the internal ROM and forces the device to function as a Z86C90/C89 ROMless Z8. (Note that, when left unconnected or pulled High to V_{CC}, the device functions nor

Note: *When using in ROM Mode in High EMI (noisy) environment, the ROMless pins should be connected directly to V_{CC}.*

$\overline{\text{DS}}$ (output, active Low). Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of $\overline{\text{DS}}$. For WRITE operations, the falling edge of $\overline{\text{DS}}$ indicates that output data is valid.

$\overline{\text{AS}}$ (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle for external memory transfer. Address output is from Port 0/Port 1 for all external programs. Memory address transfers are valid at the trailing edge of $\overline{\text{AS}}$. Under program control, $\overline{\text{AS}}$ is placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

Port 0 (P07-P00). Port 0 is an 8-bit, bidirectional, CMOS-compatible I/0 port. These eight I/O lines can be configured under software control as a nibble I/0 port, or as an address port for interfacing external memory. The input buffers are Schmitt-triggered and nibble programmed. Either nibble output that can be globally programmed as push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 0 can be placed under handshake control. In Handshake Mode, Port 3 lines P32 and P35 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to Port 0's upper nibble. The lower nibble must have the same direction as the upper nibble.

For external memory references, Port 0 provides address bits A11-A8 (lower nibble) or Al 5-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. In ROMless mode, after a hardware reset, Port 0 is configured as address lines Al 5-A8, and extended timing is set to accommodate slow memory access. The initialization routine can include re-configuration to eliminate this extended timing mode. In ROM mode, Port 0 is defined as input after reset.

Port 0 can be set in the High-Impedance Mode if selected as an address output state, along with Port 1 and the control signals $\overline{\text{AS}}$, $\overline{\text{DS}}$, and R/$\overline{\text{W}}$ (Figure 18).

Port 1 can be placed in the high-impedance state along with Port 0, $\overline{AS}$, $\overline{DS}$, and R/$\overline{W}$, allowing the Z86E43/743/E44 to share common resources in multiprocessor and DMA applications. In ROM mode, Port 1 is defined as input after reset.

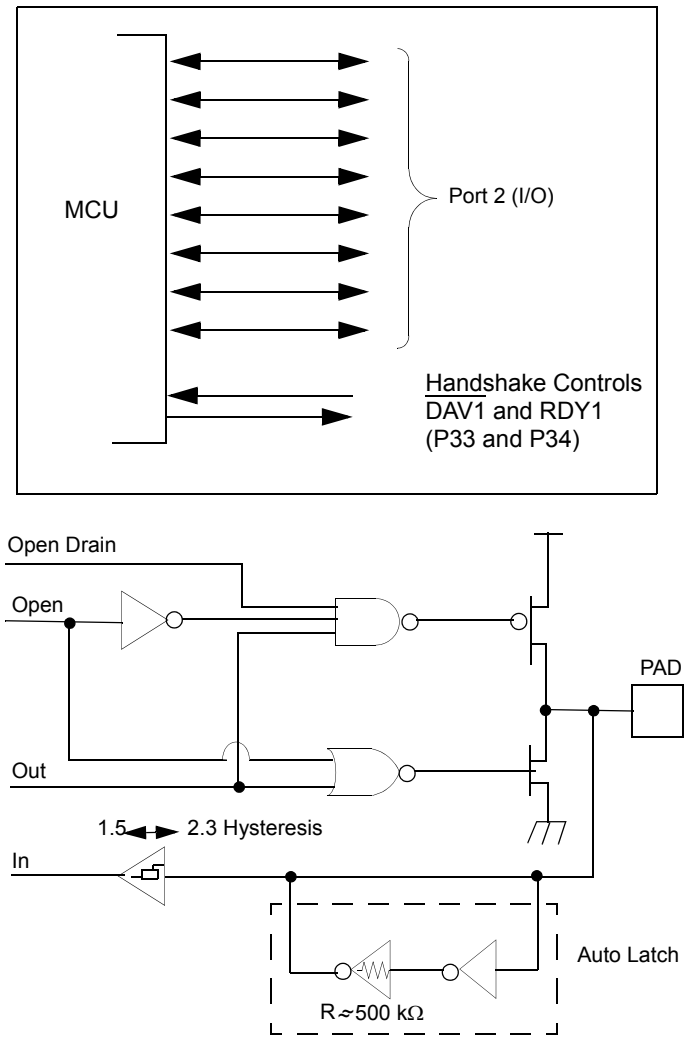


Figure 19. Port 1 Configuration (Z86E43/743/E44 Only)

Port 2 (P27-P20). Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port. These eight I/O lines can be configured under software control as an input or output, independently. All input buffers are Schmitt-triggered. Bits programmed as outputs can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. When used as an I/O port, Port 2 can be placed under handshake control. After reset, Port 2 is defined as an input.

Table 19. Port 3 Pin Assignments

Pin	I/O	CTC1	Analog	Interrupt	P0 HS	P1 HS	P2 HS	Ext
P30	IN			IRQ3				
P31	IN	T_{IN}	AN1	IRQ2		D/R		
P32	IN		AN2	IRQ0	D/R			
P33	IN		REF	IRQ1		D/R		
P34	OUT		AN1-Out			R/D		DM
P35	OUT				R/D			
P36	OUT	T_{OUT}				R/D		
P37	OUT		An2-Out					

Comparator Inputs. Port 3, P31, and P32, each have a comparator front end. The comparator reference voltage P33 is common to both comparators. In analog mode, P31 and P32 are the positive input of the comparators and P33 is the reference voltage of the comparators.

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs (except P33-P31) that are not externally driven. Whether this level is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer. Auto Latches are available on Port 0, Port 1, Port 2, and P30. There are no Auto Latches on P31, P32, and P33.

Low EMI Emission. The Z86E43/743/E44 can be programmed to operate in a low EMI Emission Mode in the PCON register. The oscillator and all I/O ports can be programmed as low EMI emission mode independently. Use of this feature results in:

- The pre-drivers slew rate reduced to 10 ns typical.
- Low EMI output drivers have resistance of 200 Ohms (typical).
- Low EMI Oscillator.
- Internal SCLK/TCLK= XTAL operation limited to a maximum of 4 MHz - 250 ns cycle time, when Low EMI Oscillator is selected.

Note: *For emulation only:*
Do not set the emulator to emulate Port 1 in low EMI mode. Port 1 must always be configured in Standard Mode.

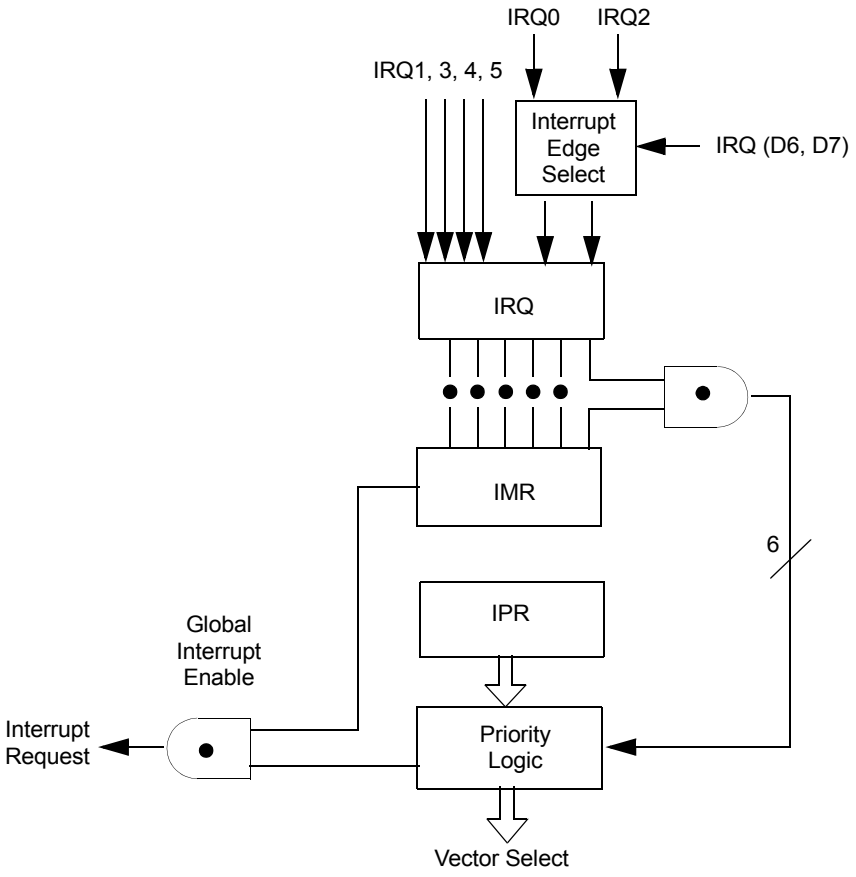


Figure 28. Interrupt Block Diagram

Table 20. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	$\overline{\text{DAV0}}$, IRQ0	0,1	External (P32), Rising/Falling Edge Triggered
IRQ1	IRQ1	2,3	External (P33), Falling Edge Triggered
IRQ2	$\overline{\text{DAV2}}$, IRQ2, T_{IN}	4,5	External (P31), Rising/Falling Edge Triggered
IRQ3	IRQ3	6,7	External (P30), Falling Edge Triggered
1RQ4	T0	8,9	Internal
IRQ5	T1	10,11	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority Register (IPR). An interrupt machine cycle is activated when an interrupt request is granted. Thus, disabling all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests need service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling or both edge triggered, and are programmable by the user. The software may poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in bits D7 and D6 of the IRQ Register (R250). The configuration is shown in Table 21.

Table 21. IRQ Register Configuration

IRO		Interrupt Edge	
D7	**D6**	**P31**	**P32**
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes
1. F = Falling Edge
2. R = Rising Edge

Clock. The on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, RC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 10 kHz to 16 MHz max, with a series resistance (RS) less than or equal to 100 Ω.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's recommended capacitor values from each pin directly to device pin Ground. The RC oscillator option can be selected in the programming mode. The RC oscillator configuration must be an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to Ground (Table 29).

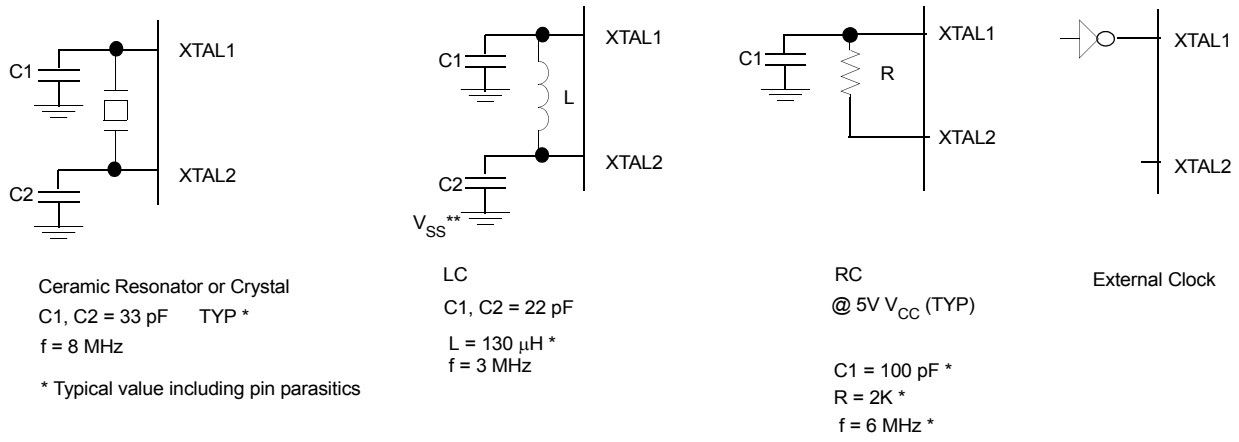


Figure 29. Oscillator Configuration

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR timer allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

1. Power fail to Power OK status
2. Stop Mode Recovery (if D5 of SMR=0)
3. WDT time-out

The POR time is a nominal 5 ms. Bit 5 of the STOP mode Register (SMR) determines whether the POR timer is by-passed after Stop Mode Recovery (typical for an external clock and RC/LC oscillators with fast start up times).

HALT. Turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupt IRQ0, IRQ1, and IRQ2 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT. In order to enter STOP or HALT Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, you must execute a NOP (Opcode = FFh) immediately before the appropriate sleep instruction, that is:

Comparator Output Port 3 (D0). Bit 0 controls the comparator output in Port 3. A "1" in this location brings the comparator outputs to P34 and P37, and a "0" releases the Port to its standard I/O configuration. The default value is 0.

Port 1 Open-Drain (D1). Port 1 can be configured as an open-drain by resetting this bit (D1=0) or configured as push-pull active by setting this bit (D1=1). The default value is 1.

Port 0 Open-Drain (D2). Port 0 can be configured as an open-drain by resetting this bit (D2=0) or configured as push-pull active by setting this bit (D2=1). The default value is 1.

Low EMI Port 0 (D3). Port 0 can be configured as a Low EMI Port by resetting this bit (D3=0) or configured as a Standard Port by setting this bit (D3=1). The default value is 1.

Low EMI Port 1 (D4). Port 1 can be configured as a Low EMI Port by resetting this bit (D4=0) or configured as a Standard Port by setting this bit (D4=1). The default value is 1.

Note: *The emulator does not support Port 1 low EMI mode and must be set D4 = 1.*

Low EMI Port 2 (D5). Port 2 can be configured as a Low EMI Port by resetting this bit (D5=0) or configured as a Standard Port by setting this bit (D5=1). The default value is 1.

Low EMI Port 3 (D6). Port 3 can be configured as a Low EMI Port by resetting this bit (D6=0) or configured as a Standard Port by setting this bit (D6=1). The default value is 1.

Low EMI OSC (D7). This bit of the PCON Register controls the low EMI noise oscillator. A "1" in this location configures the oscillator with standard drive. While a "0" configures the oscillator with low noise drive, however, it does not affect the relationship of SCLK and XTAL. The low EMI mode will reduce the drive of the oscillator (OSC). The default value is 1.

Note: *4 MHz is the maximum external clock frequency when running in the low EMI oscillator mode.*

Stop-Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of Stop Mode Recovery (Figure 31). All bits are Write Only except bit 7 which is a Read Only. Bit 7 is a flag bit that is hardware set on the condition of STOP Recovery and reset by a power-on cycle. Bit 6 controls whether a low or high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4 of the SMR register specify the Stop Mode Recovery Source. The SMR is located in Bank F of the Expanded Register File at address 0BH.

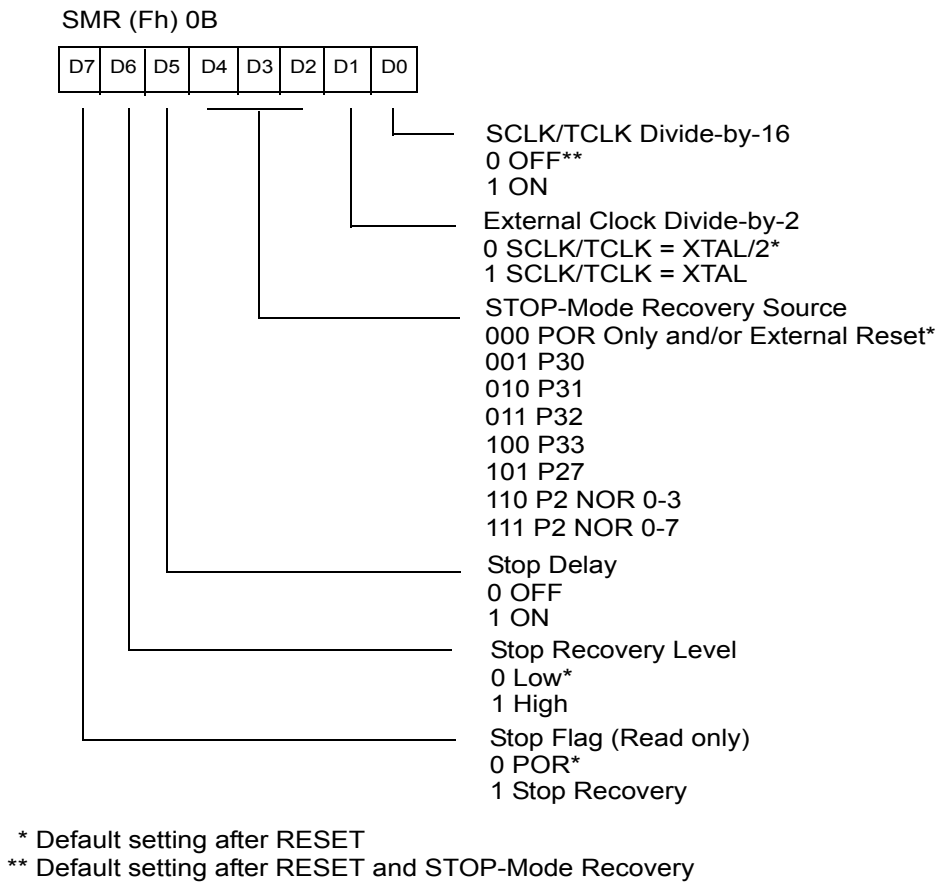


Figure 31. Stop Mode Recovery Register (Write-Only Except Bit D7, Which Is Read-Only)

SCLK/TCLK Divide-by-16 Select (D0). This bit of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources counter/timers and interrupt logic).

External Clock Divide-by-Two (D1). This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, the System Clock (SCLK) and Timer Clock (TCLK) are equal to the external clock frequency divided by two. The SCLK/TCLK is equal to the external clock frequency when this bit is set (D1=1). Using this bit together with D7 of PCON further helps lower EMI (that is, D7 (PCON) = 0, D1 (SMR) = 1). The default setting is zero.

Stop Mode Recovery Source (D2, D3, and D4). These three bits of the SMR register specify the wake up source of the Stop Mode Recovery (Figure 32). Table 22 shows the SMR source selected with the setting of D2 to D4. P33-P31 cannot be used to wake up

from STOP mode when programmed as analog inputs. When the Stop Mode Recovery sources are selected in this register then SMR2 register bits D0, D1 must be set to zero.

Note: *If the Port 2 pin is configured as an output, this output level will be read by the SMR circuitry.*

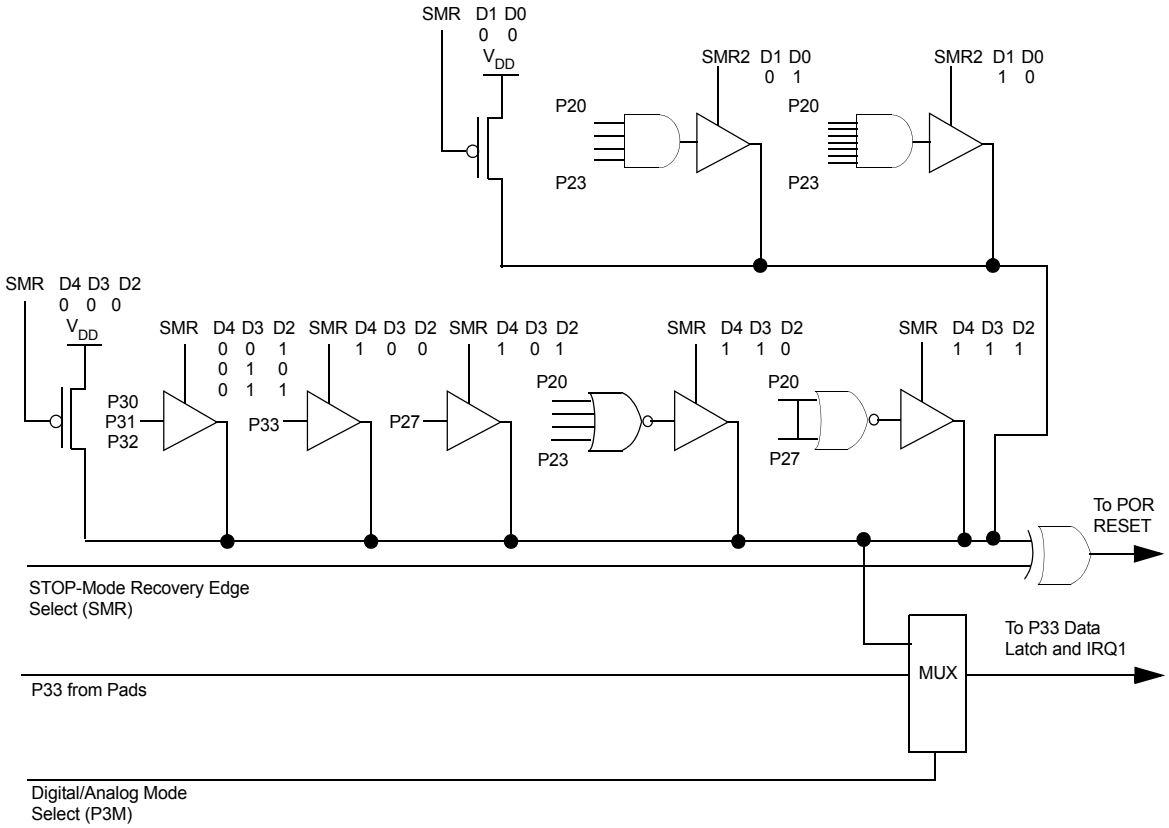


Figure 32. Stop Mode Recovery Source

Reset and initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT is driven either by an on-board RC oscillator or an external oscillator from XTAL1 pin. The POR clock source is selected with bit 4 of the WDT register.

Note: *Execution of the WDT instruction affects the Z (Zero), S (Sign), and V (Overflow) flags.*

WDT Time-Out Period (D0 and D1). Bits 0 and 1 control a tap circuit that determines the time-out periods that can be obtained (Table 23). The default value of DO and Dl are 1 and 0, respectively.

Table 23. Time-out Period of WDT

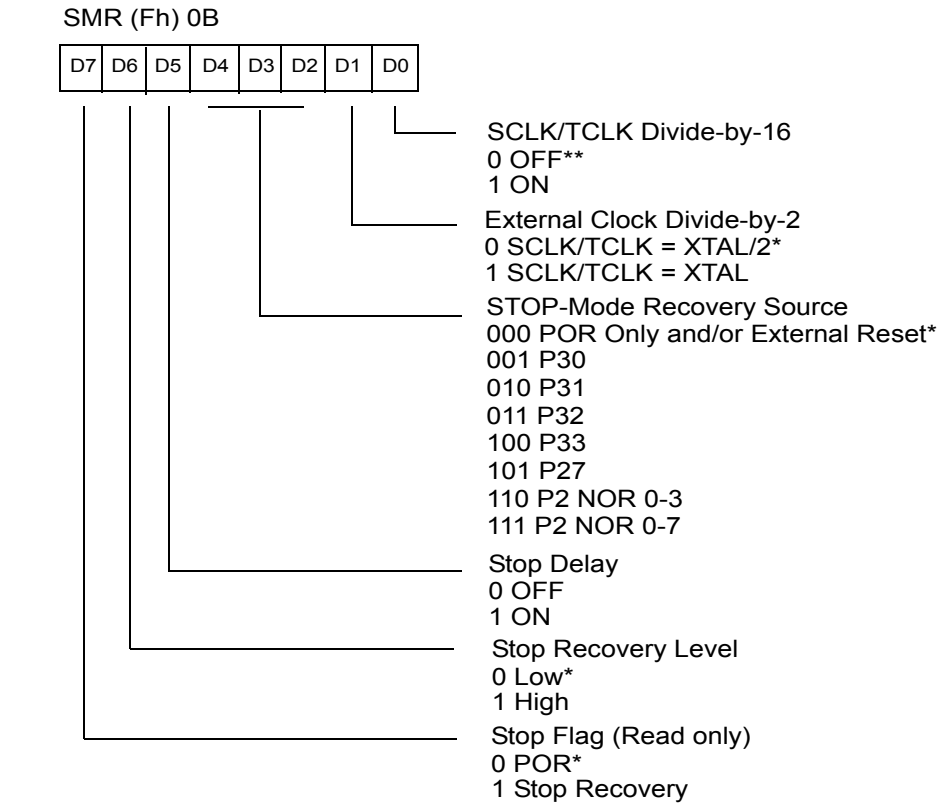
D1	DO	Time-out of the Internal RC OSC	Time-out of the System Clock
0	0	5 ms	128 SCLK
0	1	10 ms[1]	256 SCLK[1]
1	0	20 ms	512 SCLK
1	1	80 ms	2048 SCLK

Note: The default setting is 10 ms.

WDT During HALT Mode (D2). This bit determines whether or not the WDT is active during HALT Mode. A “1” indicates that the WDT is active during HALT. A “0” disables the WDT in HALT Mode. The default value is “1 “. WDT During STOP Mode (D3). This bit determines whether or not the WDT is active during STOP mode. A “1” indicates active during STOP. A “0” disables the WDT during STOP Mode. This is applicable only when the WDT clock source is the internal RC oscillator.

Clock Source For WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1, and the WDT is stopped in STOP Mode. The default configuration of this bit is 0, which selects the RC oscillator.

Permanent WDT. When this feature is enabled, the WDT is enabled after reset and will operate in Run and HALT Mode. The control bits in the WDTMR do not affect the WDT operation. If the clock source of the WDT is the internal RC oscillator, then the WDT will run in STOP mode. If the clock source of the WDT is the XTAL1 pin, then the WDT will not run in STOP mode.



Note: Note used in conjunction with SMR2 Source
* Default setting after RESET
** Default setting after RESET and STOP-Mode Recovery

Figure 37. Stop Mode Recovery Register (Write Only Except Bit D7, Which is Read Only)

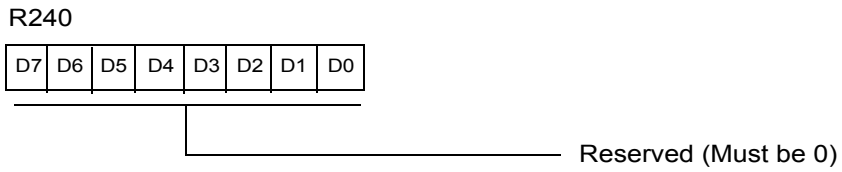


Figure 40. Reserved

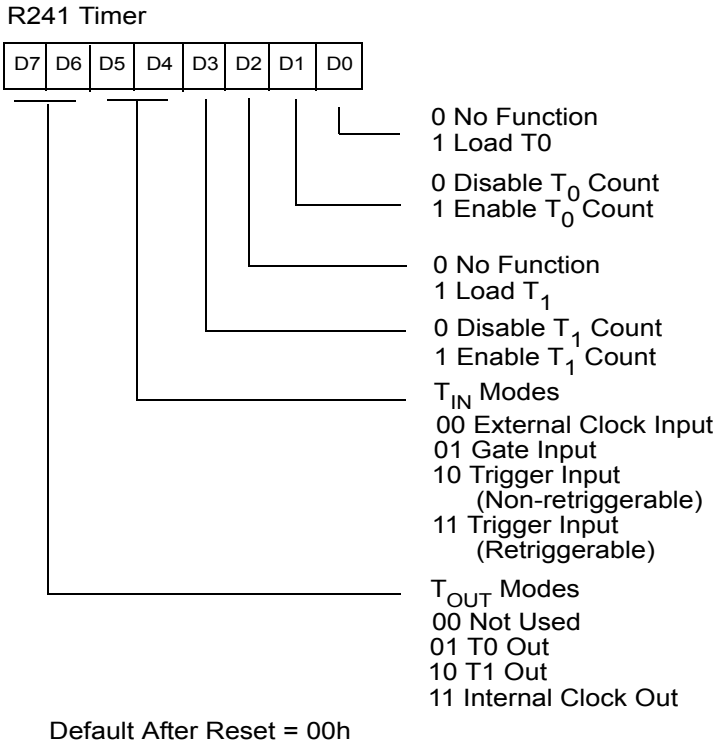


Figure 41. Timer Mode Register ($F1_h$: Read/Write)

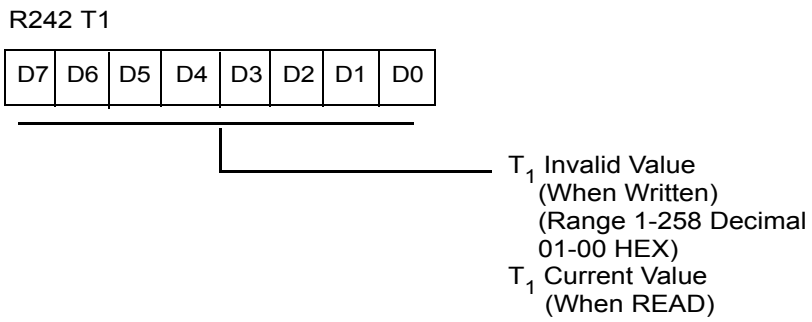


Figure 42. Counter/Timer 1 Register ($F2_h$: Read/Write)

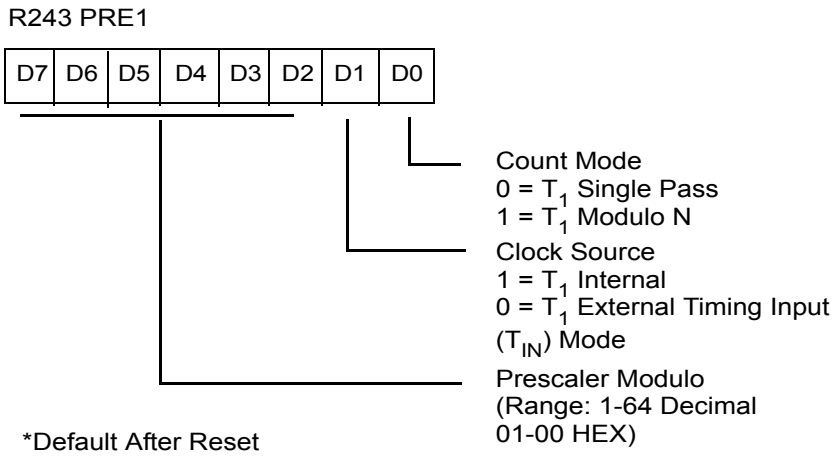


Figure 43. Prescaler 1 Register ($F3_h$: Write Only)

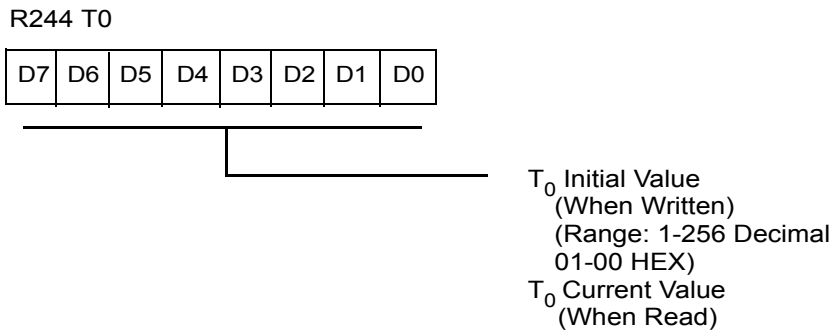


Figure 44. Counter/Timer 0 Register ($F4_h$: Read/Write)

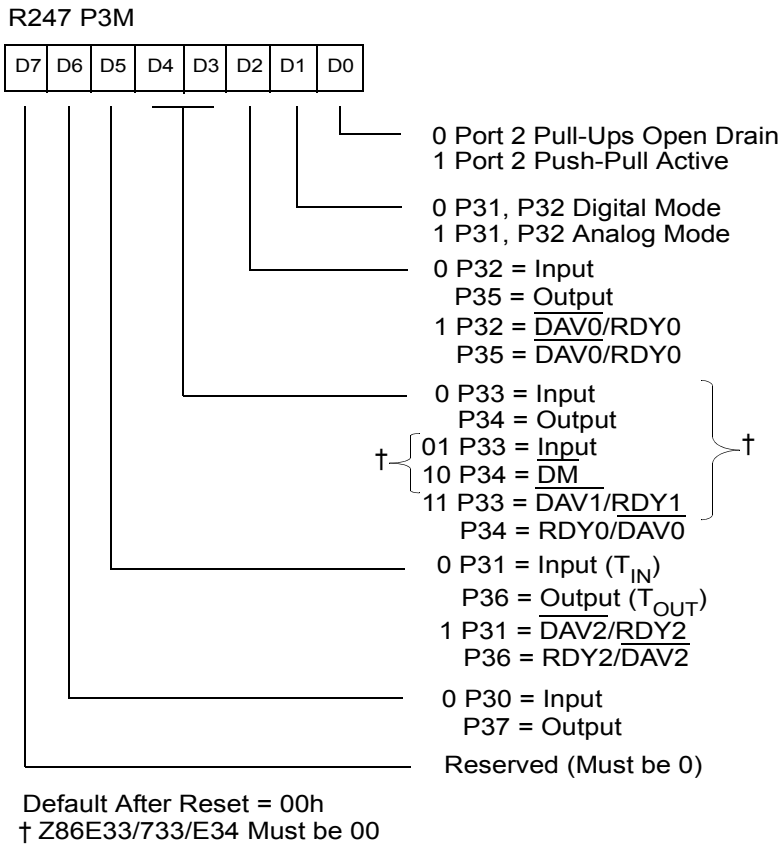
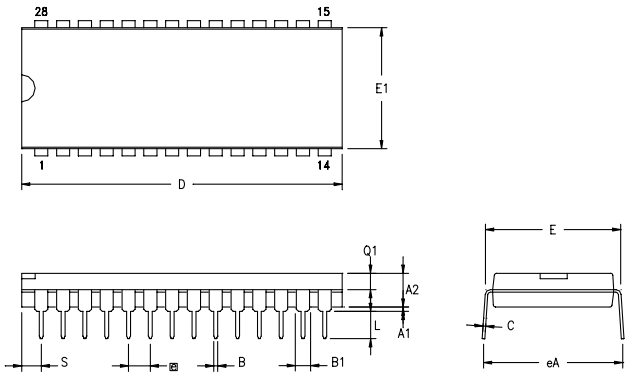


Figure 47. Port 3 Mode Register ($F7_h$: Write Only)

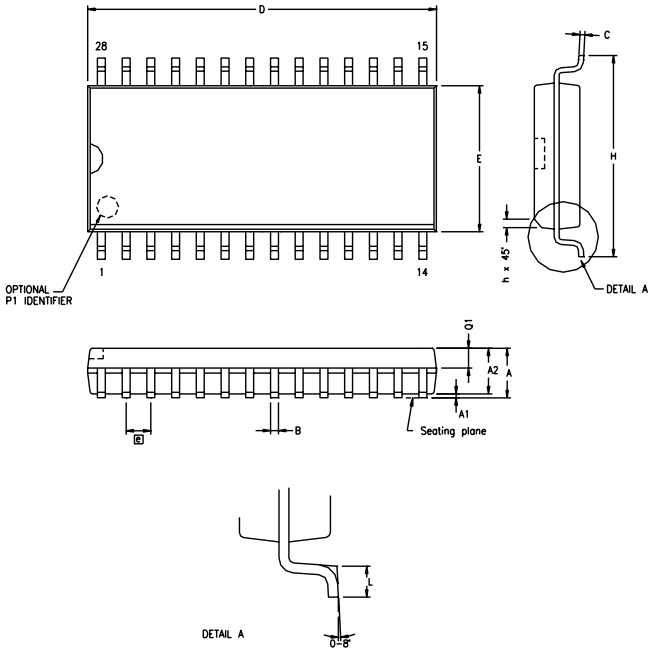


SYMBOL	OPT #	MILLIMETER		INCH	
		MIN	MAX	MIN	MAX
A1		0.38	1.02	.015	.040
A2		3.18	4.19	.125	.165
B		0.38	0.53	.015	.021
B1	01	1.40	1.65	.055	.065
	02	1.14	1.40	.045	.055
C		0.23	0.38	.009	.015
D	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
e		2.54 TYP		.100 TYP	
eA		15.49	16.76	.610	.660
L		3.05	3.81	.120	.150
Q1	01	1.40	1.91	.055	.075
	02	1.40	1.78	.055	.070
S	01	1.52	2.29	.060	.090
	02	1.02	1.52	.040	.060

CONTROLLING DIMENSIONS : INCH

OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

Figure 58. 28-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.64	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	17.78	18.00	.700	.710
E	7.40	7.60	.291	.299
e	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.71	.012	.028
L	0.61	1.00	.024	.039
Q1	0.97	1.09	.038	.043

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 59. 28-Pin SOIC Package Diagram