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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | Z8 |
| Core Size | 8-Bit |
| Speed | 16MHz |
| Connectivity | EBI/EMI |
| Peripherals | POR, WDT |
| Number of I/O | 24 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 237 x 8 |
| Voltage - Supply (Vcc/Vdd) | 3.5V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | External |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-SOIC (0.295", 7.50mm Width) |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z86e3416ssc |

- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive

## Functional Block Diagram

Figure 1 displays the functional block diagram.

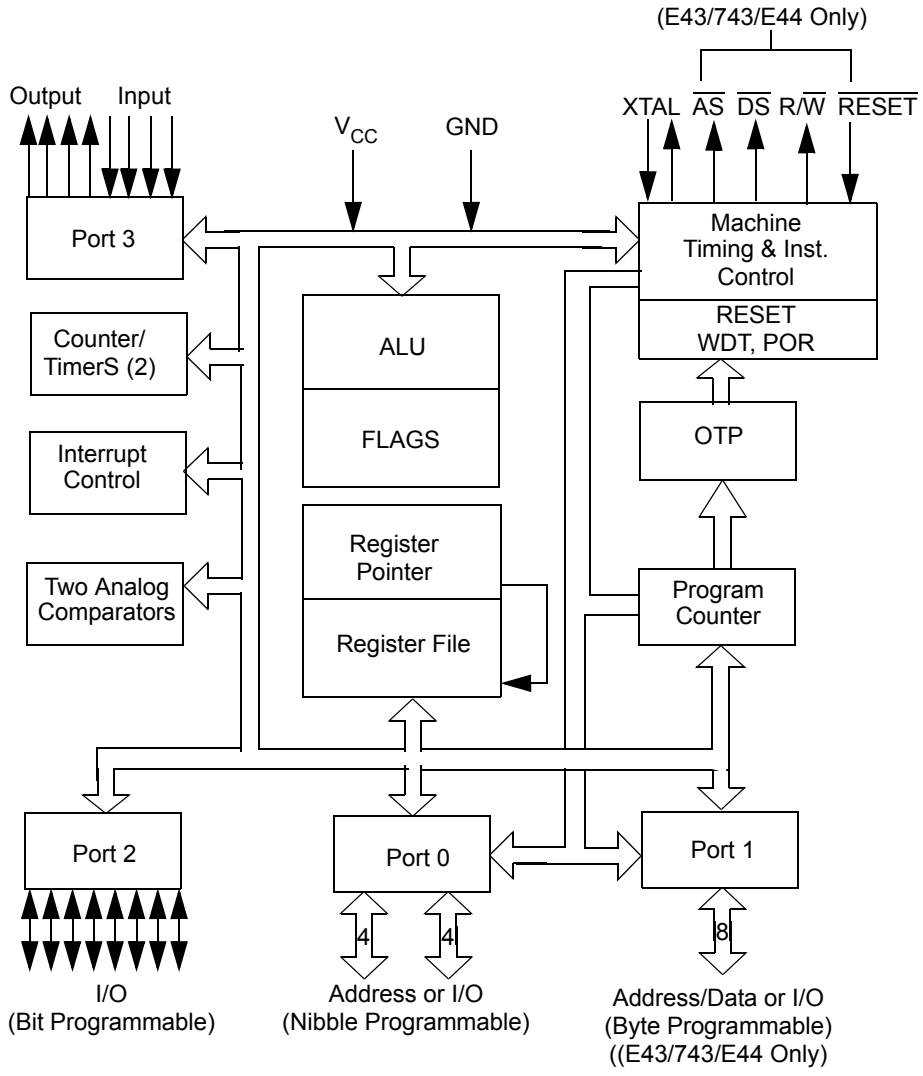


**Figure 1. Functional Block Diagram**

# Pin Description

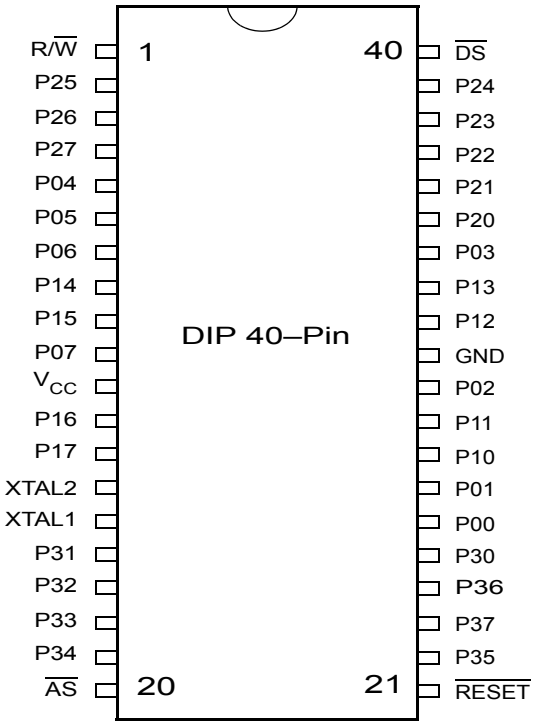


**Figure 3. 40-Pin DIP Pin Configuration Standard Mode**

**Table 2. 40-Pin DIP Pin Identification Standard Mode**

| Pin No | Symbol | Function | Direction |
|---|---|---|---|
| 1 | R/$\overline{W}$ | Read/Write | Output |
| 2-4 | P25-P27 | Port 2, Pins 5,6,7 | Input/Output |
| 5-7 | P04-P06 | Port 0, Pins 4,5,6 | Input/Output |
| 8-9 | P14-P15 | Port 1, Pins 4,5 | Input/Output |
| 10 | P07 | Port 0, Pin 7 | Input/Output |
| 11 | $V_{CC}$ | Power Supply | |
| 12-13 | P16-P17 | Port 1, Pins 6,7 | Input/Output |
| 14 | XTAL2 | Crystal Oscillator | Output |

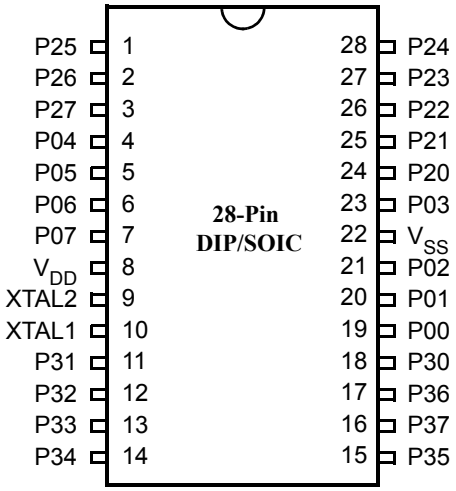


**Figure 9. Standard Mode 28-Pin DIP/SOIC Pin Configuration**

**Table 8. 28-Pin DIP/SOIC/PLCC Pin Identification Standard Mode**

| Pin No | Symbol | Function | Direction |
|---|---|---|---|
| 1-3 | P25-P27 | Port 2, Pins 5,6, | Input/Output |
| 4-7 | P04-P07 | Port 0, Pins 4,5,6,7 In/Output | |
| 8 | $V_{CC}$ | Power Supply | |
| 9 | XTAL2 | Crystal Oscillator | Output |
| 10 | XTAL1 | Crystal Oscillator | Input |
| 11-13 | P31-P33 | Port 3, Pins 1,2,3 | Input |
| 14-15 | P34-P35 | Port 3, Pins 4,5 | Output |
| 16 | P37 | Port 3, Pin 7 | Output |
| 17 | P36 | Port 3, Pin 6 | Output |
| 18 | P30 | Port 3, Pin 0 | Input |
| 19-21 | P00-P02 | Port 0, Pins 0,1,2 | Input/Output |
| 22 | $V_{SS}$ | Ground | |
| 23 | P03 | Port 0, Pin 3 | Input/Output |
| 24-28 | P20-P24 | Port 2, Pins 0,1,2,3,4 | Input/Output |

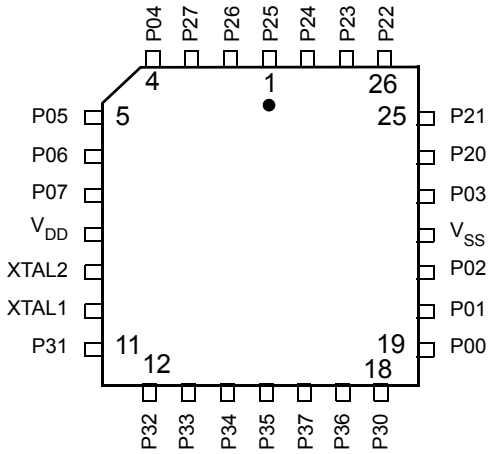


**Figure 10. Standard Mode 28-Pin PLCC Pin Configuration**

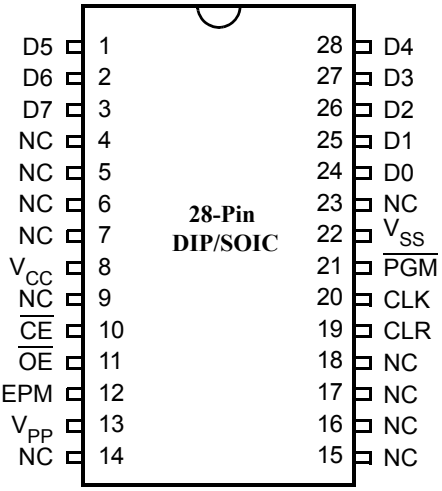


**Figure 11. EPROM Programming Mode 28-Pin DIP/SOIC Pin Configuration**

# Electrical Characteristics

## Absolute Maximum Ratings

**Table 10. Absolute Maximum Ratings**

| Parameter | Min | Max | Units | Notes |
|---|---|---|---|---|
| Ambient Temperature under Bias | –40 | +105 | C | |
| Storage Temperature | –65 | +150 | C | |
| Voltage on any Pin with Respect to $V_{SS}$ | –0.6 | +7 | V | 1 |
| Voltage on $V_{DD}$ Pin with Respect to $V_{SS}$ | –0.3 | +7 | V | |
| Voltage on XTAL1, P32, P33 and $\overline{\text{RESET}}$ Pins with Respect to $V_{SS}$ | –0.6 | $V_{DD}$+1 | V | 2 |
| Total Power Dissipation | | 1.21 | W | |
| Maximum Allowable Current out of $V_{SS}$ | | 220 | mA | |
| Maximum Allowable Current into $V_{DD}$ | | 180 | mA | |
| Maximum Allowable Current into an Input Pin | –600 | +600 | µA | 3 |
| Maximum Allowable Current into an Open-Drain Pin | –600 | +600 | µA | 4 |
| Maximum Allowable Output Current Sunk by Any I/O Pin | | 25 | mA | |
| Maximum Allowable Output Current Sourced by Any I/O Pin | | 25 | mA | |
| Maximum Allowable Output Current Sunk by $\overline{\text{RESET}}$ Pin | | 3 | mA | |

**Notes**
1. This applies to all pins except XTAL pins and where otherwise noted.
2. There is no input protection diode from pin to $V_{DD}$.
3. This excludes XTAL pins.
4. Device pin is not at an output Low state.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

**Table 11. DC Electrical Characteristics $T_A$ = 0 °C to +70 °C (Continued)**

| Symbol | Parameter | $V_{CC}$[1] | Min | Max | Typical @ 25°C | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| $T_{POR}$ | Power-On Reset | 3.5V | 2.0 ms | 24 | 7 | ms | | |
| | | 5.5V | 1.0 ms | 13 | 4 | ms | | |
| $V_{LV}$ | Auto Reset Voltage | | 2.3 | 3.0 | 2.8 | V | | 11,12 |

**Notes**
1. The $V_{CC}$ voltage specification of 5.5 V guarantees 5.0 V ± 0.5 V and the $V_{CC}$ voltage specification of 3.5 V guarantees only 3.5 V
2. STD Mode (not Low EMI Mode)
3. Z86E43/743/E44 only.
4. For analog comparator inputs when analog comparators are enabled
5. All outputs unloaded, I/O pins floating, inputs at rail.
6. CL1=CL2=22 pF.
7. Same as note 5 except inputs at $V_{CC}$
8. Clock must be forced Low, when XTAL1 is clock driven and XTAL2
9. WDT running
10. Auto Latch (mask option) selected.
11. Device does function down to the Auto Reset voltage
12. Max. temperature is 70 °C

**Table 12. DC Electrical Characteristics $T_A$= -40 °C to +105 °C**

| Symbol | Parameter | $V_{CC}$[1] | Min | Max | Typical @ 25°C | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| $V_{CH}$ | Clock Input High Voltage | 4.5V | 0.7 $V_{CC}$ | $V_{CC}$ +0.3 | 2.5 | V | Driven by External Clock Generator | |
| | | 5.5V | 0.7 $V_{CC}$ | $V_{CC}$ +0.3 | 2.5 | V | | |
| $V_{CL}$ | Clock Input Low Voltage | 4.5V | GND -0.3 | 0.2 $V_{CC}$ | 1.5 | V | Driven by External Clock Generator | |
| | | 5.5V | GND -0.3 | 0.2 $V_{CC}$ | 1.5 | V | | |
| $V_{IH}$ | Input High Voltage | 4.5V | 0.7 $V_{CC}$ | $V_{CC}$ +0.3 | 2.5 | V | | |
| | | 5.5V | 0.7 $V_{CC}$ | $V_{CC}$ +0.3 | 2.5 | V | | |
| $V_{IL}$ | Input Low Voltage | 4.5V | GND -0.3 | 0.2 $V_{CC}$ | 1.5 | V | | |
| | | 5.5V | GND -0.3 | 0.2 $V_{CC}$ | 1.5 | V | | |
| $V_{OH}$ | Output High Voltage Low EMI Mode | 4.5V | $V_{CC}$ -0.4 | | 4.8 | | $I_{OH}$ = -0.5 mA | 2 |
| | | 5.5V | $V_{CC}$ -0.4 | | 4.8 | | $I_{OH}$ = -0.5 mA | 2 |

**Table 13. DC Electrical Characteristics $T_A$ = 0 °C to +70 °C, 12 MHz (Continued)**

| No. | Symbol | Parameter | $V_{CC}$ [1] | Min | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| 4 | TwAS | $\overline{AS}$ Low Width | 3.5V | 55 | | ns | 2 |
| | | | 5.5V | 55 | | ns | 2 |
| 5 | TdAS(DS) | Address Float to $\overline{DS}$ Fall | 3.5V | 0 | | ns | |
| | | | 5.5V | 0 | | ns | |
| 6 | TwDSR | $\overline{DS}$ (Read) Low Width | 3.5V | 200 | | ns | 2,3 |
| | | | 5.5V | 200 | | ns | 2,3 |
| 7 | TwDSW | $\overline{DS}$ (Write) Low Width | 3.5V | 110 | | ns | 2,3 |
| | | | 5.5V | 110 | | ns | 2,3 |
| 8 | TdDSR(DR) | $\overline{DS}$ Fail to Read Data Req'd Valid | 3.5V | | 150 | ns | 2,3 |
| | | | 5.5V | | 150 | ns | 2,3 |
| 9 | ThDR(DS) | Read Data to $\overline{DS}$ Rise Hold Time | 3.5V | 0 | | ns | 2 |
| | | | 5.5V | 0 | | ns | 2 |
| 10 | TdDS(A) | $\overline{DS}$ Rise to Address Active Delay | 3.5V | 45 | | ns | 2 |
| | | | 5.5V | 55 | | ns | 2 |
| 11 | TdDS(AS) | $\overline{DS}$ Rise to $\overline{AS}$ Fall Delay | 3.5V | 30 | | ns | 2 |
| | | | 5.5V | 45 | | ns | 2 |
| 12 | TdR/W(AS) | R/$\overline{W}$ Valid to $\overline{AS}$ Rise Delay | 3.5V | 45 | | ns | 2 |
| | | | 5.5V | 45 | | ns | 2 |
| 13 | TdDS(R/W) | $\overline{DS}$ Rise to R/$\overline{W}$ Not Valid | 3.5V | 45 | | ns | 2 |
| | | | 5.5V | 45 | | ns | 2 |
| 14 | TdDW(DSW) | Write Data Valid to $\overline{DS}$ Fall (Write) Delay | 3.5V | 55 | | ns | 2 |
| | | | 5.5V | 55 | | ns | 2 |
| 15 | TdDS(DW) | $\overline{DS}$ Rise to Write Data Not Valid Delay | 3.5V | 45 | | ns | 2 |
| | | | 5.5V | 55 | | ns | 2 |
| 16 | TdA(DR) | Address Valid to Read Data Req'd Valid | 3.5V | | 310 | ns | 2,3 |
| | | | 5.5V | | 310 | ns | 2,3 |
| 17 | TdAS(DS) | $\overline{AS}$ Rise to $\overline{DS}$ Fall Delay | 3.5V | 65 | | ns | 2 |
| | | | 5.5V | 65 | | ns | 2 |

**Table 14. DC Electrical Characteristics $T_A$ = -40 °C to +105 °C, 12 MHz (Continued)**

| No. | Symbol | Parameter | $V_{CC}$[1] | Min | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| 10 | TdDS(A) | $\overline{DS}$ Rise to Address Active Delay | 4.5V | 45 | | ns | 2 |
| | | | 5.5V | 55 | | ns | 2 |
| 11 | TdDS(AS) | $\overline{DS}$ Rise to $\overline{AS}$ Fall Delay | 4.5V | 45 | | ns | 2 |
| | | | 5.5V | 45 | | ns | 2 |
| 12 | TdR/W(AS) | R/$\overline{W}$ Valid to $\overline{AS}$ Rise Delay | 4.5V | 45 | | ns | 2 |
| | | | 5.5V | 45 | | ns | 2 |
| 13 | TdDS(R/W) | $\overline{DS}$ Rise to R/$\overline{W}$ Not Valid | 4.5V | 45 | | ns | 2 |
| | | | 5.5V | 45 | | ns | 2 |
| 14 | TdDW(DSW) | Write Data Valid to $\overline{DS}$ Fall (Write) Delay | 4.5V | 55 | | ns | 2 |
| | | | 5.5V | 55 | | ns | 2 |
| 15 | TdDS(DW) | $\overline{DS}$ Rise to Write Data Not Valid Delay | 4.5V | 55 | | ns | 2 |
| | | | 5.5V | 55 | | ns | 2 |
| 16 | TdA(DR) | Address Valid to Read Data Req'd Valid | 4.5V | | 310 | ns | 2,3 |
| | | | 5.5V | | 310 | ns | 2,3 |
| 17 | TdAS(DS) | $\overline{AS}$ Rise to $\overline{DS}$ Fall Delay | 4.5V | 65 | | ns | 2 |
| | | | 5.5V | 65 | | ns | 2 |
| 18 | TdDM(AS) | $\overline{DM}$ Valid to $\overline{AS}$ Rise Delay | 4.5V | 35 | | ns | 2 |
| | | | 5.5V | 35 | | ns | 2 |
| 19 | ThDS(AS) | $\overline{DS}$ Valid to Address Valid Hold Time | 4.5V | 35 | | ns | 2 |
| | | | 5.5V | 35 | | ns | 2 |

**Notes**

1. The $V_{CC}$ voltage specification of 5.5 V guarantees 5.0 V ± 0.5 V and the $V_{CC}$ voltage specification of 3.5 V guarantees only 3.5 V.
2. Timing numbers given are for minimum TpC.
3. When using extended memory timing, add 2 TpC.

**Standard Test Load**

All timing references use 0.7 $V_{CC}$ for a logic 1 and 0.2 $V_{CC}$ for a logic 0.

For Standard Mode (not Low-EMI Mode for outputs) with SMR, D1 = 0, D0 = 0.

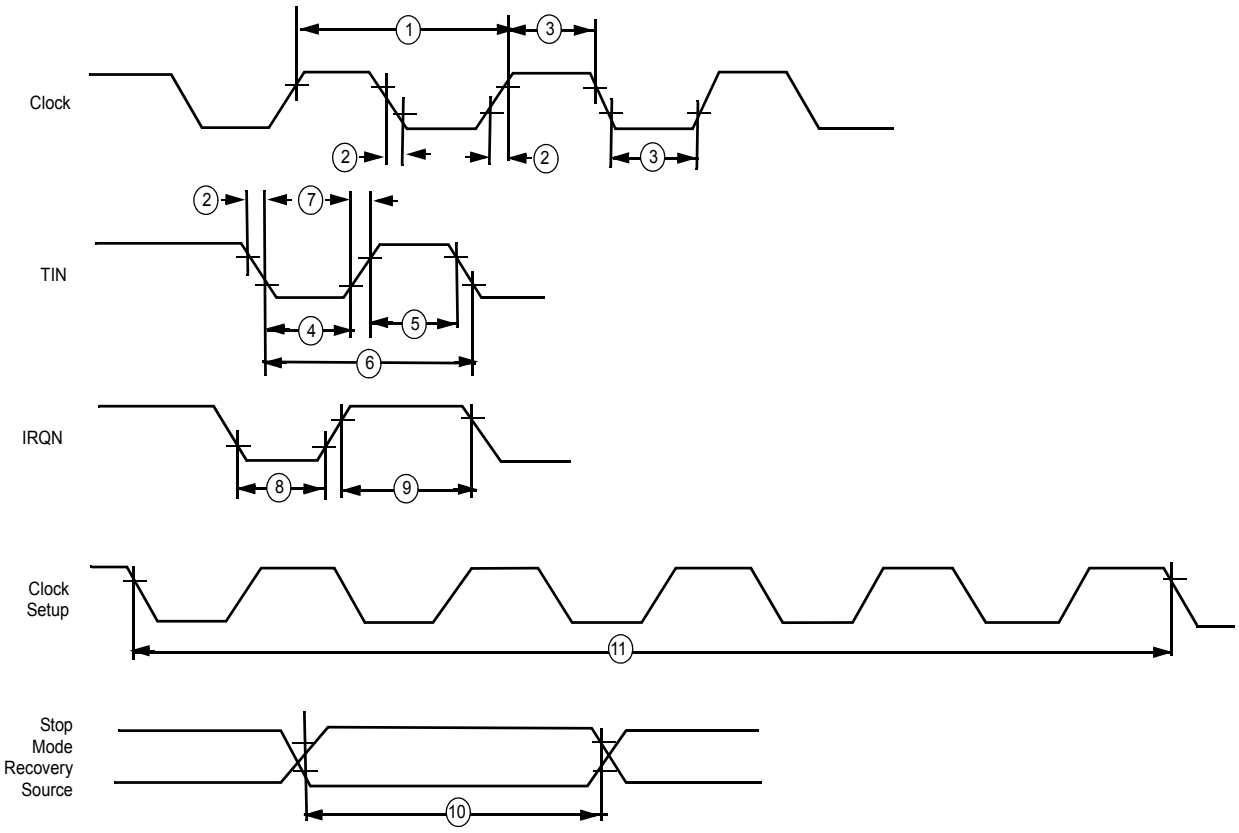


**Figure 15. Additional Timing Diagram**

**Table 15. Additional Timing Table (Divide-By-One Mode) $T_A$ = 0 °C to +70 °C**

| No | Symbol | Parameter | $V_{CC}$ [1] | Min | Max | Min | Max | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| 1 | TpC | Input Clock Period | 3.5V | 250 | DC | 166 | DC | ns | 2,3,4 |
| | | | 5.5V | 250 | DC | 166 | DC | ns | 2,3,4 |
| 2 | TrC,TfC | Clock Input Rise & Fall Times | 3.5V | | 25 | | 25 | ns | 2,3,4 |
| | | | 5.5V | | 25 | | 25 | ns | 2,3,4 |
| 3 | TwC | Input Clock Width | 3.5V | 100 | | 100 | | ns | 2,3,4 |
| | | | 5.5V | 100 | | 100 | | ns | 2,3,4 |
| 4 | TwTinL | Timer Input Low Width | 3.5V | 100 | | 100 | | ns | 2,3,4 |
| | | | 5.5V | 70 | | 70 | | ns | 2,3,4 |

**Table 16. Additional Timing Table (Divide-By-One Mode) $T_A$ = -40 °C to +105 °C (Continued)**

| No | Symbol | Parameter | $V_{CC}$ [1] | Min | Max | Min | Max | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| 2 | TrC,TfC | Clock Input Rise & Fall Times | 4.5V | | 25 | | 25 | ns | 2,3,4 |
| | | | 5.5V | | 25 | | 25 | ns | 2,3,4 |
| 3 | TwC | Input Clock Width | 4.5V | 100 | | 100 | | ns | 2,3,4 |
| | | | 5.5V | 100 | | 100 | | ns | 2,3,4 |
| 4 | TwTinL | Timer Input Low Width | 4.5V | 100 | | 100 | | ns | 2,3,4 |
| | | | 5.5V | 70 | | 70 | | ns | 2,3,4 |
| 5 | TwTinH | Timer Input High Width | 4.5V | 5TpC | | 5TpC | | | 2,3,4 |
| | | | 5.5V | 5TpC | | 5TpC | | | 2,3,4 |
| 6 | TpTin | Timer Input Period | 4.5V | 8TpC | | 8TpC | | | 2,3,4 |
| | | | 5.5V | 8TpC | | 8TpC | | | 2,3,4 |
| 7 | TrTin, TfTin | Timer Input Rise & Fall Timer | 4.5V | | 100 | | 100 | ns | 2,3,4 |
| | | | 5.5V | | 100 | | 100 | ns | 2,3,4 |
| 8A | TwIL | Int. Request Low Time | 4.5V | 100 | | 100 | | ns | 2,3,4,5 |
| | | | 5.5V | 70 | | 70 | | ns | 2,3,4,5 |
| 8B | TwIL | Int. Request Low Time | 4.5V | 5TpC | | 5TpC | | | 2,3,4,6 |
| | | | 5.5V | 5TpC | | 5TpC | | | 2,3,4,6 |
| 9 | TwIH | Int. Request Input High Time | 4.5V | 5TpC | | 5TpC | | | 2,3,4,5 |
| | | | 5.5V | 5TpC | | 5TpC | | | 2,3,4,5 |
| 10 | Twsm | Stop Mode Recovery Width Spec | 4.5V | 12 | | 12 | | ns | 4,7 |
| | | | 5.5V | 12 | | 12 | | ns | 4,7 |
| 11 | Tost | Oscillator Startup Time | 4.5V | | 5TpC | | 5TpC | | 4,7,8 |
| | | | 5.5V | | 5TpC | | 5TpC | | 4,7,8 |

**Notes**

1. The $V_{CC}$ voltage specification of 5.5 V guarantees 5.0 V ± 0.5 V and the $V_{CC}$ voltage specification of 3.5 V guarantees only 3.5 V.
2. Timing Reference uses 0.7 $V_{CC}$ for a logic 1 and 0.2 $V_{CC}$; for a logic 0.
3. SMR D1 = 0.
4. Maximum frequency for internal system clock is 4 MHz when using Low EMI OSC PCON Bit D7=0.
5. Interrupt request via Port 3 (P31-P33).
6. Interrupt request via Port 3 (P30).
7. SMR-D5 = 1, POR STOP Mode Delay is on.
8. For RC and LC oscillator, and for oscillator driven by clock driver.

**Table 18. Additional Timing Table (Divide by Two Mode) $T_A$ = -40 °C to +105 °C (Continued)**

| No | Symbol | Parameter | $V_{CC}$ [1] | Min | Max | Min | Max | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| 12 | Twdt | Watchdog Timer Delay Time Before Timeout | 3.5V | 7 | | 10 | | ms | D0 =0 | 8,9 |
| | | | 5.5V | 3.5 | | 5 | | ms | D1 = 0 | 5,11 |
| | | | 3.5V | 14 | | 20 | | ms | D0 =1 | 5,11 |
| | | | 5.5V | 7 | | 10 | | ms | D1 = 0 | 5,11 |
| | | | 3.5V | 28 | | 40 | | ms | D1 = 0 | 5,11 |
| | | | 5.5V | 14 | | 20 | | ms | D1 = 1 | 5,11 |
| | | | 3.5V | 112 | | 160 | | ms | D0 = 1 | 5,11 |
| | | | 5.5V | 56 | | 80 | | ms | D1 = 1 | 5,11 |

**Notes**
1. The $V_{CC}$ voltage specification of 5.5 V guarantees 5.0 V ± 0.5 V and the $V_{CC}$ voltage specification of 3.5 V guarantees only 3.5 V.
2. Timing Reference uses 0.7 VC0 for a logic 1 and 0.2 VGC for a logic 0.
3. SMR D1 = 0.
4. SMR-D5 = 1, POR STOP Mode Delay is on
5. Interrupt request via Port 3 (P31-P33)
6. Interrupt request via Port 3 (P30).
7. Maximum frequency for internal system clock is 2 MHz when using Low EMI OSC PCON Bit D7 = 0
8. Reg. WDTMR.
9. Using internal RC.

# Pin Functions

## EPROM Programming Mode

**D7-D0** Data Bus. The data can be read from or written to external memory through the data bus.

**$V_{CC}$** Power Supply. This pin must supply 5 V during the EPROM read mode and 6 V during other modes.

**$\overline{CE}$** Chip Enable (active Low). This pin is active during EPROM Read Mode, Program Mode, and Program Verify Mode.

**$\overline{OE}$** Output Enable (active Low). This pin drives the direction of the Data Bus. When this pin is Low, the Data Bus is output, when High, the Data Bus is input.

**EPM** EPROM Program Mode. This pin controls the different EPROM Program Mode by applying different voltages.

**$V_{PP}$** Program Voltage. This pin supplies the program voltage.

**PGM** Program Mode (active Low). When this pin is Low, the data is programmed to the EPROM through the Data Bus.

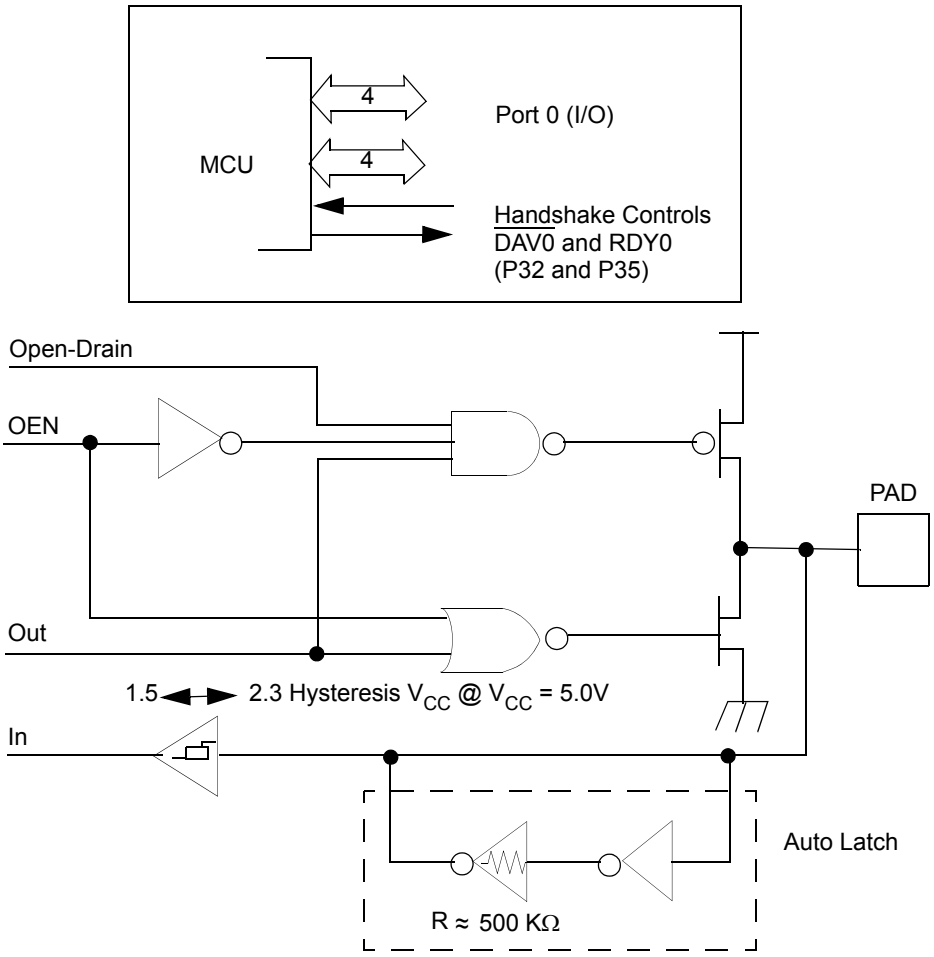


**Figure 18. Port 0 Configuration**

**Port 1 (P17-P10)**. Port 1 is an 8-bit, bidirectional, CMOS-compatible port with multiplexed Address (A7-A0) and Data (D7-D0) ports. These eight I/O lines can be programmed as inputs or outputs or can be configured under software control as an Address/Data port for interfacing external memory. The input buffers are Schmitt-triggered and the output buffers can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 1 can be placed under handshake control. In this configuration, Port 3, lines P33 and P34 are used as the handshake controls RDY1 and $\overline{\text{DAV1}}$ (Ready and Data Available). To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 outputs the additional lines (see Figure 19).

# Functional Description

The MCU incorporates the following special functions to enhance the standard Z8 architecture to provide the user with increased design flexibility.

**RESET**. The device is reset in one of three ways:

1. Power-On Reset
2. Watchdog Timer
3. Stop Mode Recovery Source

**Note:** *Having the Auto Power-On Reset circuitry built-in, the MCU does not need to be connected to an external power-on reset circuit. The reset time is $T_{POR}$. The MCU does not re-initialize WDTMR, SMR, P2M, and P3M registers to their reset values on a Stop Mode Recovery operation.*

**Note:** *The device $V_{CC}$ must rise up to the operating $V_{CC}$ specification before the $T_{POR}$ expires.*

**Program Memory**. The MCU can address up to 4/8/16 KB of Internal Program Memory (see Figure 22). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For EPROM mode, byte 12 (000Ch) to address 4095 (0FFFh)/8191 (1FFFh)/16384 (3FFFh), consists of programmable EPROM. After reset, the program counter points at the address 000Ch, which is the starting address of the user program.

In ROMless mode, the Z86E43/743/E44 can address up to 64 KB of External Program Memory. The ROM/ROMless option is only available on the 44-pin devices.

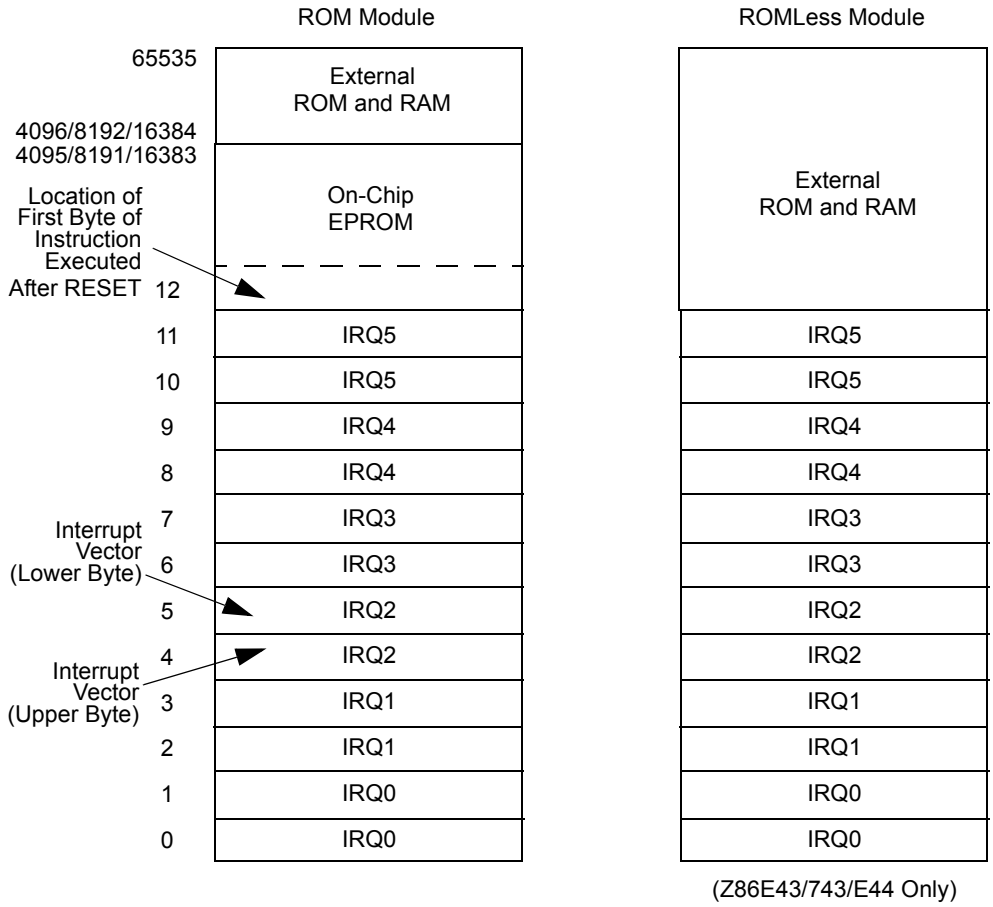


**Figure 22. Program Memory Map**

**EPROM Protect**. When in ROM Protect Mode, and executing out of External Program Memory, instructions LDC, LDCI, LDE, and LDEI cannot read Internal Program Memory.

When in EPROM Protect Mode and executing out of Internal Program Memory, instructions LDC, LDCI, LDE, and LDEI can read Internal Program Memory.

**Data Memory ($\overline{DM}$)**. In ROM Mode, the Z86E43/743/E44 can address up to 60156/48 KB of external data memory beginning at location 4096/8192/16384. In ROMless mode, the Z86E43/743/E44 can address up to 64 KB of data memory. External data memory may be included with, or separated from, the external program memory space. $\overline{DM}$, an optional I/0 function that can be programmed to appear on pin P34, is used to distinguish between data and program memory space (Figure 23). The state of the $\overline{DM}$ signal is controlled by the type of instruction being executed. An LDC opcode references PROGRAM ($\overline{DM}$ inactive) memory, and an LDE instruction references data ($\overline{DM}$ active Low) memory.

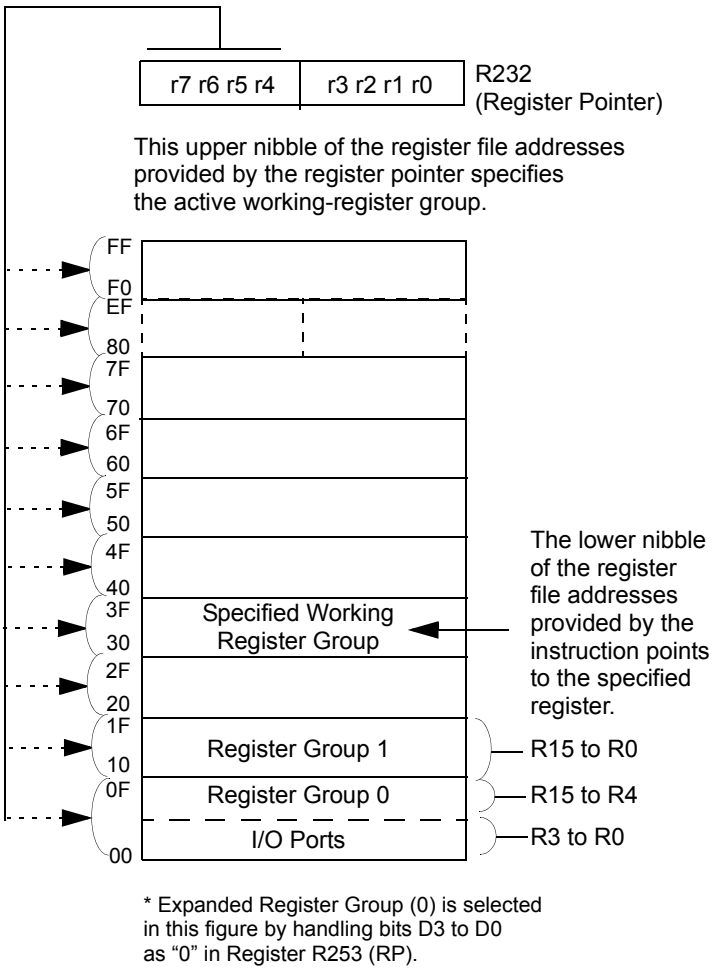


**Figure 25. Register Pointer**

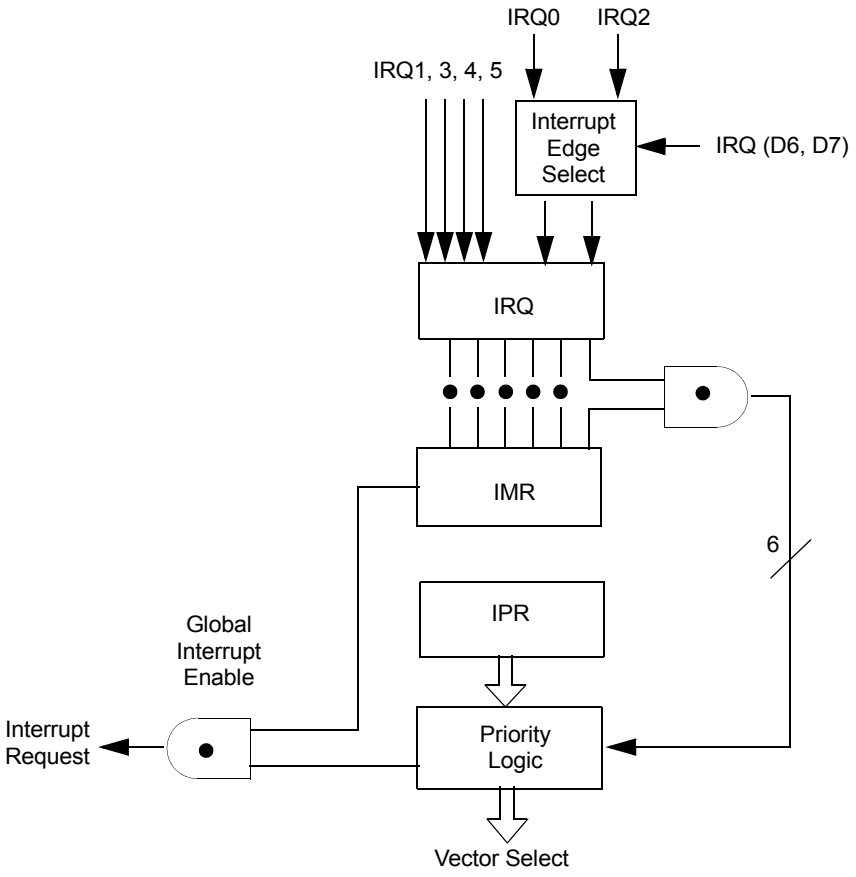


**Figure 28. Interrupt Block Diagram**

**Table 20. Interrupt Types, Sources, and Vectors**

| Name | Source | Vector Location | Comments |
|---|---|---|---|
| IRQ0 | $\overline{\text{DAV0}}$, IRQ0 | 0,1 | External (P32), Rising/Falling Edge Triggered |
| IRQ1 | IRQ1 | 2,3 | External (P33), Falling Edge Triggered |
| IRQ2 | $\overline{\text{DAV2}}$, IRQ2, $T_{IN}$ | 4,5 | External (P31), Rising/Falling Edge Triggered |
| IRQ3 | IRQ3 | 6,7 | External (P30), Falling Edge Triggered |
| 1RQ4 | T0 | 8,9 | Internal |
| IRQ5 | T1 | 10,11 | Internal |

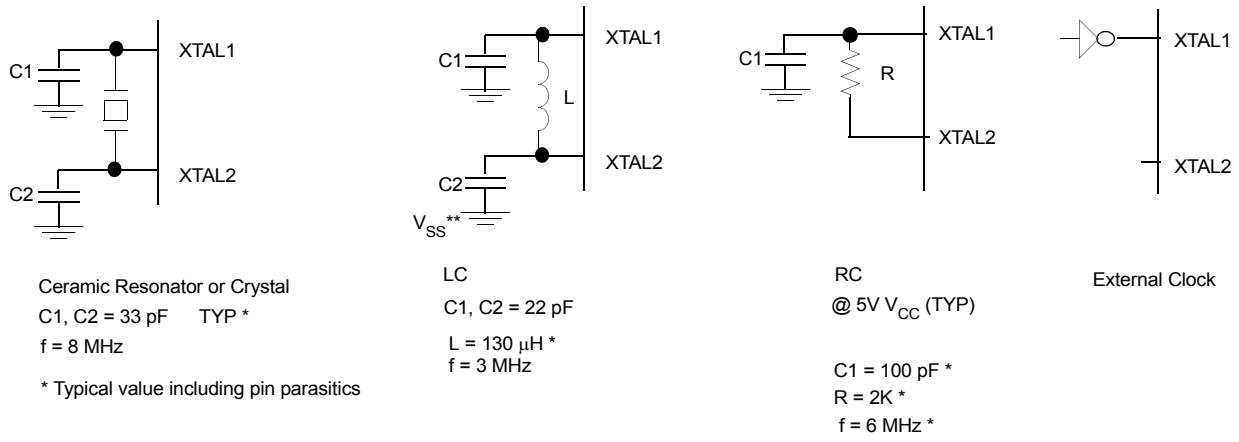


**Figure 29. Oscillator Configuration**

**Power-On Reset (POR)**. A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR timer allows $V_{CC}$ and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

1. Power fail to Power OK status
2. Stop Mode Recovery (if D5 of SMR=0)
3. WDT time-out

The POR time is a nominal 5 ms. Bit 5 of the STOP mode Register (SMR) determines whether the POR timer is by-passed after Stop Mode Recovery (typical for an external clock and RC/LC oscillators with fast start up times).

**HALT**. Turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupt IRQ0, IRQ1, and IRQ2 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT. In order to enter STOP or HALT Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, you must execute a NOP (Opcode = FFh) immediately before the appropriate sleep instruction, that is:

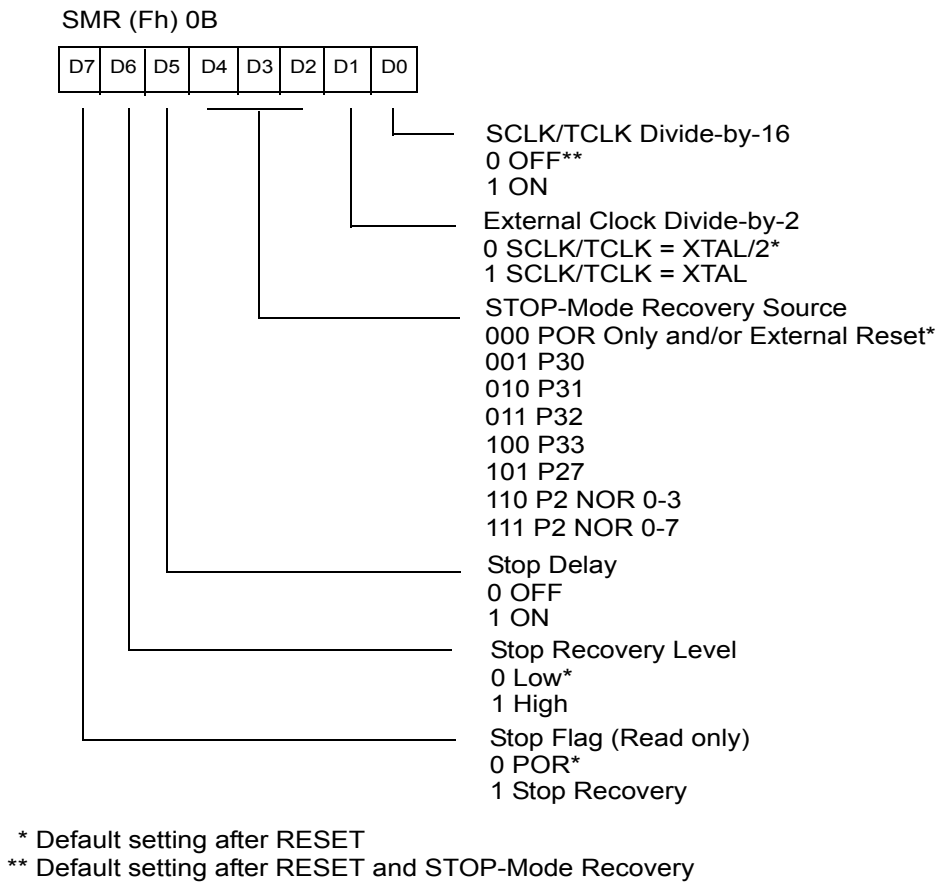


**Figure 31. Stop Mode Recovery Register (Write-Only Except Bit D7, Which Is Read-Only)**

**SCLK/TCLK Divide-by-16 Select (D0)**. This bit of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources counter/timers and interrupt logic).

**External Clock Divide-by-Two (D1)**. This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, the System Clock (SCLK) and Timer Clock (TCLK) are equal to the external clock frequency divided by two. The SCLK/TCLK is equal to the external clock frequency when this bit is set (D1=1). Using this bit together with D7 of PCON further helps lower EMI (that is, D7 (PCON) = 0, D1 (SMR) = 1). The default setting is zero.

**Stop Mode Recovery Source (D2, D3, and D4)**. These three bits of the SMR register specify the wake up source of the Stop Mode Recovery (Figure 32). Table 22 shows the SMR source selected with the setting of D2 to D4. P33-P31 cannot be used to wake up

**Note:** *WDT time-out in STOP Mode will not reset SMR,SMR2,PCON, WDTMR, P2M, P3M, Ports 2 & 3 Data Registers, but will activate the $T_{POR}$ delay.*

**WDTMR Register Accessibility**. The WDTMR register is accessible only during the first 60 internal system clock cycles from the execution of the first instruction after Power-On Reset, Watchdog reset or a Stop Mode Recovery (Figure 33 and Figure 34). After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register File at address location 0Fh.

**Clock Free WDT Reset**. The WDT will enable the Z8 to reset the I/0 pins whenever the WDT times out, even without a clock source running on the XTAL1 and XTAL2 pins. WDTMR Bit D4 must be 0 for the clock Free WDT to work. The I/O pins will default to their default settings.

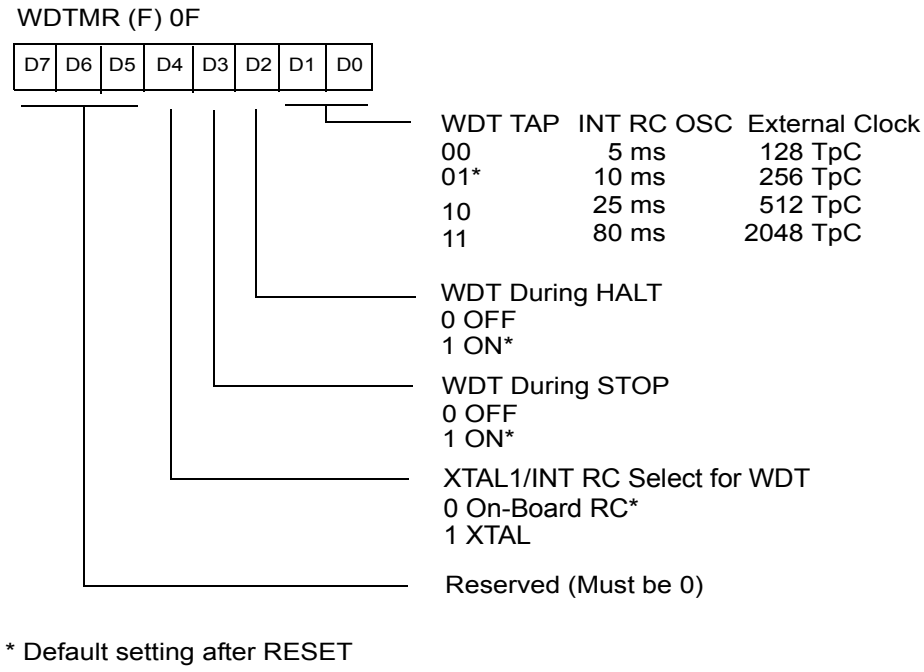


**Figure 33. Watchdog Timer Mode Register Write Only**

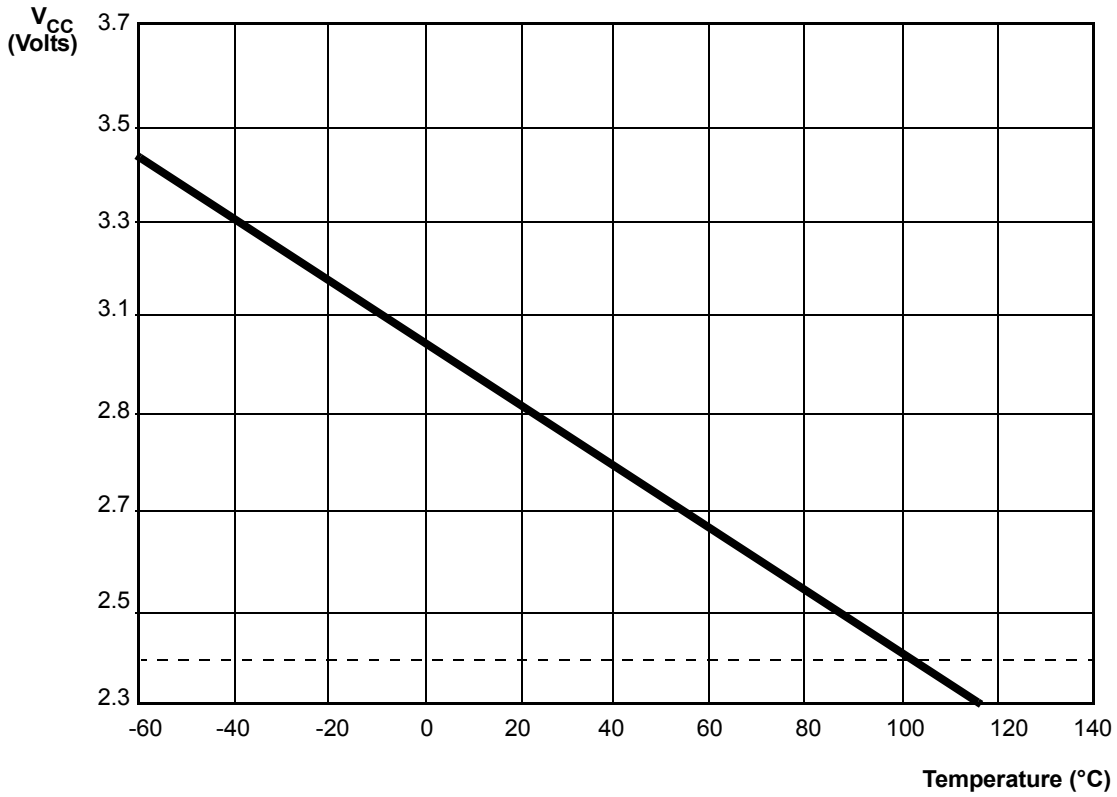


**Figure 35. Typical $V_{LV}$ Voltage vs. Temperature**