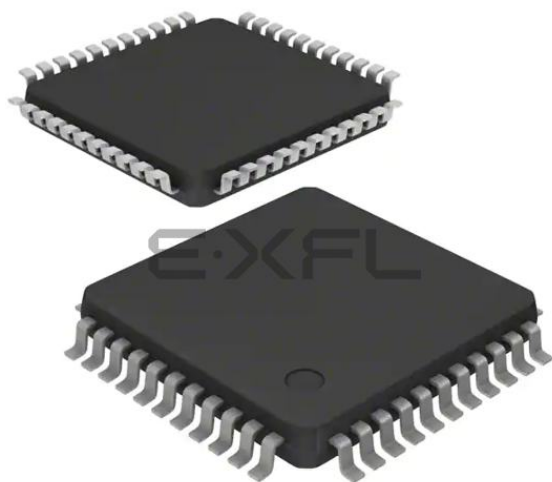




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Details

Product Status	Active
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	EBI/EMI
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e4312asg

Pin Description

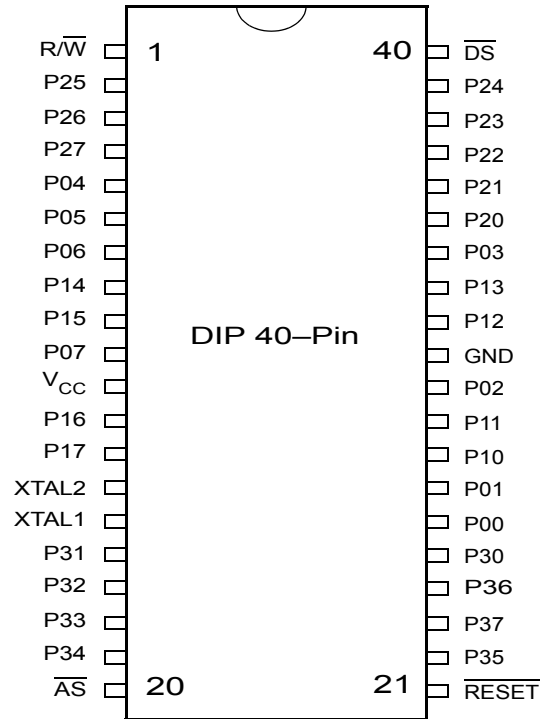


Figure 3. 40-Pin DIP Pin Configuration Standard Mode

Table 2. 40-Pin DIP Pin Identification Standard Mode

Pin No	Symbol	Function	Direction
1	R/W	Read/Write	Output
2-4	P25-P27	Port 2, Pins 5,6,7	Input/Output
5-7	P04-P06	Port 0, Pins 4,5,6	Input/Output
8-9	P14-P15	Port 1, Pins 4,5	Input/Output
10	P07	Port 0, Pin 7	Input/Output
11	V _{CC}	Power Supply	
12-13	P16-P17	Port 1, Pins 6,7	Input/Output
14	XTAL2	Crystal Oscillator	Output

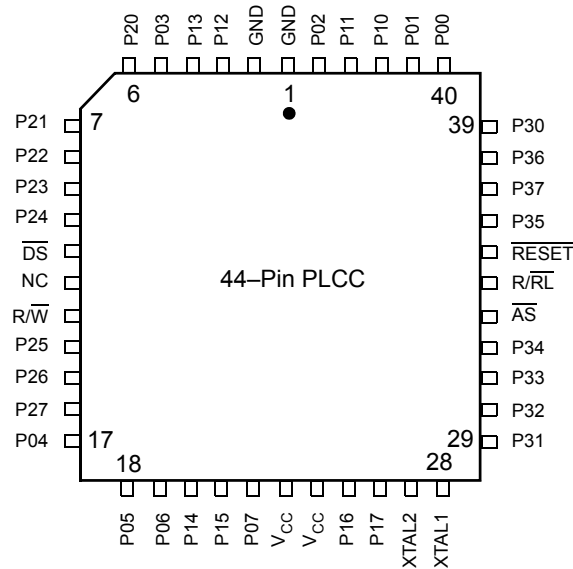


Figure 4. 44-Pin PLCC Pin Configuration Standard Mode

Table 3. 44-Pin PLCC Pin Identification

Pin No	Symbol	Function	Direction
1-2	GND	Ground	
3-4	P12-P13	Port 1, Pins 2,3	Input/Output
5	P03	Port 0, Pin 3	Input/Output
6-10	P20-P24	Port 2, Pins 0,1,2,3,4	Input/Output
11	DS	Data Strobe	Output
12	NC	No Connection	
13	R/W	Read/Write	Output
14-16	P25-P27	Port 2, Pins 5,6,7	Input/Output
17-19	P04-P06	Port 0, Pins 4,5,6	Input/Output
20-21	P14-P15	Port 1, Pins 4,5	Input/Output
22	P07	Port 0, Pin 7	Input/Output
23-24	V _{CC}	Power Supply	
25-26	P16-P17	Port 1, Pins 6,7	Input/Output

**Table 6. 44-Pin PLCC Pin Configuration EPROM Programming Mode
(Continued)**

Pin No	Symbol	Function	Direction
32-39	NC	No Connection	
40	CLR	Clear	Input
41	CLK	Clock	Input
42-43	NC	No Connection	
44	/PGM	Prog. Mode	Input

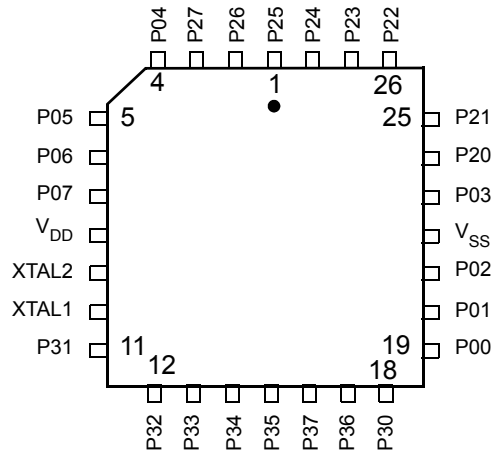


Figure 10. Standard Mode 28-Pin PLCC Pin Configuration

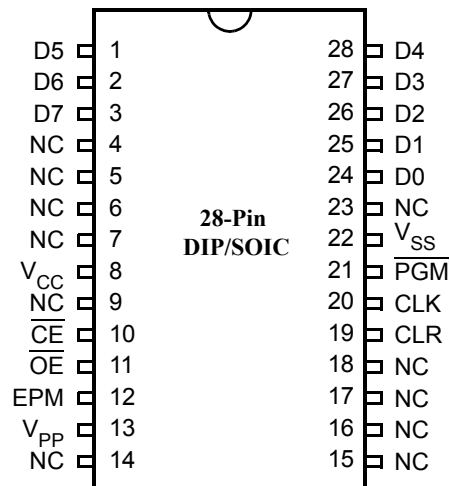


Figure 11. EPROM Programming Mode 28-Pin DIP/SOIC Pin Configuration

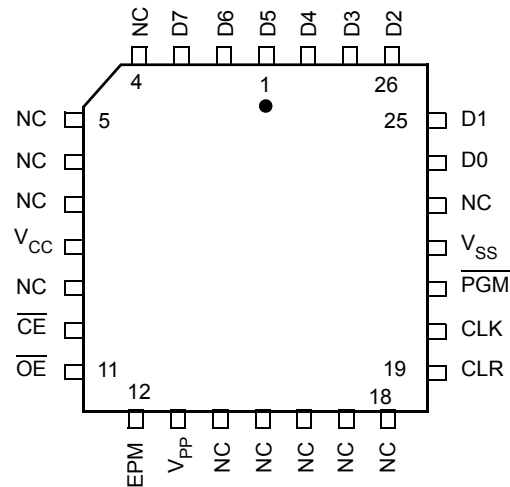


Figure 12. EPROM Programming Mode 28-Pin PLCC Pin Configuration

Table 9. 28-Pin EPROM Pin Identification EPROM Mode

Pin #	Symbol	Function	Direction
1-3	D5-D7	Data 5,6,7	Input/Output
4-7	NC	No Connection	
8	V _{CC}	Power Supply	
9	NC	No connection	
10	CE	Chip Select	Input
11	OE	Output Enable	Input
12	EPM	EPROM Prog. Mode	Input
13	V _{PP}	Prog. Voltage	Input
14-18	NC	No Connection	
19	CLR	Clear	
20	CLK	Clock	
21	/PGM	Prog. Mode	Input
22	V _{SS}	Ground	
23	NC	No Connection	
24-28	D0-D4	Data 0,1,2,3,4	Input/Output

Table 11. DC Electrical Characteristics $T_A = 0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$ (Continued)

Symbol	Parameter	V_{CC}^1	Min	Max	Typical @ 25 $^{\circ}\text{C}$	Units	Conditions	Notes
T_{POR}	Power-On Reset	3.5V	2.0 ms	24	7	ms		
		5.5V	1.0 ms	13	4	ms		
V_{LV}	Auto Reset Voltage		2.3	3.0	2.8	V		11,12

Notes

1. The V_{CC} voltage specification of 5.5 V guarantees $5.0\text{ V} \pm 0.5\text{ V}$ and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V
2. STD Mode (not Low EMI Mode)
3. Z86E43/743/E44 only.
4. For analog comparator inputs when analog comparators are enabled
5. All outputs unloaded, I/O pins floating, inputs at rail.
6. $CL1=CL2=22\text{ pF}$.
7. Same as note 5 except inputs at V_{CC}
8. Clock must be forced Low, when XTAL1 is clock driven and XTAL2
9. WDT running
10. Auto Latch (mask option) selected.
11. Device does function down to the Auto Reset voltage
12. Max. temperature is $70\text{ }^{\circ}\text{C}$

Table 12. DC Electrical Characteristics $T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$

Symbol	Parameter	V_{CC}^1	Min	Max	Typical @ 25 $^{\circ}\text{C}$	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	4.5V	$0.7 V_{CC}$	$V_{CC} + 0.3$	2.5	V	Driven by External Clock Generator	
		5.5V	$0.7 V_{CC}$	$V_{CC} + 0.3$	2.5	V		
V_{CL}	Clock Input Low Voltage	4.5V	GND -0.3	$0.2 V_{CC}$	1.5	V	Driven by External Clock Generator	
		5.5V	GND -0.3	$0.2 V_{CC}$	1.5	V		
V_{IH}	Input High Voltage	4.5V	$0.7 V_{CC}$	$V_{CC} + 0.3$	2.5	V		
		5.5V	$0.7 V_{CC}$	$V_{CC} + 0.3$	2.5	V		
V_{IL}	Input Low Voltage	4.5V	GND -0.3	$0.2 V_{CC}$	1.5	V		
		5.5V	GND -0.3	$0.2 V_{CC}$	1.5	V		
V_{OH}	Output High Voltage Low EMI Mode	4.5V	$V_{CC} - 0.4$		4.8		$I_{OH} = -0.5\text{ mA}$	2
		5.5V	$V_{CC} - 0.4$		4.8		$I_{OH} = -0.5\text{ mA}$	2

Table 12. DC Electrical Characteristics $T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$ (Continued)

Symbo l	Parameter	V_{CC}^1	Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC2}	Standby Current STOP Mode	4.5V		10	2	μA	$V_{IN} = 0\text{V}$, V_{CC}	7,8,9
		5.5V		10	3	μA	$V_{IN} = 0\text{V}$, V_{CC}	7,8,9
		4.5V		40	10	μA	$V_{IN} = 0\text{V}$, V_{CC}	7,8
		5.5V		40	10	μA	$V_{IN} = 0\text{V}$, V_{CC}	7,8
I_{ALL}	Auto Latch Low Current	4.5V	1.4	20	4.7	μA	$0\text{V} < V_{IN} < V_{CC}$	10
		5.5V	1.4	20	4.7	μA	$0\text{V} < V_{IN} < V_{CC}$	10
I_{ALH}	Auto Latch High Current	4.5V	-1.0	-10	-3.8	μA	$0\text{V} < V_{IN} < V_{CC}$	10
		5.5V	-1.0	-10	-3.8	μA	$0\text{V} < V_{IN} < V_{CC}$	10
T_{POR}	Power-On Reset	4.5V	1.0	14	4	ms		
		5.5V	1.0	14	4	ms		
V_{LV}	Auto Reset Voltage		2.0	3.3	2.8	V		11

Notes

1. The V_{CC} voltage specification of 5.5 V guarantees $5.0\text{ V} \pm 0.5\text{ V}$ and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V.
2. STD Mode (not Low EMI Mode).
3. Z86E43/743/E44 only.
4. For analog comparator inputs when analog comparators are enabled.
5. All outputs unloaded, I/O pins floating, inputs at rail.
6. $CL1=CL2=22\text{ pF}$.
7. Same as note 5 except inputs at V_{CC} .
8. Clock must be forced Low, when XTAL1 is clock driven and XTAL2.
9. WDT is not running.
10. Auto Latch (mask option) selected.
11. Device does function down to the Auto Reset voltage.

Table 13. DC Electrical Characteristics $T_A = 0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$, 12 MHz (Continued)

No.	Symbol	Parameter	V_{CC}^1	Min	Max	Units	Notes
4	TwAS	$\overline{AS}$ Low Width	3.5V	55		ns	2
			5.5V	55		ns	2
5	TdAS(DS)	Address Float to $\overline{DS}$ Fall	3.5V	0		ns	
			5.5V	0		ns	
6	TwDSR	$\overline{DS}$ (Read) Low Width	3.5V	200		ns	2,3
			5.5V	200		ns	2,3
7	TwDSW	$\overline{DS}$ (Write) Low Width	3.5V	110		ns	2,3
			5.5V	110		ns	2,3
8	TdDSR(DR)	$\overline{DS}$ Fail to Read Data Req'd Valid	3.5V		150	ns	2,3
			5.5V		150	ns	2,3
9	ThDR(DS)	Read Data to $\overline{DS}$ Rise Hold Time	3.5V	0		ns	2
			5.5V	0		ns	2
10	TdDS(A)	$\overline{DS}$ Rise to Address Active Delay	3.5V	45		ns	2
			5.5V	55		ns	2
11	TdDS(AS)	$\overline{DS}$ Rise to $\overline{AS}$ Fall Delay	3.5V	30		ns	2
			5.5V	45		ns	2
12	TdR/W(AS)	$R/\overline{W}$ Valid to $\overline{AS}$ Rise Delay	3.5V	45		ns	2
			5.5V	45		ns	2
13	TdDS(R/W)	$\overline{DS}$ Rise to $R/\overline{W}$ Not Valid	3.5V	45		ns	2
			5.5V	45		ns	2
14	TdDW(DSW)	Write Data Valid to $\overline{DS}$ Fall (Write) Delay	3.5V	55		ns	2
			5.5V	55		ns	2
15	TdDS(DW)	$\overline{DS}$ Rise to Write Data Not Valid Delay	3.5V	45		ns	2
			5.5V	55		ns	2
16	TdA(DR)	Address Valid to Read Data Req'd Valid	3.5V		310	ns	2,3
			5.5V		310	ns	2,3
17	TdAS(DS)	$\overline{AS}$ Rise to $\overline{DS}$ Fall Delay	3.5V	65		ns	2
			5.5V	65		ns	2

Table 15. Additional Timing Table (Divide-By-One Mode) $T_A = 0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$ (Continued)

No	Symbol	Parameter	V_{CC}^1	Min	Max	Min	Max	Units	Notes
5	TwTinH	Timer Input High Width	3.5V	5TpC		5TpC			2,3,4
			5.5V	5TpC		5TpC			2,3,4
6	TpTin	Timer Input Period	3.5V	8TpC		8TpC			2,3,4
			5.5V	8TpC		8TpC			2,3,4
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.5V		100		100	ns	2,3,4
			5.5V		100		100	ns	2,3,4
8A	TwIL	Int. Request Low Time	3.5V	100		100		ns	2,3,4,5
			5.5V	70		70		ns	2,3,4,5
8B	TwIL	Int. Request Low Time	3.5V	5TpC		5TpC			2,3,4,6
			5.5V	5TpC		5TpC			2,3,4,6
9	TwIH	Int. Request Input High Time	3.5V	5TpC		5TpC			2,3,4,5
			5.5V	5TpC		5TpC			2,3,4,5
10	Twsm	Stop Mode Recovery Width Spec	3.5V	12		12		ns	4,7
			5.5V	12		12		ns	4,7
11	Tost	Oscillator Startup Time	3.5V		5TpC		5TpC		4,7,8
			5.5V		5TpC		5TpC		4,7,8

Notes

1. The V_{CC} voltage specification of 5.5 V guarantees $5.0\text{ V} \pm 0.5\text{ V}$ and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V.
2. Timing Reference uses $0.7 V_{CC}$ for a logic 1 and $0.2 V_{CC}$ for a logic 0.
3. SMR D1 = 0.
4. Maximum frequency for internal system clock is 4 MHz when using Low EMI OSC PCON Bit D7 = 0.
5. Interrupt request via Port 3 (P31-P33).
6. Interrupt request via Port 3 (P30).
7. SMR-D5 = 1, POR STOP Mode Delay is on.
8. For RC and LC oscillator, and for oscillator driven by clock driver.

Table 16. Additional Timing Table (Divide-By-One Mode) $T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$

No	Symbol	Parameter	V_{CC}^1	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	4.5V	250	DC	166	DC	ns	2,3,4
			5.5V	250	DC	166	DC	ns	2,3,4

Table 16. Additional Timing Table (Divide-By-One Mode) $T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$ (Continued)

No	Symbol	Parameter	V_{CC} ¹	Min	Max	Min	Max	Units	Notes
2	TrC,TfC	Clock Input Rise & Fall Times	4.5V		25		25	ns	2,3,4
			5.5V		25		25	ns	2,3,4
3	TwC	Input Clock Width	4.5V	100		100		ns	2,3,4
			5.5V	100		100		ns	2,3,4
4	TwTinL	Timer Input Low Width	4.5V	100		100		ns	2,3,4
			5.5V	70		70		ns	2,3,4
5	TwTinH	Timer Input High Width	4.5V	5TpC		5TpC			2,3,4
			5.5V	5TpC		5TpC			2,3,4
6	TpTin	Timer Input Period	4.5V	8TpC		8TpC			2,3,4
			5.5V	8TpC		8TpC			2,3,4
7	TrTin, TfTin	Timer Input Rise & Fall Timer	4.5V		100		100	ns	2,3,4
			5.5V		100		100	ns	2,3,4
8A	TwIL	Int. Request Low Time	4.5V	100		100		ns	2,3,4,5
			5.5V	70		70		ns	2,3,4,5
8B	TwIL	Int. Request Low Time	4.5V	5TpC		5TpC			2,3,4,6
			5.5V	5TpC		5TpC			2,3,4,6
9	TwIH	Int. Request Input High Time	4.5V	5TpC		5TpC			2,3,4,5
			5.5V	5TpC		5TpC			2,3,4,5
10	Twsm	Stop Mode Recovery Width Spec	4.5V	12		12		ns	4,7
			5.5V	12		12		ns	4,7
11	Tost	Oscillator Startup Time	4.5V		5TpC		5TpC		4,7,8
			5.5V		5TpC		5TpC		4,7,8

Notes

1. The V_{CC} voltage specification of 5.5 V guarantees $5.0\text{ V} \pm 0.5\text{ V}$ and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V.
2. Timing Reference uses $0.7 V_{CC}$ for a logic 1 and $0.2 V_{CC}$ for a logic 0.
3. SMR D1 = 0.
4. Maximum frequency for internal system clock is 4 MHz when using Low EMI OSC PCON Bit D7=0.
5. Interrupt request via Port 3 (P31-P33).
6. Interrupt request via Port 3 (P30).
7. SMR-D5 = 1, POR STOP Mode Delay is on.
8. For RC and LC oscillator, and for oscillator driven by clock driver.

Table 18. Additional Timing Table (Divide by Two Mode) $T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$

No	Symbol	Parameter	V_{CC}^1	Min	Max	Min	Max	Units	Conditions	Notes
1	TpC	Input Clock Period	3.5V	62.5	DC	250	DC	ns		2,6,4
			5.5V	62.5	DC	250	DC	ns		2,6,4
2	TrC,TfC	Clock Input Rise & Fall Times	3.5V		15		25	ns		2,6,4
			5.5V		15		25	ns		2,6,4
3	TwC	Input Clock Width	3.5V	31		31		ns		2,6,4
			5.5V	31		31		ns		2,6,4
4	TwTinL	Timer Input Low Width	3.5V	70		70		ns		2,6,4
			5.5V	70		70		ns		2,6,4
5	TwTinH	Timer Input High Width	3.5V	5TpC		5TpC				2,6,4
			5.5V	5TpC		5TpC				2,6,4
6	TpTin	Timer Input Period	3.5V	8TpC		8TpC				2,6,4
			5.5V	8TpC		8TpC				2,6,4
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.5V		100		100	ns		2,6,4
			5.5V		100		100	ns		2,6,4
8A	TwIL	Int. Request Low Time	3.5V	70		70		ns		2,6,4,5
			5.5V	70		70		ns		2,6,4,5
8B	TwIL	Int. Request Low Time	3.5V	5TpC		5TpC				2,6,4,5
			5.5V	5TpC		5TpC				2,6,4,5
9	TwIH	Int. Request Input High Time	3.5V	5TpC		5TpC				2,6,4,5
			5.5V	5TpC		5TpC				2,6,4,5
10	Twsm	Stop Mode Recovery Width Spec	3.5V	12		12		ns		6,7
			5.5V	12		12		ns		6,7
11	Tost	Oscillator Startup Time	3.5V		5TpC		5TpC			6,7
			5.5V		5TpC		5TpC			6,7

Table 18. Additional Timing Table (Divide by Two Mode) $T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$ (Continued)

No	Symbol	Parameter	V_{CC}^1	Min	Max	Min	Max	Units	Conditions	Notes
12	Twdt	Watchdog Timer Delay Time Before Timeout	3.5V	7		10		ms	D0 = 0	8,9
			5.5V	3.5		5		ms	D1 = 0	5,11
			3.5V	14		20		ms	D0 = 1	5,11
			5.5V	7		10		ms	D1 = 0	5,11
			3.5V	28		40		ms	D1 = 0	5,11
			5.5V	14		20		ms	D1 = 1	5,11
			3.5V	112		160		ms	D0 = 1	5,11
			5.5V	56		80		ms	D1 = 1	5,11

Notes

1. The V_{CC} voltage specification of 5.5 V guarantees $5.0\text{ V} \pm 0.5\text{ V}$ and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V.
2. Timing Reference uses 0.7 VC0 for a logic 1 and 0.2 VGC for a logic 0.
3. SMR D1 = 0.
4. SMR-D5 = 1, POR STOP Mode Delay is on
5. Interrupt request via Port 3 (P31-P33)
6. Interrupt request via Port 3 (P30).
7. Maximum frequency for internal system clock is 2 MHz when using Low EMI OSC PCON Bit D7 = 0
8. Reg. WDTMR.
9. Using internal RC.

Pin Functions

EPROM Programming Mode

D7-D0 Data Bus. The data can be read from or written to external memory through the data bus.

V_{CC} Power Supply. This pin must supply 5 V during the EPROM read mode and 6 V during other modes.

$\overline{CE}$ Chip Enable (active Low). This pin is active during EPROM Read Mode, Program Mode, and Program Verify Mode.

$\overline{OE}$ Output Enable (active Low). This pin drives the direction of the Data Bus. When this pin is Low, the Data Bus is output, when High, the Data Bus is input.

EPM EPROM Program Mode. This pin controls the different EPROM Program Mode by applying different voltages.

V_{PP} Program Voltage. This pin supplies the program voltage.

PGM Program Mode (active Low). When this pin is Low, the data is programmed to the EPROM through the Data Bus.

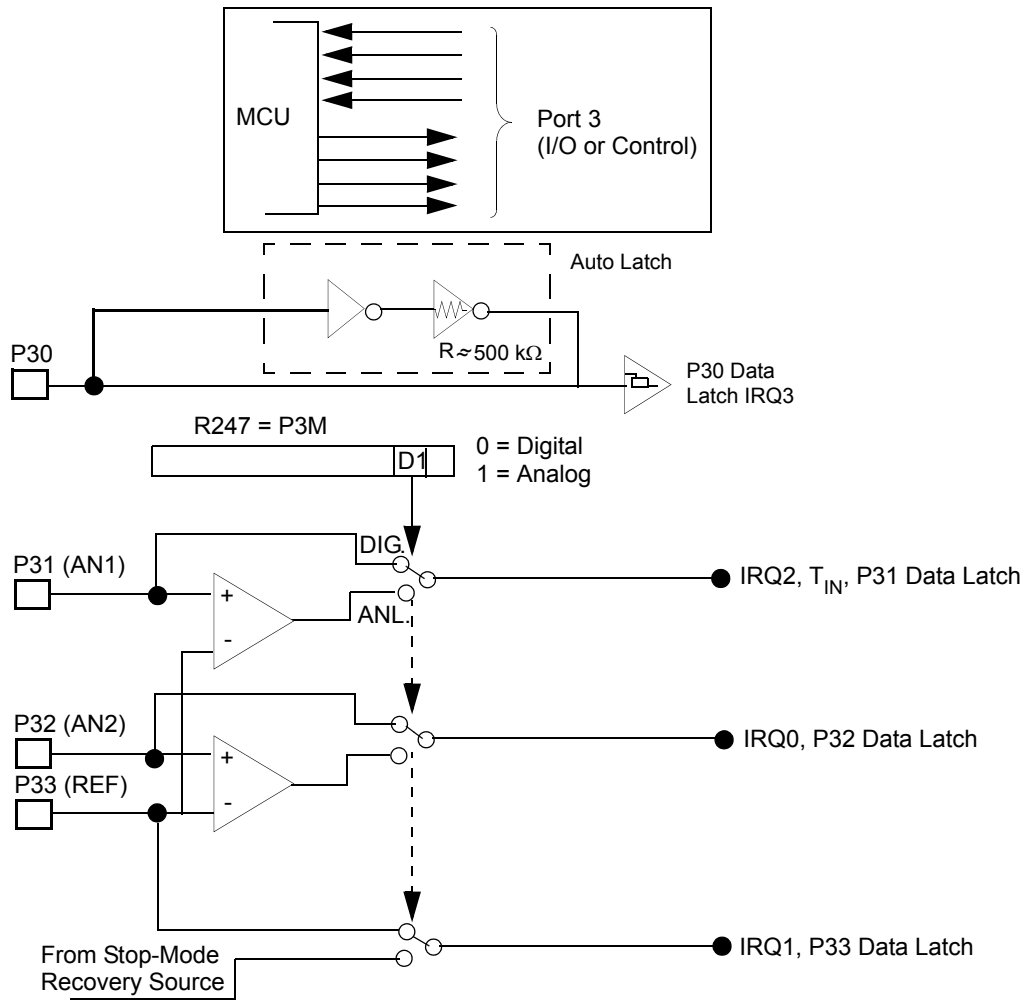


Figure 21. Port 3 Configuration

Reset and initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT is driven either by an on-board RC oscillator or an external oscillator from XTAL1 pin. The POR clock source is selected with bit 4 of the WDT register.

► **Note:** Execution of the WDT instruction affects the Z (Zero), S (Sign), and V (Overflow) flags.

WDT Time-Out Period (D0 and D1). Bits 0 and 1 control a tap circuit that determines the time-out periods that can be obtained (Table 23). The default value of D0 and D1 are 1 and 0, respectively.

Table 23. Time-out Period of WDT

D1	D0	Time-out of the Internal RC OSC	Time-out of the System Clock
0	0	5 ms	128 SCLK
0	1	10 ms ¹	256 SCLK ¹
1	0	20 ms	512 SCLK
1	1	80 ms	2048 SCLK

Note: The default setting is 10 ms.

WDT During HALT Mode (D2). This bit determines whether or not the WDT is active during HALT Mode. A “1” indicates that the WDT is active during HALT. A “0” disables the WDT in HALT Mode. The default value is “1”. **WDT During STOP Mode (D3).** This bit determines whether or not the WDT is active during STOP mode. A “1” indicates active during STOP. A “0” disables the WDT during STOP Mode. This is applicable only when the WDT clock source is the internal RC oscillator.

Clock Source For WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1, and the WDT is stopped in STOP Mode. The default configuration of this bit is 0, which selects the RC oscillator.

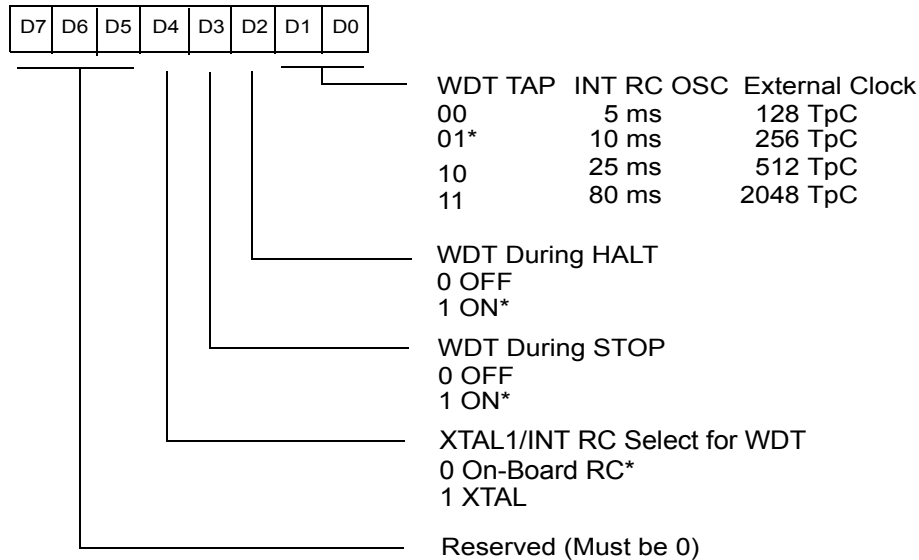
Permanent WDT. When this feature is enabled, the WDT is enabled after reset and will operate in Run and HALT Mode. The control bits in the WDTMR do not affect the WDT operation. If the clock source of the WDT is the internal RC oscillator, then the WDT will run in STOP mode. If the clock source of the WDT is the XTAL1 pin, then the WDT will not run in STOP mode.

► **Note:** *WDT time-out in STOP Mode will not reset SMR, SMR2, PCON, WDTMR, P2M, P3M, Ports 2 & 3 Data Registers, but will activate the T_{POR} delay.*

WDTMR Register Accessibility. The WDTMR register is accessible only during the first 60 internal system clock cycles from the execution of the first instruction after Power-On Reset, Watchdog reset or a Stop Mode Recovery (Figure 33 and Figure 34). After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register File at address location 0Fh.

Clock Free WDT Reset. The WDT will enable the Z8 to reset the I/O pins whenever the WDT times out, even without a clock source running on the XTAL1 and XTAL2 pins. WDTMR Bit D4 must be 0 for the clock Free WDT to work. The I/O pins will default to their default settings.

WDTMR (F) 0F



* Default setting after RESET

Figure 33. Watchdog Timer Mode Register Write Only

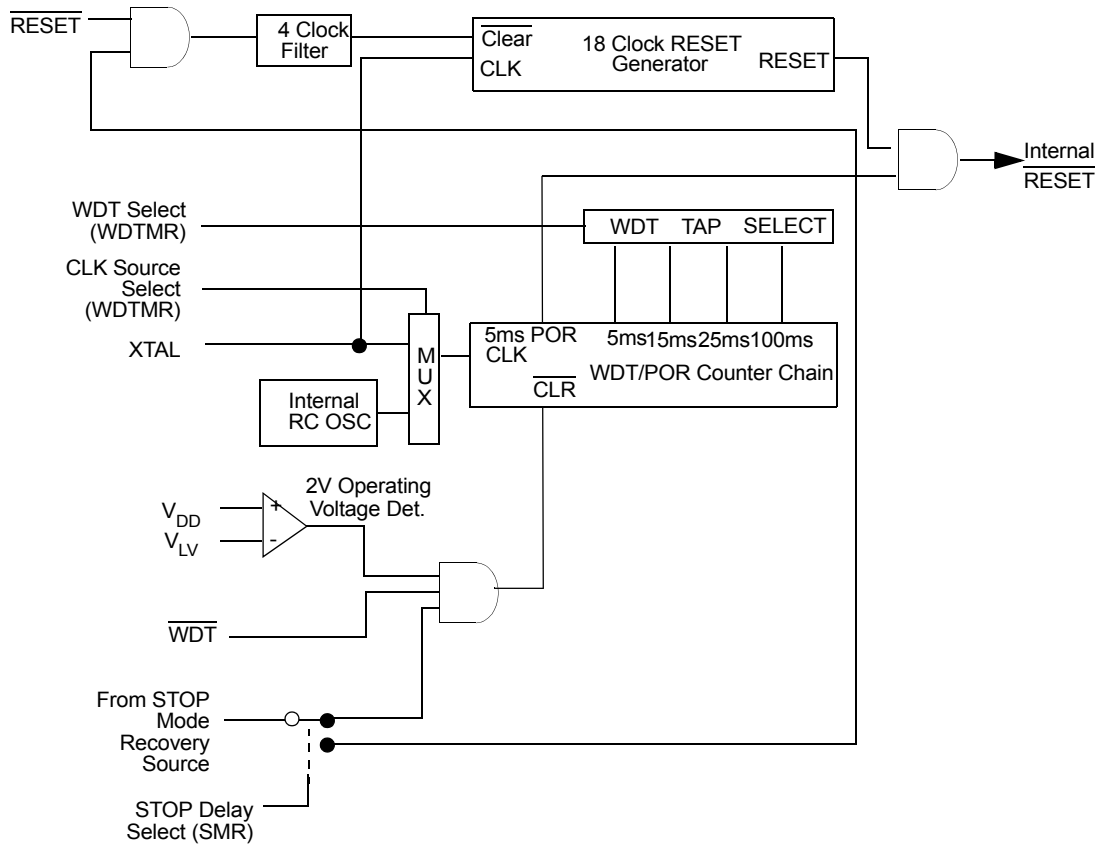
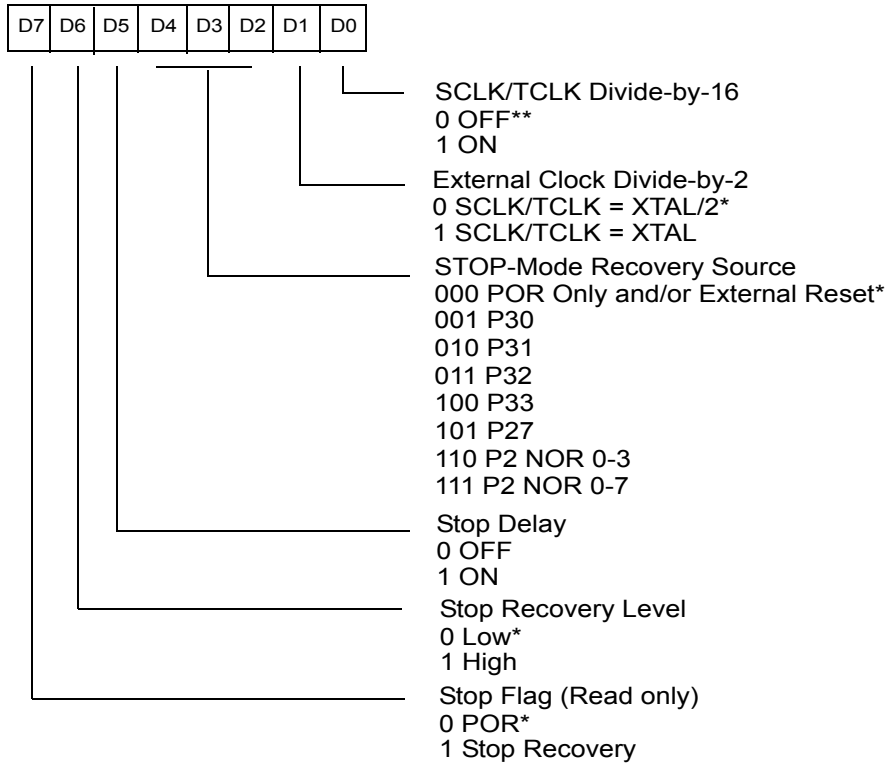


Figure 34. Resets and WDT

Auto Reset Voltage. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. Reset is globally driven if V_{CC} is below VLV (Figure 35).

SMR (Fh) 0B



Note: Note used in conjunction with SMR2 Source

* Default setting after RESET

** Default setting after RESET and STOP-Mode Recovery

Figure 37. Stop Mode Recovery Register (Write Only Except Bit D7, Which is Read Only)

R240

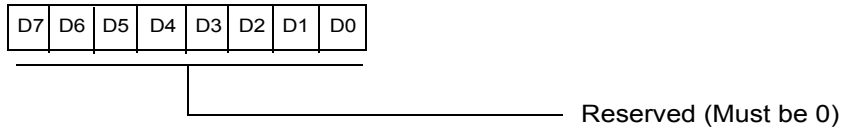
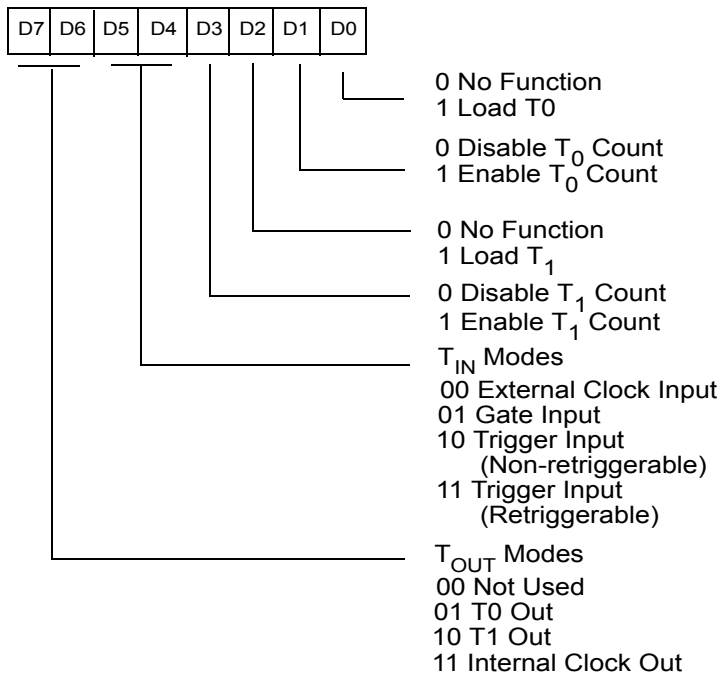


Figure 40. Reserved

R241 Timer



Default After Reset = 00h

Figure 41. Timer Mode Register (F1_n: Read/Write)

R245 PRE0

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

Count Mode
0 = T_1 Single Pass
1 = T_1 Modulo N

Reserved (Must be 0)

Prescaler Modulo
(Range: 1-64 Decimal
01-00 HEX)

Figure 45. Prescaler 0 Register (F5_h: Write Only)

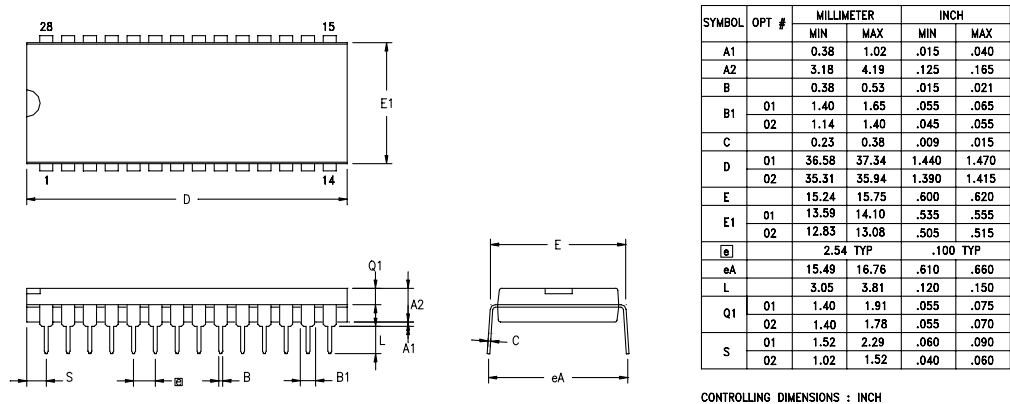
R246 P2M

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

P20 - P27 I/O Definition
0 Defines Bit as output
1 Defines Bit as input

* Default after Reset

Figure 46. Port 2 Mode Register (F6_h: Write Only)



OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

Figure 58. 28-Pin DIP Package Diagram

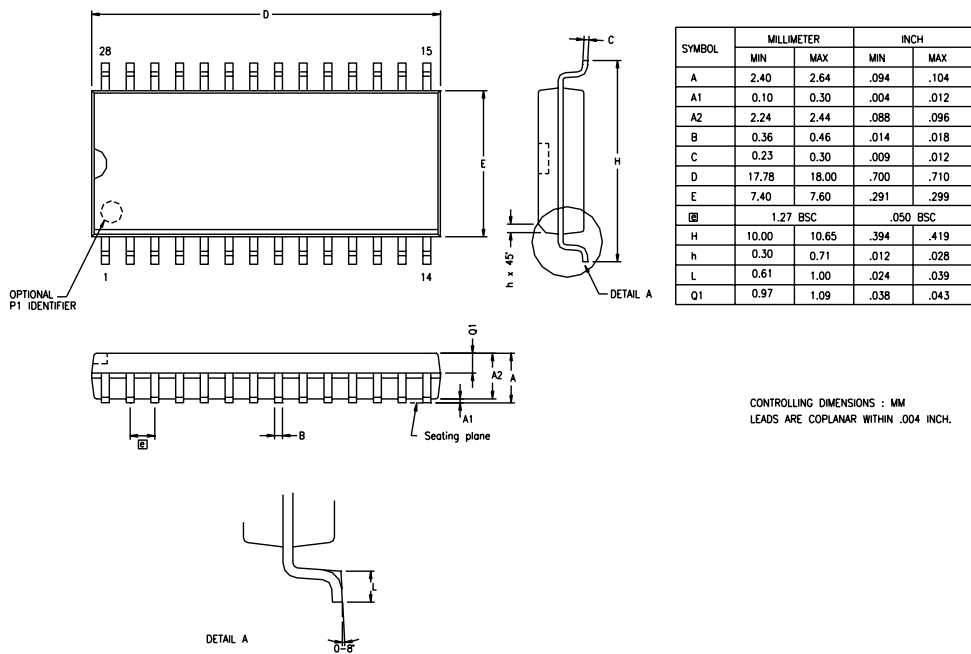


Figure 59. 28-Pin SOIC Package Diagram