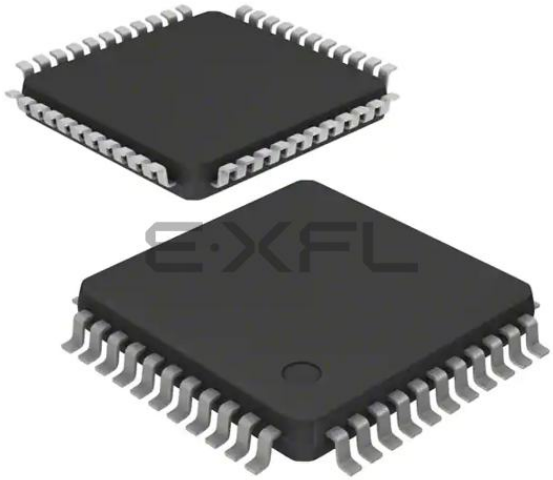

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	EBI/EMI
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e4312fsc00tr

Table 4. 44-Pin LQFP Pin Identification (Continued)

Pin No	Symbol	Function	Direction
18	RESET	Reset	Input
19	P35	Port 3, Pin 5	Output
20	P37	Port 3, Pin 7	Output
21	P36	Port 3, Pin 6	Output
22	P30	Port 3, Pin 0	Input
23-24	P00-P01	Port 0, Pin 0,1	Input/Output
25-26	P10-P11	Port 1, Pins 0,1	Input/Output
27	P02	Port 0, Pin 2	Input/Output
28-29	GND	Ground	
30-31	P12-P13	Port 1, Pins 2,3	Input/Output
32	P03	Port 0, Pin 3	Input/Output
33-37	P20-24	Port 2, Pins 0,1,2,3,4	Input/Output
38	DS	Data Strobe	Output
39	NC	No Connection	
40	R/$\overline{W}$	Read/Write	Output
41-43	P25-P27	Port 2, Pins 5,6,7	Input/Output
44	P04	Port 0, Pin 4	Input/Output

Table 7. 44-Pin LQFP Pin Identification EPROM Programming Mode (Continued)

Pin No	Symbol	Function	Direction
33-37	D0-D4	Data 0,1,2,3,4	Input/Output
38-40	NC	No Connection	
41-43	D5-D7	Data 5,6,7	Input/Output
44	NC	No Connection	

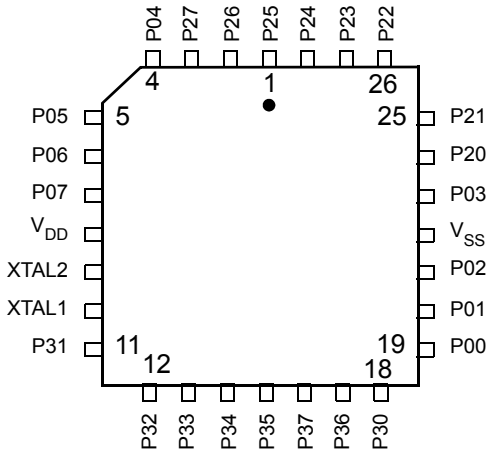


Figure 10. Standard Mode 28-Pin PLCC Pin Configuration

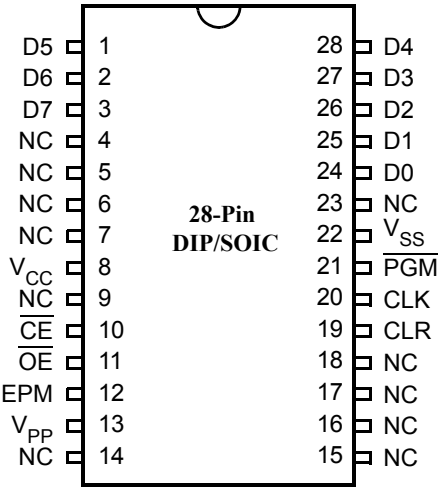


Figure 11. EPROM Programming Mode 28-Pin DIP/SOIC Pin Configuration

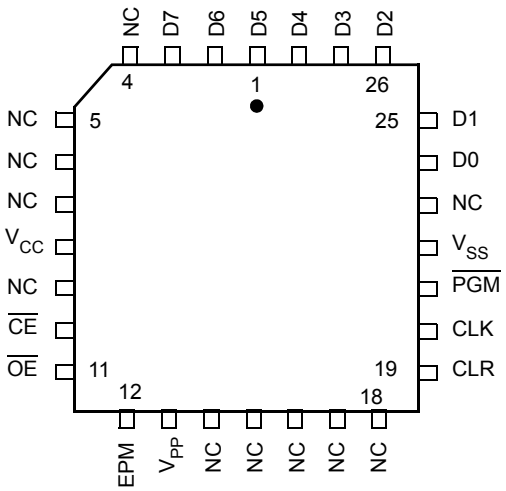


Figure 12. EPROM Programming Mode 28-Pin PLCC Pin Configuration

Table 9. 28-Pin EPROM Pin Identification EPROM Mode

Pin #	Symbol	Function	Direction
1-3	D5-D7	Data 5,6,7	Input/Output
4-7	NC	No Connection	
8	V_{CC}	Power Supply	
9	NC	No connection	
10	CE	Chip Select	Input
11	OE	Output Enable	Input
12	EPM	EPROM Prog. Mode	Input
13	V_{PP}	Prog. Voltage	Input
14-18	NC	No Connection	
19	CLR	Clear	
20	CLK	Clock	
21	/PGM	Prog. Mode	Input
22	V_{SS}	Ground	
23	NC	No Connection	
24-28	D0-D4	Data 0,1,2,3,4	Input/Output

Table 12. DC Electrical Characteristics T_A= -40 °C to +105 °C (Continued)

Symbol	Parameter	V_{CC} [1]	Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{OH1}	Output High Voltage	4.5V	V_{CC} -0.4		4.8	V	I_{OH} = -2.0 mA	2
		5.5V	V_{CC} -0.4		4.8	V	I_{OH} = -2.0 mA	2
V_{OL}	Output Low Voltage Low EMI Mode	4.5V		0.4	0.2	V	I_{OL} = 1.0 mA	
		5.5V		0.4	0.2	V	I_{OL} = 1.0 mA	
V_{OL1}	Output Low Voltage	4.5V		0.4	0.1	V	I_{OL} = +4.0 mA	2
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	2
V_{OL2}	Output Low Voltage	4.5V		1.2	0.5	V	I_{OL} = +12 mA	2
		5.5V		1.2	0.5	V	I_{OL} = +12 mA	2
V_{RH}	Reset Input High Voltage	4.5V	.8 V_{CC}	V_{CC}	1.7	V		3
		5.5V	.8 V_{CC}	V_{CC}	2.1	V		3
V_{OLR}	Reset Output Low Voltage	4.5V		0.6	0.3	V	I_{OL} = 1.0 mA	3
		5.5V		0.6	0.2	V	I_{OL} = 1.0 mA	3
V_{OFFSET}	Comparator Input Offset Voltage	4.5V		25	10	mV		
		5.5V		25	10	mV		
V_{ICR}	Input Common Mode Voltage Range	4.5V	0	V_{CC} -1.5V		V		4
		5.5V	0	V_{CC} -1.5V		V		4
I_{IL}	Input Leakage	4.5V	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	4.5V	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	4.5V	-18	-180	-112	µA		3
		5.5V	-18	-180	-112	µA		3
I_{CC}	Supply Current	4.5V		20	15	mA	@ 12 MHz	5,6
		5.5V		20	15	mA	@ 12 MHz	5,6
I_{CC1}	Standby Current HALT Mode	4.5V		6	2	mA	V_{IN} = 0V, V_{CC} @ 12 MHz	5,6
		5.5V		6	4	mA	V_{IN} = 0V, V_{CC} @ 12 MHz	5,6

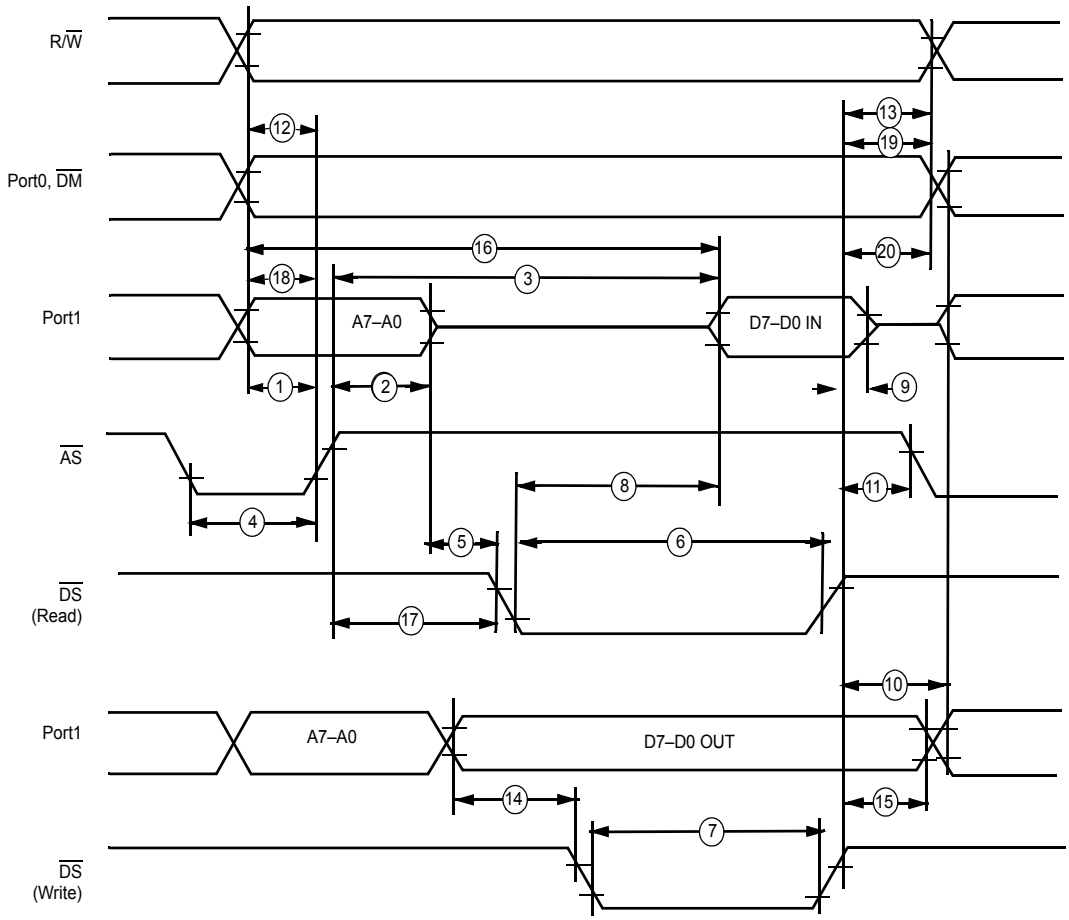


Figure 14. External I/O or Memory Read/Write Timing (Z86E43/743/E44 Only)

Table 13. DC Electrical Characteristics T_A = 0 °C to +70 °C, 12 MHz

No.	Symbol	Parameter	V_{CC} [1]	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to $\overline{AS}$ Rise Delay	3.5V	35		ns	2
			5.5V	35		ns	2
2	TdAS(A)	$\overline{AS}$ Rise to Address Float Delay	3.5V	45		ns	2
			5.5V	45		ns	2
3	TdAS(DR)	$\overline{AS}$ Rise to Read Data Req'd Valid	3.5V		250	ns	2,3
			5.5V		250	ns	2,3

Table 13. DC Electrical Characteristics T_A = 0 °C to +70 °C, 12 MHz (Continued)

No.	Symbol	Parameter	V_{CC} [1]	Min	Max	Units	Notes
18	TdDM(AS)	$\overline{DM}$ Valid to $\overline{AS}$ Rise Delay	3.5V	35		ns	2
			5.5V	35		ns	2
19	ThDS(AS)	$\overline{DS}$ Valid to Address Valid Hold Time	3.5V	35		ns	2
			5.5V	35		ns	2

Notes

1. The V_{CC} voltage specification of 5.5 V guarantees 5.0 V ± 0.5 V and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V.
2. Timing numbers given are for minimum TpC.
3. When using extended memory timing, add 2 TpC

Standard Test Load

All timing references use 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

For Standard Mode (not Low-EMI Mode for outputs) with SMR, D1 = 0, D0 = 0.

Table 14. DC Electrical Characteristics T_A = -40 °C to +105 °C, 12 MHz

No.	Symbol	Parameter	V_{CC} [1]	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to $\overline{AS}$ Rise Delay	4.5V	35		ns	2
			5.5V	35		ns	2
2	TdAS(A)	$\overline{AS}$ Rise to Address Float Delay	4.5V	45		ns	2
			5.5V	45		ns	2
3	TdAS(DR)	$\overline{AS}$ Rise to Read Data Req'd Valid	4.5V		250	ns	2,3
			5.5V		250	ns	2,3
4	TwAS	$\overline{AS}$ Low Width	4.5V	55		ns	2
			5.5V	55		ns	2
5	TdAS(DS)	Address Float to $\overline{DS}$ Fall	4.5V	0		ns	
			5.5V	0		ns	
6	TwDSR	$\overline{DS}$ (Read) Low Width	4.5V	200		ns	2,3
			5.5V	200		ns	2,3
7	TwDSW	$\overline{DS}$ (Write) Low Width	4.5V	110		ns	2,3
			5.5V	110		ns	2,3
8	TdDSR(DR)	$\overline{DS}$ Fail to Read Data Req'd Valid	4.5V		150	ns	2,3
			5.5V		150	ns	2,3
9	ThDR(DS)	Read Data to $\overline{DS}$ Rise Hold Time	4.5V	0		ns	2
			5.5V	0		ns	2

Table 14. DC Electrical Characteristics T_A = -40 °C to +105 °C, 12 MHz (Continued)

No.	Symbol	Parameter	V_{CC}[1]	Min	Max	Units	Notes
10	TdDS(A)	$\overline{DS}$ Rise to Address Active Delay	4.5V	45		ns	2
			5.5V	55		ns	2
11	TdDS(AS)	$\overline{DS}$ Rise to $\overline{AS}$ Fall Delay	4.5V	45		ns	2
			5.5V	45		ns	2
12	TdR/W(AS)	R/$\overline{W}$ Valid to $\overline{AS}$ Rise Delay	4.5V	45		ns	2
			5.5V	45		ns	2
13	TdDS(R/W)	$\overline{DS}$ Rise to R/$\overline{W}$ Not Valid	4.5V	45		ns	2
			5.5V	45		ns	2
14	TdDW(DSW)	Write Data Valid to $\overline{DS}$ Fall (Write) Delay	4.5V	55		ns	2
			5.5V	55		ns	2
15	TdDS(DW)	$\overline{DS}$ Rise to Write Data Not Valid Delay	4.5V	55		ns	2
			5.5V	55		ns	2
16	TdA(DR)	Address Valid to Read Data Req'd Valid	4.5V		310	ns	2,3
			5.5V		310	ns	2,3
17	TdAS(DS)	$\overline{AS}$ Rise to $\overline{DS}$ Fall Delay	4.5V	65		ns	2
			5.5V	65		ns	2
18	TdDM(AS)	$\overline{DM}$ Valid to $\overline{AS}$ Rise Delay	4.5V	35		ns	2
			5.5V	35		ns	2
19	ThDS(AS)	$\overline{DS}$ Valid to Address Valid Hold Time	4.5V	35		ns	2
			5.5V	35		ns	2

Notes

1. The V_{CC} voltage specification of 5.5 V guarantees 5.0 V ± 0.5 V and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V.
2. Timing numbers given are for minimum TpC.
3. When using extended memory timing, add 2 TpC.

Standard Test Load

All timing references use 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

For Standard Mode (not Low-EMI Mode for outputs) with SMR, D1 = 0, D0 = 0.

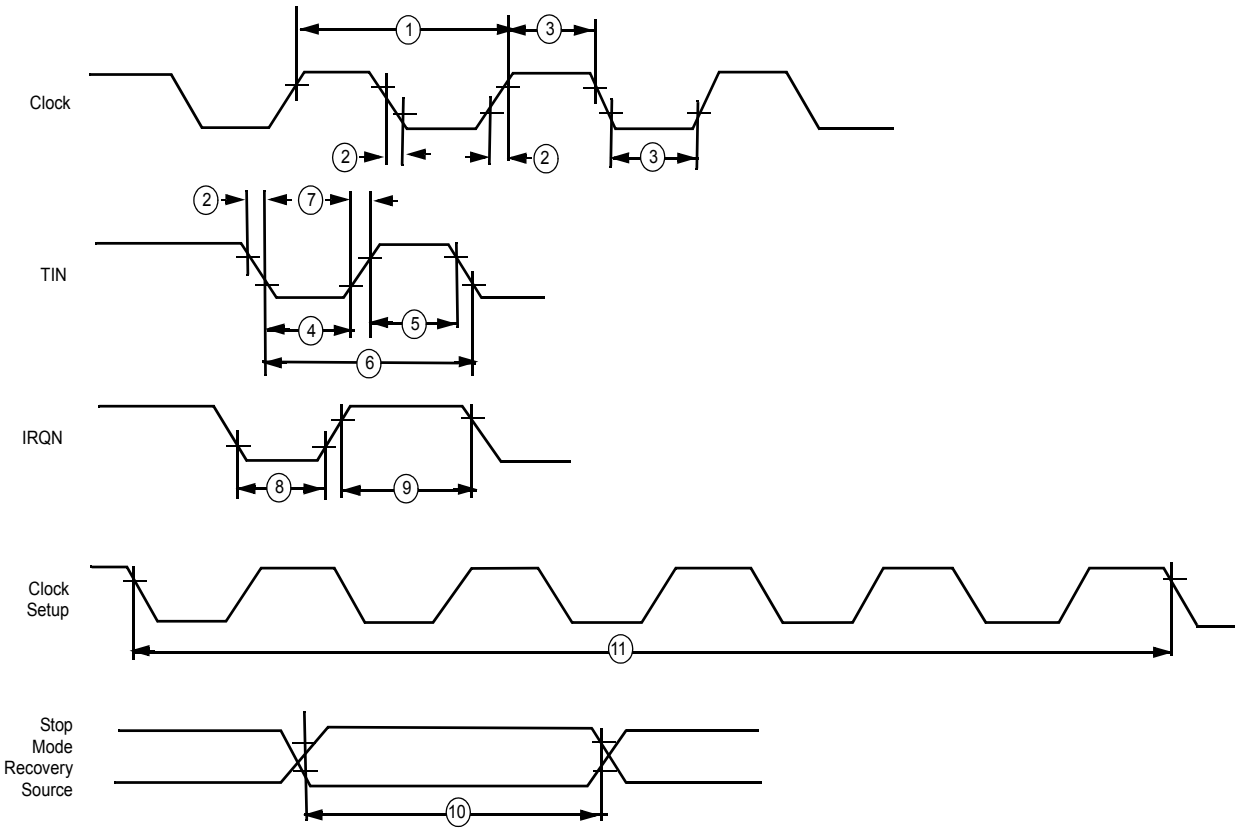


Figure 15. Additional Timing Diagram

Table 15. Additional Timing Table (Divide-By-One Mode) T_A = 0 °C to +70 °C

No	Symbol	Parameter	V_{CC} [1]	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.5V	250	DC	166	DC	ns	2,3,4
			5.5V	250	DC	166	DC	ns	2,3,4
2	TrC,TfC	Clock Input Rise & Fall Times	3.5V		25		25	ns	2,3,4
			5.5V		25		25	ns	2,3,4
3	TwC	Input Clock Width	3.5V	100		100		ns	2,3,4
			5.5V	100		100		ns	2,3,4
4	TwTinL	Timer Input Low Width	3.5V	100		100		ns	2,3,4
			5.5V	70		70		ns	2,3,4

Table 18. Additional Timing Table (Divide by Two Mode) T_A = -40 °C to +105 °C (Continued)

No	Symbol	Parameter	V_{CC} [1]	Min	Max	Min	Max	Units	Conditions	Notes
12	Twdt	Watchdog Timer Delay Time Before Timeout	3.5V	7		10		ms	D0 =0	8,9
			5.5V	3.5		5		ms	D1 = 0	5,11
			3.5V	14		20		ms	D0 =1	5,11
			5.5V	7		10		ms	D1 = 0	5,11
			3.5V	28		40		ms	D1 = 0	5,11
			5.5V	14		20		ms	D1 = 1	5,11
			3.5V	112		160		ms	D0 = 1	5,11
			5.5V	56		80		ms	D1 = 1	5,11

Notes
1. The V_{CC} voltage specification of 5.5 V guarantees 5.0 V ± 0.5 V and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V.
2. Timing Reference uses 0.7 VC0 for a logic 1 and 0.2 VGC for a logic 0.
3. SMR D1 = 0.
4. SMR-D5 = 1, POR STOP Mode Delay is on
5. Interrupt request via Port 3 (P31-P33)
6. Interrupt request via Port 3 (P30).
7. Maximum frequency for internal system clock is 2 MHz when using Low EMI OSC PCON Bit D7 = 0
8. Reg. WDTMR.
9. Using internal RC.

Pin Functions

EPROM Programming Mode

D7-D0 Data Bus. The data can be read from or written to external memory through the data bus.

V_{CC} Power Supply. This pin must supply 5 V during the EPROM read mode and 6 V during other modes.

$\overline{CE}$ Chip Enable (active Low). This pin is active during EPROM Read Mode, Program Mode, and Program Verify Mode.

$\overline{OE}$ Output Enable (active Low). This pin drives the direction of the Data Bus. When this pin is Low, the Data Bus is output, when High, the Data Bus is input.

EPM EPROM Program Mode. This pin controls the different EPROM Program Mode by applying different voltages.

V_{PP} Program Voltage. This pin supplies the program voltage.

PGM Program Mode (active Low). When this pin is Low, the data is programmed to the EPROM through the Data Bus.

The Z86E43/743/E44 does not reset WDTMR, SMR, P2M, and P3M registers on a Stop-Mode Recovery operation.

$\overline{\text{ROMless}}$ (input, active Low). This pin, when connected to GND, disables the internal ROM and forces the device to function as a Z86C90/C89 ROMless Z8. (Note that, when left unconnected or pulled High to V_{CC}, the device functions nor

Note: *When using in ROM Mode in High EMI (noisy) environment, the ROMless pins should be connected directly to V_{CC}.*

$\overline{\text{DS}}$ (output, active Low). Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of $\overline{\text{DS}}$. For WRITE operations, the falling edge of $\overline{\text{DS}}$ indicates that output data is valid.

$\overline{\text{AS}}$ (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle for external memory transfer. Address output is from Port 0/Port 1 for all external programs. Memory address transfers are valid at the trailing edge of $\overline{\text{AS}}$. Under program control, $\overline{\text{AS}}$ is placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

Port 0 (P07-P00). Port 0 is an 8-bit, bidirectional, CMOS-compatible I/0 port. These eight I/O lines can be configured under software control as a nibble I/0 port, or as an address port for interfacing external memory. The input buffers are Schmitt-triggered and nibble programmed. Either nibble output that can be globally programmed as push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 0 can be placed under handshake control. In Handshake Mode, Port 3 lines P32 and P35 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to Port 0's upper nibble. The lower nibble must have the same direction as the upper nibble.

For external memory references, Port 0 provides address bits A11-A8 (lower nibble) or Al 5-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. In ROMless mode, after a hardware reset, Port 0 is configured as address lines Al 5-A8, and extended timing is set to accommodate slow memory access. The initialization routine can include re-configuration to eliminate this extended timing mode. In ROM mode, Port 0 is defined as input after reset.

Port 0 can be set in the High-Impedance Mode if selected as an address output state, along with Port 1 and the control signals $\overline{\text{AS}}$, $\overline{\text{DS}}$, and R/$\overline{\text{W}}$ (Figure 18).

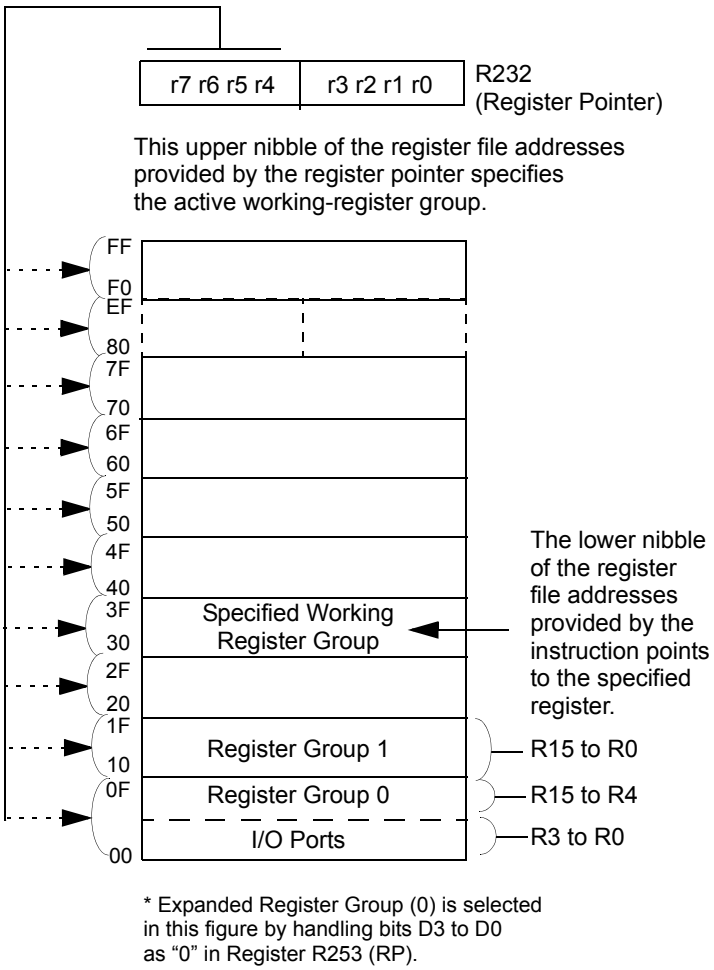


Figure 25. Register Pointer

```
FF    NOP    ; clear the pipeline
6F    STOP   ; enter STOP mode
```

or

```
FF    NOP    ; clear the pipeline
7F    HALT   ; enter HALT mode
```

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 microamperes or less. STOP Mode is terminated by one of the following resets: either by WDT time-out, POR, a Stop Mode Recovery Source, which is defined by the SMR register or external reset. This causes the processor to restart the application program at address 000Ch.

Port Configuration Register (PCON). The PCON register configures the ports individually; comparator output on Port 3, open-drain on Port 0 and Port 1, low EMI on Ports 0, 1, 2 and 3, and low EMI oscillator. The PCON register is located in the expanded register file at Bank F, location 00 (Figure 30).

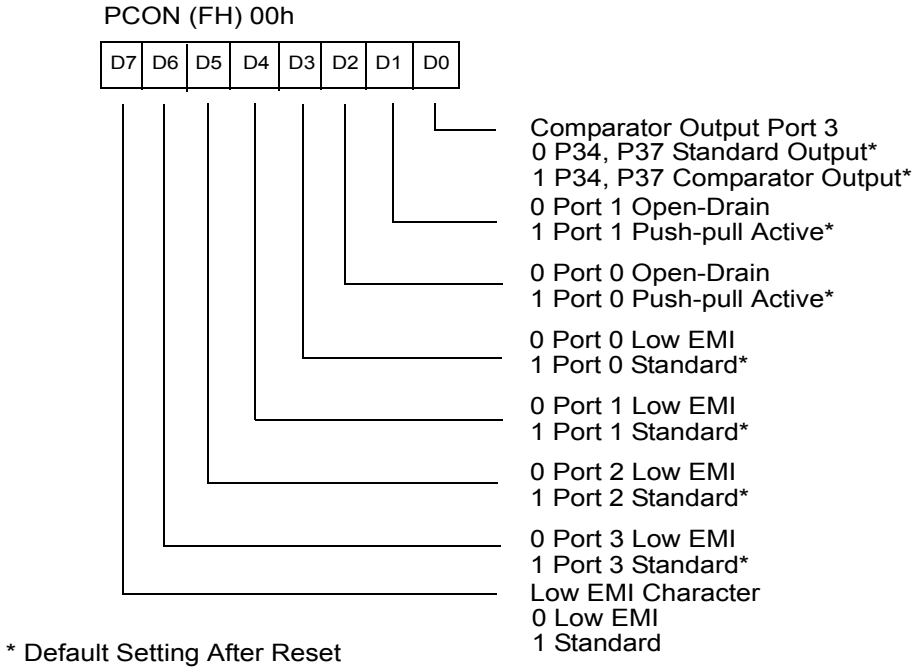


Figure 30. Port Configuration Register (PCON) (Write Only)

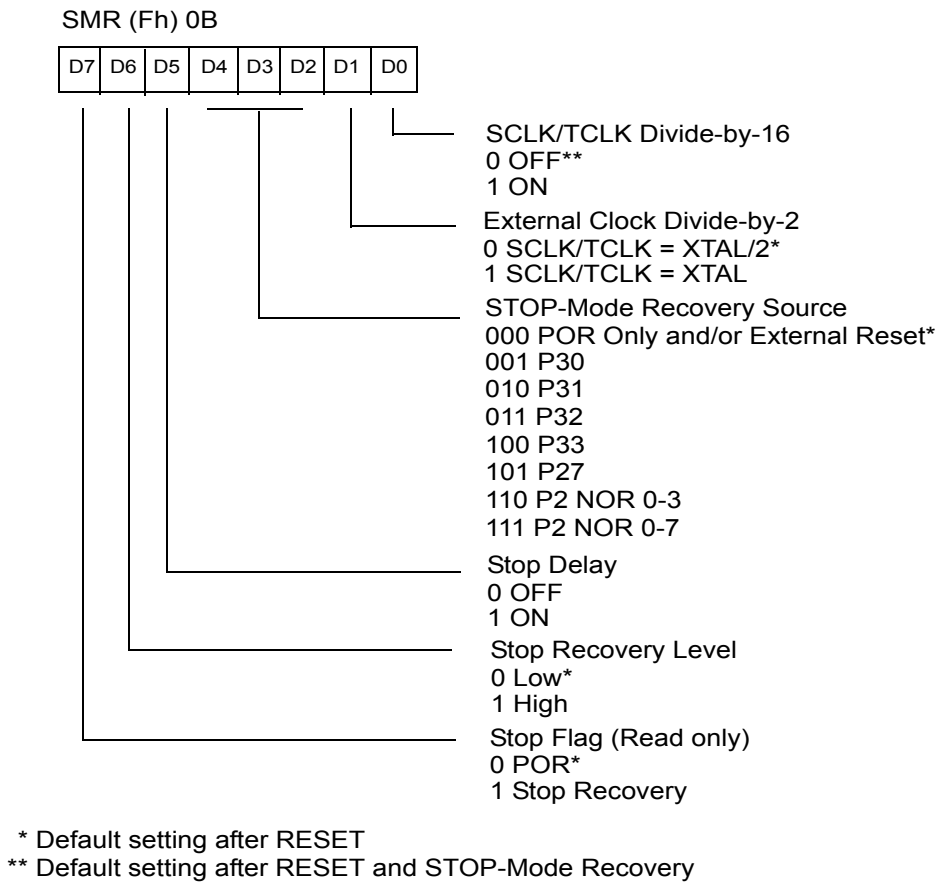


Figure 31. Stop Mode Recovery Register (Write-Only Except Bit D7, Which Is Read-Only)

SCLK/TCLK Divide-by-16 Select (D0). This bit of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources counter/timers and interrupt logic).

External Clock Divide-by-Two (D1). This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, the System Clock (SCLK) and Timer Clock (TCLK) are equal to the external clock frequency divided by two. The SCLK/TCLK is equal to the external clock frequency when this bit is set (D1=1). Using this bit together with D7 of PCON further helps lower EMI (that is, D7 (PCON) = 0, D1 (SMR) = 1). The default setting is zero.

Stop Mode Recovery Source (D2, D3, and D4). These three bits of the SMR register specify the wake up source of the Stop Mode Recovery (Figure 32). Table 22 shows the SMR source selected with the setting of D2 to D4. P33-P31 cannot be used to wake up

from STOP mode when programmed as analog inputs. When the Stop Mode Recovery sources are selected in this register then SMR2 register bits D0, D1 must be set to zero.

Note: *If the Port 2 pin is configured as an output, this output level will be read by the SMR circuitry.*

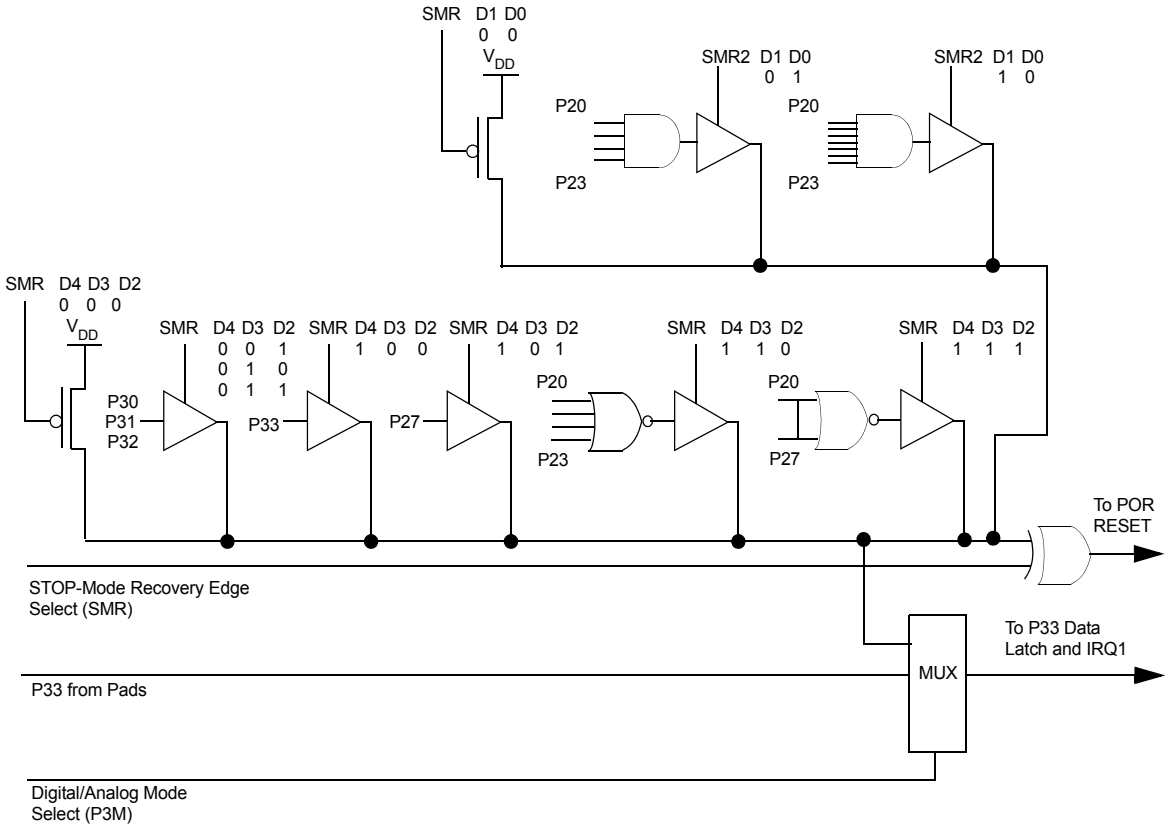


Figure 32. Stop Mode Recovery Source

Table 22. Stop Mode Recovery Source

D4	D3	D2	SMR Source selection
0	0	0	POR recovery only
0	0	1	P30 transition
0	1	0	P31 transition (Not in analog mode)
0	1	1	P32 transition (Not in analog mode)
1	0	0	P33 transition (Not in analog mode)
1	0	1	P27 transition
1	1	0	Logical NOR of Port 2 bits 0-3
1	1	1	Logical NOR of Port 2 bits 0-7

Stop Mode Recovery Delay Select (D5). The 5 ms RESET delay after Stop Mode Recovery is disabled by programming this bit to a zero. A "1" in this bit will cause a 5 ms RESET delay after Stop Mode Recovery. The default condition of this bit is 1. If the fast wake up mode is selected, the Stop Mode Recovery source needs to be kept active for at least 5TpC.

Stop Mode Recovery Level Select (D6). A "1" in this bit defines that a high level on any one of the recovery sources wakes the MCU from STOP Mode. A 0 defines low level recovery. The default value is 0.

Cold or Warm Start (D7). This bit is set by the device upon entering STOP Mode. A "0" in this bit indicates that the device has been reset by POR (cold). A "1" in this bit indicates the device was awakened by a SMR source (warm).

Stop Mode Recovery Register 2 (SMR2). This register contains additional Stop Mode Recovery sources. When the Stop Mode Recovery sources are selected in this register then SMR Register Bits D2, D3, and D4 must be 0.

SMR:10		Operation
D1	DO	Description of Action
0	0	POR and/or external reset recovery
0	1	Logical AND of P20 through P23
1	0	Logical AND of P20 through P27

Watchdog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is disabled after Power-On

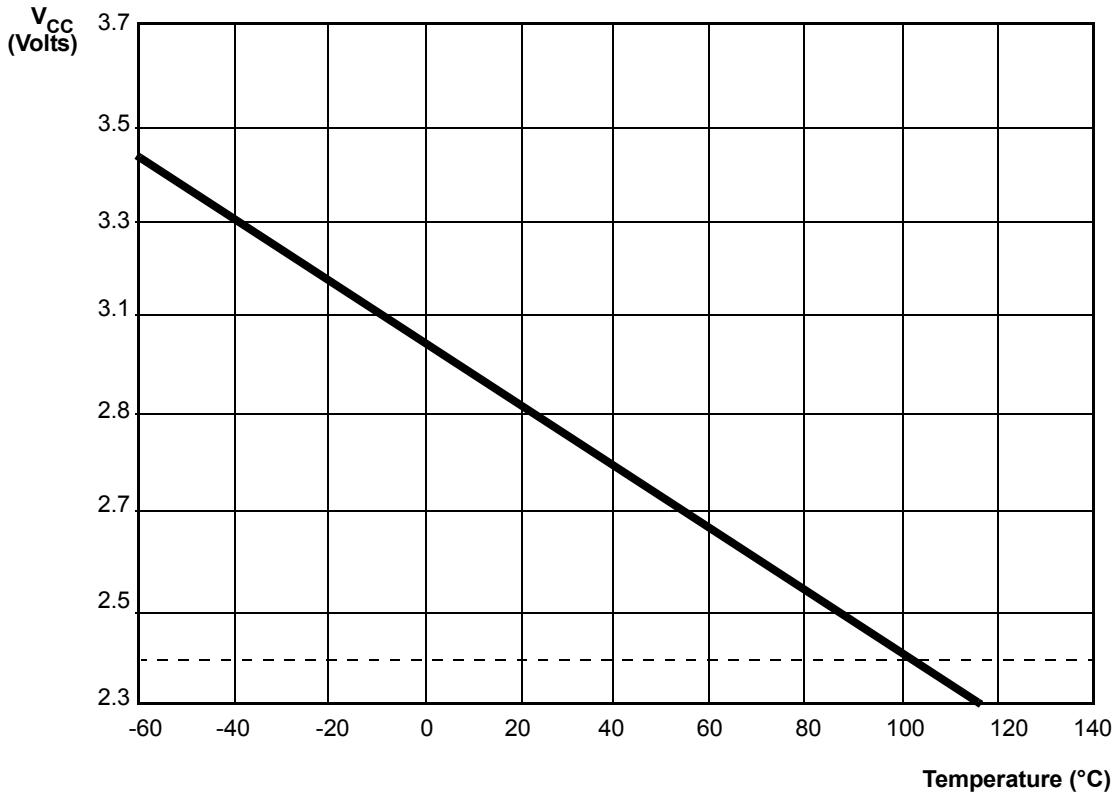


Figure 35. Typical V_{LV} Voltage vs. Temperature

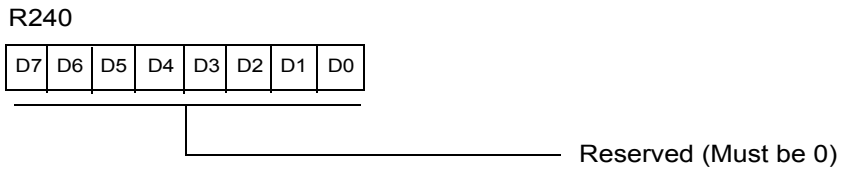


Figure 40. Reserved

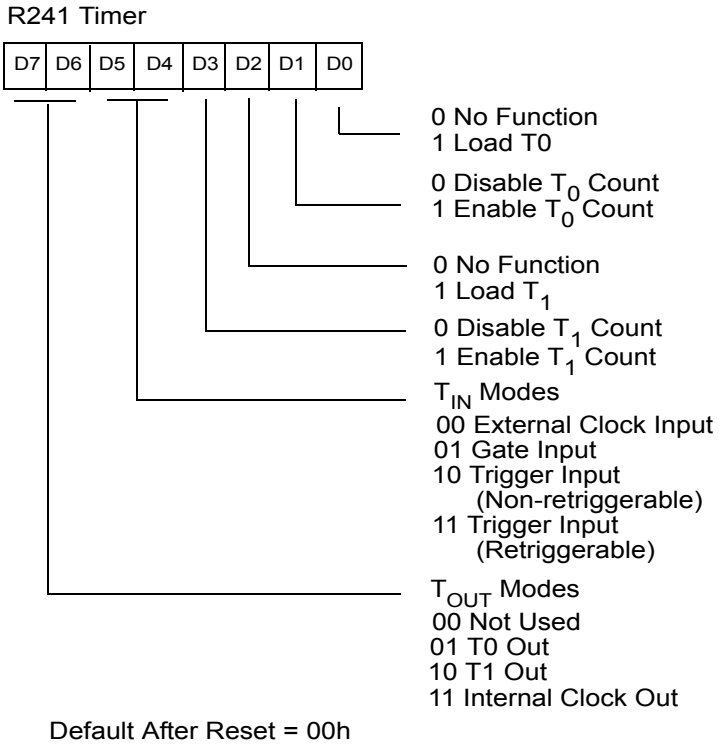
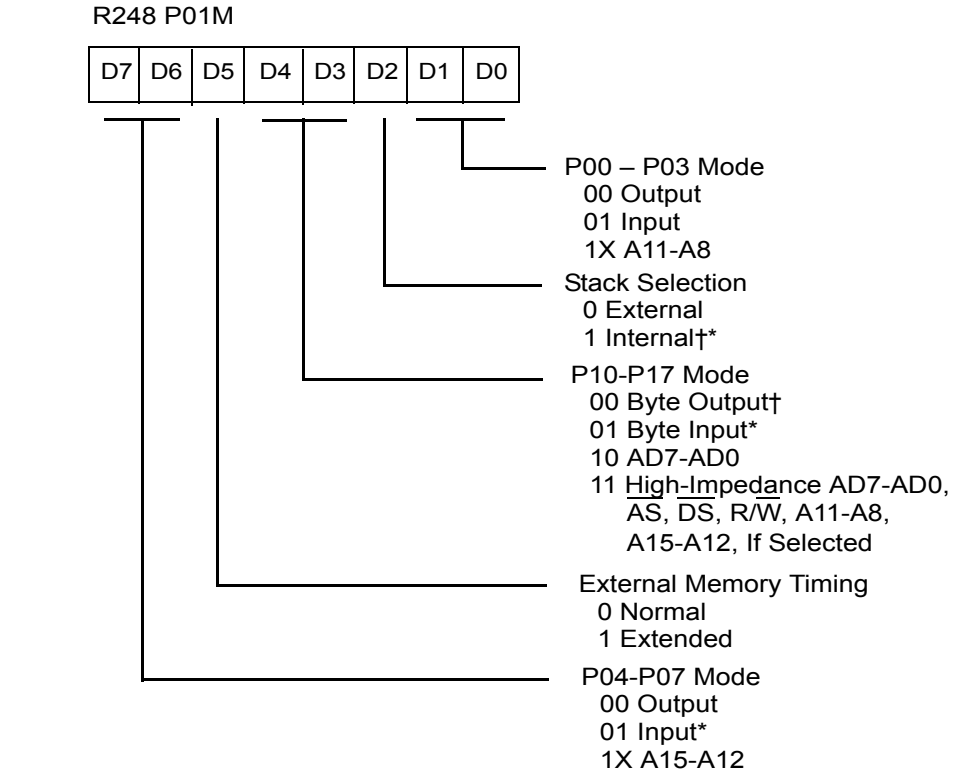
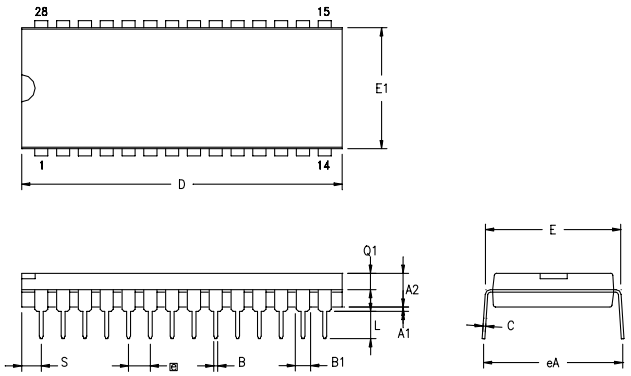


Figure 41. Timer Mode Register ($F1_h$: Read/Write)



Reset Condition = 0100 1101B
For ROMless Condition = 1011 0110B
† Z86E33/733/E34 Must be 00
* Default after Reset

Figure 48. Port 0 and 1 Mode Register ($F8_h$: Write Only)

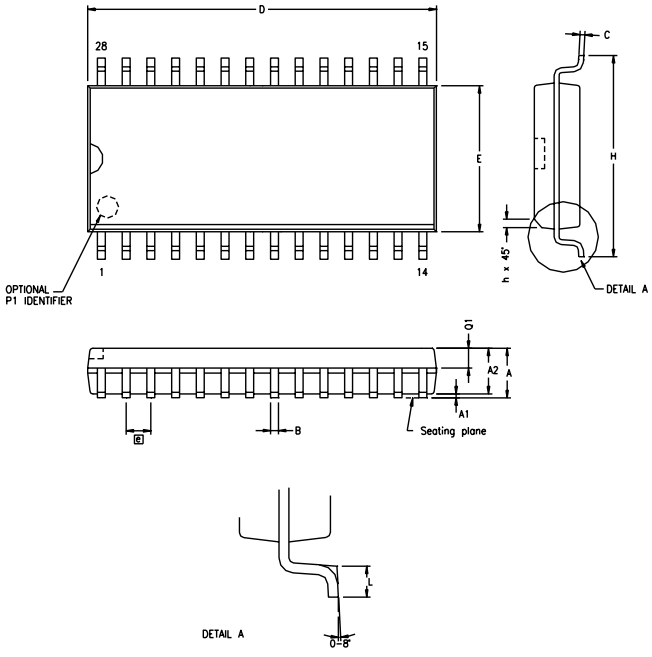


SYMBOL	OPT #	MILLIMETER		INCH	
		MIN	MAX	MIN	MAX
A1		0.38	1.02	.015	.040
A2		3.18	4.19	.125	.165
B		0.38	0.53	.015	.021
B1	01	1.40	1.65	.055	.065
	02	1.14	1.40	.045	.055
C		0.23	0.38	.009	.015
D	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
e		2.54 TYP		.100 TYP	
eA		15.49	16.76	.610	.660
L		3.05	3.81	.120	.150
Q1	01	1.40	1.91	.055	.075
	02	1.40	1.78	.055	.070
S	01	1.52	2.29	.060	.090
	02	1.02	1.52	.040	.060

CONTROLLING DIMENSIONS : INCH

OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

Figure 58. 28-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.64	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	17.78	18.00	.700	.710
E	7.40	7.60	.291	.299
e	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.71	.012	.028
L	0.61	1.00	.024	.039
Q1	0.97	1.09	.038	.043

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 59. 28-Pin SOIC Package Diagram