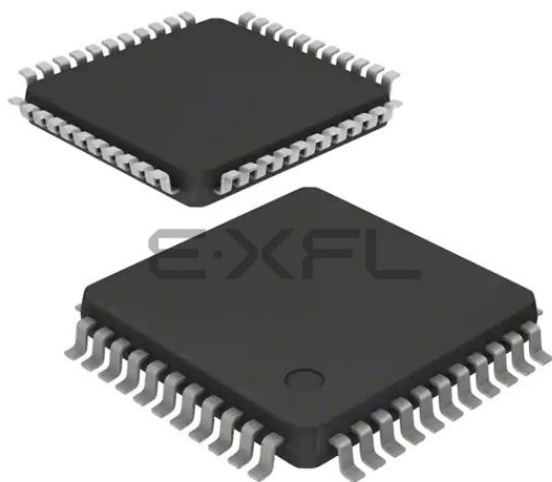




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Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	EBI/EMI
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e4312fsg

Revision History

Each instance in Revision History reflects a change to this document from its previous revision. For more details, refer to the corresponding pages and appropriate links in the table below.

Date	Revision Level	Description	Page No
May 2008	01	Original issue.	All

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Table 2. 40-Pin DIP Pin Identification Standard Mode (Continued)

Pin No	Symbol	Function	Direction
15	XTAL1	Crystal Oscillator	Input
16-18	P31-P33	Port 3, Pins 1,2,3	Input
19	P34	Port 3, Pin 4	Output
20	AS	Address Strobe	Output
21	RESET	Reset	Input
22	P35	Port 3, Pin 5	Output
23	P37	Port 3, Pin 7	Output
24	P36	Port 3, Pin 6	Output
25	P30	Port 3, Pin 0	Input
26-27	P00-P01	Port 0, Pins 0,1	Input/Output
28-29	P10-P11	Port 1, Pins 0,1	Input/Output
30	P02	Port 0, Pin 2	Input/Output
31	GND	Ground	
32-33	P12-P13	Port 1, Pins 2,3	Input/Output
34	P03	Port 0, Pin 3	Input/Output
35-39	P20-P24	Port 2, Pins 0, 1,2,3,4	Input/Output
40	DS	Data Strobe	Output

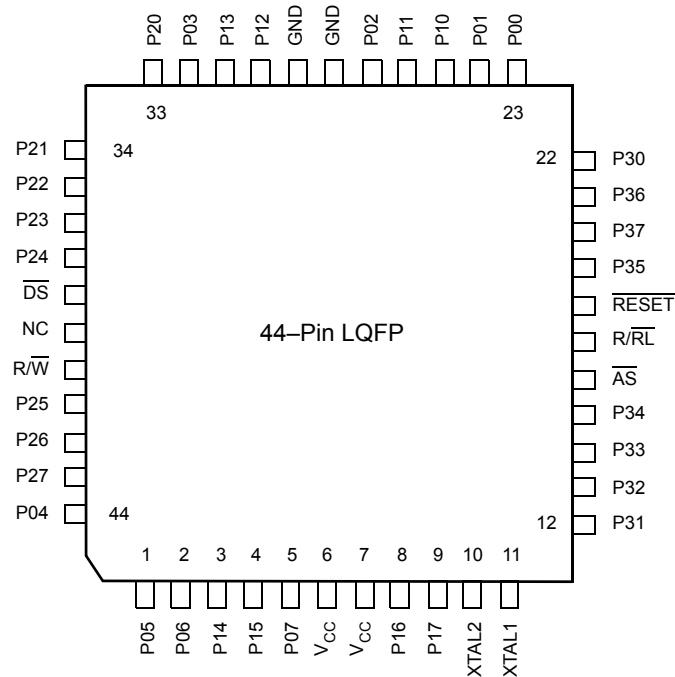


Figure 5. 44-Pin LQFP Pin Configuration Standard Mode

Table 4. 44-Pin LQFP Pin Identification

Pin No	Symbol	Function	Direction
1-2	P05-P06	Port 0, Pins 5,6	Input/Output
3-4	P14-P15	Port 1, Pins 4,5	Input/Output
5	P07	Port 0, Pin 7	Input/Output
6-7	V _{CC}	Power Supply	
8-9	P16-P17	Port 1, Pins 6,7	Input/Output
10	XTAL2	Crystal Oscillator	Output
11	XTAL1	Crystal Oscillator	Input
12-14	P31-P33	Port 3, Pins 1,2,3	Input
15	P34	Port 3, Pin 4	Output
16	AS	Address Strobe	Output
17	R//RL	ROM/ROMless select	Input

Table 4. 44-Pin LQFP Pin Identification (Continued)

Pin No	Symbol	Function	Direction
18	RESET	Reset	Input
19	P35	Port 3, Pin 5	Output
20	P37	Port 3, Pin 7	Output
21	P36	Port 3, Pin 6	Output
22	P30	Port 3, Pin 0	Input
23-24	P00-P01	Port 0, Pin 0,1	Input/Output
25-26	P10-P11	Port 1, Pins 0,1	Input/Output
27	P02	Port 0, Pin 2	Input/Output
28-29	GND	Ground	
30-31	P12-P13	Port 1, Pins 2,3	Input/Output
32	P03	Port 0, Pin 3	Input/Output
33-37	P20-24	Port 2, Pins 0,1,2,3,4	Input/Output
38	DS	Data Strobe	Output
39	NC	No Connection	
40	$\overline{R/W}$	Read/Write	Output
41-43	P25-P27	Port 2, Pins 5,6,7	Input/Output
44	P04	Port 0, Pin 4	Input/Output

Table 11. DC Electrical Characteristics $T_A = 0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$ (Continued)

Symbol	Parameter	V_{CC}^1	Min	Max	Typical @ 25 $^{\circ}\text{C}$	Units	Conditions	Notes
T_{POR}	Power-On Reset	3.5V	2.0 ms	24	7	ms		
		5.5V	1.0 ms	13	4	ms		
V_{LV}	Auto Reset Voltage		2.3	3.0	2.8	V		11,12

Notes

1. The V_{CC} voltage specification of 5.5 V guarantees $5.0\text{ V} \pm 0.5\text{ V}$ and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V
2. STD Mode (not Low EMI Mode)
3. Z86E43/743/E44 only.
4. For analog comparator inputs when analog comparators are enabled
5. All outputs unloaded, I/O pins floating, inputs at rail.
6. $CL1=CL2=22\text{ pF}$.
7. Same as note 5 except inputs at V_{CC}
8. Clock must be forced Low, when XTAL1 is clock driven and XTAL2
9. WDT running
10. Auto Latch (mask option) selected.
11. Device does function down to the Auto Reset voltage
12. Max. temperature is $70\text{ }^{\circ}\text{C}$

Table 12. DC Electrical Characteristics $T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$

Symbol	Parameter	V_{CC}^1	Min	Max	Typical @ 25 $^{\circ}\text{C}$	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	4.5V	$0.7 V_{CC}$	$V_{CC} + 0.3$	2.5	V	Driven by External Clock Generator	
		5.5V	$0.7 V_{CC}$	$V_{CC} + 0.3$	2.5	V		
V_{CL}	Clock Input Low Voltage	4.5V	$\text{GND} - 0.3$	$0.2 V_{CC}$	1.5	V	Driven by External Clock Generator	
		5.5V	$\text{GND} - 0.3$	$0.2 V_{CC}$	1.5	V		
V_{IH}	Input High Voltage	4.5V	$0.7 V_{CC}$	$V_{CC} + 0.3$	2.5	V		
		5.5V	$0.7 V_{CC}$	$V_{CC} + 0.3$	2.5	V		
V_{IL}	Input Low Voltage	4.5V	$\text{GND} - 0.3$	$0.2 V_{CC}$	1.5	V		
		5.5V	$\text{GND} - 0.3$	$0.2 V_{CC}$	1.5	V		
V_{OH}	Output High Voltage Low EMI Mode	4.5V	$V_{CC} - 0.4$		4.8		$I_{OH} = -0.5\text{ mA}$	2
		5.5V	$V_{CC} - 0.4$		4.8		$I_{OH} = -0.5\text{ mA}$	2

Table 13. DC Electrical Characteristics $T_A = 0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$, 12 MHz (Continued)

No.	Symbol	Parameter	V_{CC}^1	Min	Max	Units	Notes
4	TwAS	$\overline{AS}$ Low Width	3.5V	55		ns	2
			5.5V	55		ns	2
5	TdAS(DS)	Address Float to $\overline{DS}$ Fall	3.5V	0		ns	
			5.5V	0		ns	
6	TwDSR	$\overline{DS}$ (Read) Low Width	3.5V	200		ns	2,3
			5.5V	200		ns	2,3
7	TwDSW	$\overline{DS}$ (Write) Low Width	3.5V	110		ns	2,3
			5.5V	110		ns	2,3
8	TdDSR(DR)	$\overline{DS}$ Fail to Read Data Req'd Valid	3.5V		150	ns	2,3
			5.5V		150	ns	2,3
9	ThDR(DS)	Read Data to $\overline{DS}$ Rise Hold Time	3.5V	0		ns	2
			5.5V	0		ns	2
10	TdDS(A)	$\overline{DS}$ Rise to Address Active Delay	3.5V	45		ns	2
			5.5V	55		ns	2
11	TdDS(AS)	$\overline{DS}$ Rise to $\overline{AS}$ Fall Delay	3.5V	30		ns	2
			5.5V	45		ns	2
12	TdR/W(AS)	$R/\overline{W}$ Valid to $\overline{AS}$ Rise Delay	3.5V	45		ns	2
			5.5V	45		ns	2
13	TdDS(R/W)	$\overline{DS}$ Rise to $R/\overline{W}$ Not Valid	3.5V	45		ns	2
			5.5V	45		ns	2
14	TdDW(DSW)	Write Data Valid to $\overline{DS}$ Fall (Write) Delay	3.5V	55		ns	2
			5.5V	55		ns	2
15	TdDS(DW)	$\overline{DS}$ Rise to Write Data Not Valid Delay	3.5V	45		ns	2
			5.5V	55		ns	2
16	TdA(DR)	Address Valid to Read Data Req'd Valid	3.5V		310	ns	2,3
			5.5V		310	ns	2,3
17	TdAS(DS)	$\overline{AS}$ Rise to $\overline{DS}$ Fall Delay	3.5V	65		ns	2
			5.5V	65		ns	2

Table 13. DC Electrical Characteristics $T_A = 0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$, 12 MHz (Continued)

No.	Symbol	Parameter	V_{CC}^1	Min	Max	Units	Notes
18	TdDM(AS)	$\overline{\text{DM}}$ Valid to $\overline{\text{AS}}$ Rise Delay	3.5V	35		ns	2
			5.5V	35		ns	2
19	ThDS(AS)	$\overline{\text{DS}}$ Valid to Address Valid Hold Time	3.5V	35		ns	2
			5.5V	35		ns	2

Notes

1. The V_{CC} voltage specification of 5.5 V guarantees $5.0\text{ V} \pm 0.5\text{ V}$ and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V.
2. Timing numbers given are for minimum T_{pC} .
3. When using extended memory timing, add 2 T_{pC}

Standard Test Load

All timing references use $0.7\text{ }V_{CC}$ for a logic 1 and $0.2\text{ }V_{CC}$ for a logic 0.

For Standard Mode (not Low-EMI Mode for outputs) with SMR, D1 = 0, D0 = 0.

Table 14. DC Electrical Characteristics $T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$, 12 MHz

No.	Symbol	Parameter	V_{CC}^1	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to $\overline{\text{AS}}$ Rise Delay	4.5V	35		ns	2
			5.5V	35		ns	2
2	TdAS(A)	$\overline{\text{AS}}$ Rise to Address Float Delay	4.5V	45		ns	2
			5.5V	45		ns	2
3	TdAS(DR)	$\overline{\text{AS}}$ Rise to Read Data Req'd Valid	4.5V		250	ns	2,3
			5.5V		250	ns	2,3
4	TwAS	$\overline{\text{AS}}$ Low Width	4.5V	55		ns	2
			5.5V	55		ns	2
5	TdAS(DS)	Address Float to $\overline{\text{DS}}$ Fall	4.5V	0		ns	
			5.5V	0		ns	
6	TwDSR	$\overline{\text{DS}}$ (Read) Low Width	4.5V	200		ns	2,3
			5.5V	200		ns	2,3
7	TwDSW	$\overline{\text{DS}}$ (Write) Low Width	4.5V	110		ns	2,3
			5.5V	110		ns	2,3
8	TdDSR(DR)	$\overline{\text{DS}}$ Fail to Read Data Req'd Valid	4.5V		150	ns	2,3
			5.5V		150	ns	2,3
9	ThDR(DS)	Read Data to $\overline{\text{DS}}$ Rise Hold Time	4.5V	0		ns	2
			5.5V	0		ns	2

Table 14. DC Electrical Characteristics $T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$, 12 MHz (Continued)

No.	Symbol	Parameter	V_{CC}^1	Min	Max	Units	Notes
10	TdDS(A)	$\overline{DS}$ Rise to Address Active Delay	4.5V	45		ns	2
			5.5V	55		ns	2
11	TdDS(AS)	$\overline{DS}$ Rise to $\overline{AS}$ Fall Delay	4.5V	45		ns	2
			5.5V	45		ns	2
12	TdR/W(AS)	$\overline{R/W}$ Valid to $\overline{AS}$ Rise Delay	4.5V	45		ns	2
			5.5V	45		ns	2
13	TdDS(R/W)	$\overline{DS}$ Rise to $\overline{R/W}$ Not Valid	4.5V	45		ns	2
			5.5V	45		ns	2
14	TdDW(DSW)	Write Data Valid to $\overline{DS}$ Fall (Write) Delay	4.5V	55		ns	2
			5.5V	55		ns	2
15	TdDS(DW)	$\overline{DS}$ Rise to Write Data Not Valid Delay	4.5V	55		ns	2
			5.5V	55		ns	2
16	TdA(DR)	Address Valid to Read Data Req'd Valid	4.5V		310	ns	2,3
			5.5V		310	ns	2,3
17	TdAS(DS)	$\overline{AS}$ Rise to $\overline{DS}$ Fall Delay	4.5V	65		ns	2
			5.5V	65		ns	2
18	TdDM(AS)	$\overline{DM}$ Valid to $\overline{AS}$ Rise Delay	4.5V	35		ns	2
			5.5V	35		ns	2
19	ThDS(AS)	$\overline{DS}$ Valid to Address Valid Hold Time	4.5V	35		ns	2
			5.5V	35		ns	2

Notes

1. The V_{CC} voltage specification of 5.5 V guarantees $5.0\text{ V} \pm 0.5\text{ V}$ and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V.
2. Timing numbers given are for minimum T_{pC} .
3. When using extended memory timing, add 2 T_{pC} .

Standard Test Load

All timing references use $0.7\text{ }V_{CC}$ for a logic 1 and $0.2\text{ }V_{CC}$ for a logic 0.

For Standard Mode (not Low-EMI Mode for outputs) with SMR, $D1 = 0$, $D0 = 0$.

Handshake Timing Diagrams

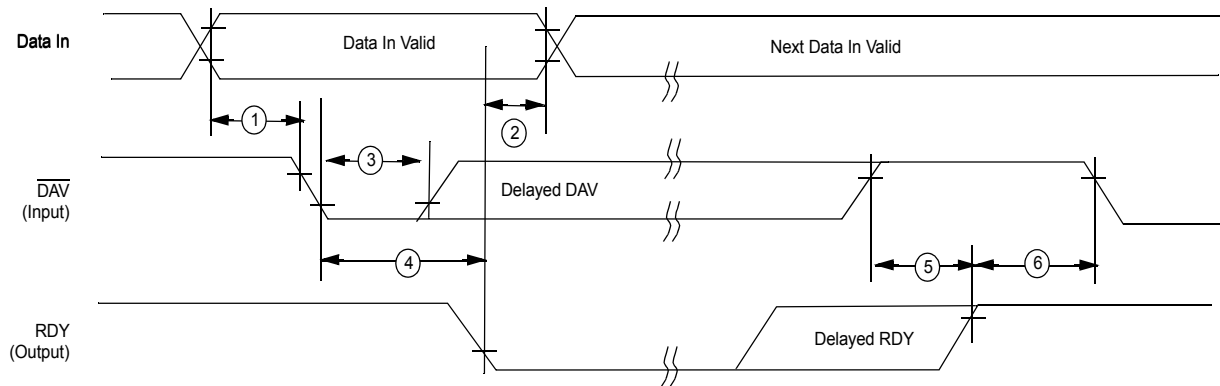


Figure 16. Input Handshake Timing

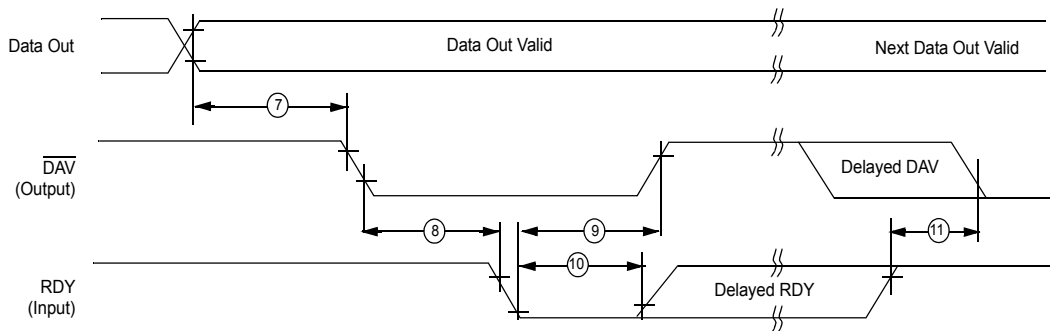


Figure 17. Output Handshake Timing

Table 17. Additional Timing Table (Divide by Two Mode) $T_A = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}$

No	Symbol	Parameter	V_{CC}^1	Min	Max	Min	Max	Units	Conditions	Notes
1	TpC	Input Clock Period	3.5V	62.5	DC	250	DC	ns		2,6,4
			5.5V	62.5	DC	250	DC	ns		2,6,4
2	TrC,TfC	Clock Input Rise & Fall Times	3.5V		15		25	ns		2,6,4
			5.5V		15		25	ns		2,6,4
3	TwC	Input Clock Width	3.5V	31		31		ns		2,6,4
			5.5V	31		31		ns		2,6,4

Table 18. Additional Timing Table (Divide by Two Mode) $T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$

No	Symbol	Parameter	V_{CC}^1	Min	Max	Min	Max	Units	Conditions	Notes
1	TpC	Input Clock Period	3.5V	62.5	DC	250	DC	ns		2,6,4
			5.5V	62.5	DC	250	DC	ns		2,6,4
2	TrC,TfC	Clock Input Rise & Fall Times	3.5V		15		25	ns		2,6,4
			5.5V		15		25	ns		2,6,4
3	TwC	Input Clock Width	3.5V	31		31		ns		2,6,4
			5.5V	31		31		ns		2,6,4
4	TwTinL	Timer Input Low Width	3.5V	70		70		ns		2,6,4
			5.5V	70		70		ns		2,6,4
5	TwTinH	Timer Input High Width	3.5V	5TpC		5TpC				2,6,4
			5.5V	5TpC		5TpC				2,6,4
6	TpTin	Timer Input Period	3.5V	8TpC		8TpC				2,6,4
			5.5V	8TpC		8TpC				2,6,4
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.5V		100		100	ns		2,6,4
			5.5V		100		100	ns		2,6,4
8A	TwIL	Int. Request Low Time	3.5V	70		70		ns		2,6,4,5
			5.5V	70		70		ns		2,6,4,5
8B	TwIL	Int. Request Low Time	3.5V	5TpC		5TpC				2,6,4,5
			5.5V	5TpC		5TpC				2,6,4,5
9	TwIH	Int. Request Input High Time	3.5V	5TpC		5TpC				2,6,4,5
			5.5V	5TpC		5TpC				2,6,4,5
10	Twsm	Stop Mode Recovery Width Spec	3.5V	12		12		ns		6,7
			5.5V	12		12		ns		6,7
11	Tost	Oscillator Startup Time	3.5V		5TpC		5TpC			6,7
			5.5V		5TpC		5TpC			6,7

Table 18. Additional Timing Table (Divide by Two Mode) $T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$ (Continued)

No	Symbol	Parameter	V_{CC}^1	Min	Max	Min	Max	Units	Conditions	Notes
12	Twdt	Watchdog Timer Delay Time Before Timeout	3.5V	7		10		ms	D0 = 0	8,9
			5.5V	3.5		5		ms	D1 = 0	5,11
			3.5V	14		20		ms	D0 = 1	5,11
			5.5V	7		10		ms	D1 = 0	5,11
			3.5V	28		40		ms	D1 = 0	5,11
			5.5V	14		20		ms	D1 = 1	5,11
			3.5V	112		160		ms	D0 = 1	5,11
			5.5V	56		80		ms	D1 = 1	5,11

Notes

1. The V_{CC} voltage specification of 5.5 V guarantees $5.0\text{ V} \pm 0.5\text{ V}$ and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V.
2. Timing Reference uses 0.7 VC0 for a logic 1 and 0.2 VGC for a logic 0.
3. SMR D1 = 0.
4. SMR-D5 = 1, POR STOP Mode Delay is on
5. Interrupt request via Port 3 (P31-P33)
6. Interrupt request via Port 3 (P30).
7. Maximum frequency for internal system clock is 2 MHz when using Low EMI OSC PCON Bit D7 = 0
8. Reg. WDTMR.
9. Using internal RC.

Pin Functions

EPROM Programming Mode

D7-D0 Data Bus. The data can be read from or written to external memory through the data bus.

V_{CC} Power Supply. This pin must supply 5 V during the EPROM read mode and 6 V during other modes.

$\overline{CE}$ Chip Enable (active Low). This pin is active during EPROM Read Mode, Program Mode, and Program Verify Mode.

$\overline{OE}$ Output Enable (active Low). This pin drives the direction of the Data Bus. When this pin is Low, the Data Bus is output, when High, the Data Bus is input.

EPM EPROM Program Mode. This pin controls the different EPROM Program Mode by applying different voltages.

V_{PP} Program Voltage. This pin supplies the program voltage.

PGM Program Mode (active Low). When this pin is Low, the data is programmed to the EPROM through the Data Bus.

Functional Description

The MCU incorporates the following special functions to enhance the standard Z8 architecture to provide the user with increased design flexibility.

RESET. The device is reset in one of three ways:

1. Power-On Reset
2. Watchdog Timer
3. Stop Mode Recovery Source

► **Note:** *Having the Auto Power-On Reset circuitry built-in, the MCU does not need to be connected to an external power-on reset circuit. The reset time is T_{POR} . The MCU does not re-initialize WDTMR, SMR, P2M, and P3M registers to their reset values on a Stop Mode Recovery operation.*

► **Note:** *The device V_{CC} must rise up to the operating V_{CC} specification before the T_{POR} expires.*

Program Memory. The MCU can address up to 4/8/16 KB of Internal Program Memory (see [Figure 22](#)). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For EPROM mode, byte 12 (000Ch) to address 4095 (0FFFh)/8191 (1FFFh)/16384 (3FFFh), consists of programmable EPROM. After reset, the program counter points at the address 000Ch, which is the starting address of the user program.

In ROMless mode, the Z86E43/743/E44 can address up to 64 KB of External Program Memory. The ROM/ROMless option is only available on the 44-pin devices.

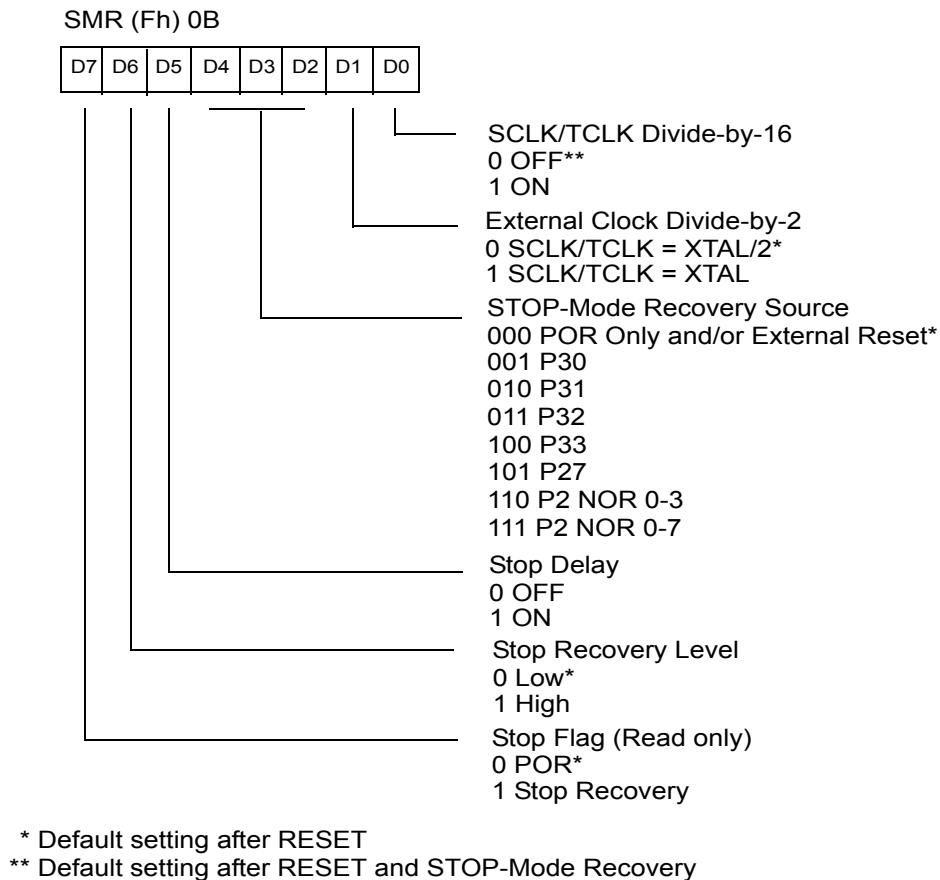


Figure 31. Stop Mode Recovery Register (Write-Only Except Bit D7, Which Is Read-Only)

SCLK/TCLK Divide-by-16 Select (D0). This bit of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources counter/timers and interrupt logic).

External Clock Divide-by-Two (D1). This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, the System Clock (SCLK) and Timer Clock (TCLK) are equal to the external clock frequency divided by two. The SCLK/TCLK is equal to the external clock frequency when this bit is set (D1=1). Using this bit together with D7 of PCON further helps lower EMI (that is, D7 (PCON) = 0, D1 (SMR) = 1). The default setting is zero.

Stop Mode Recovery Source (D2, D3, and D4). These three bits of the SMR register specify the wake up source of the Stop Mode Recovery (Figure 32). Table 22 shows the SMR source selected with the setting of D2 to D4. P33-P31 cannot be used to wake up

from STOP mode when programmed as analog inputs. When the Stop Mode Recovery sources are selected in this register then SMR2 register bits D0, D1 must be set to zero.

► **Note:** *If the Port 2 pin is configured as an output, this output level will be read by the SMR circuitry.*

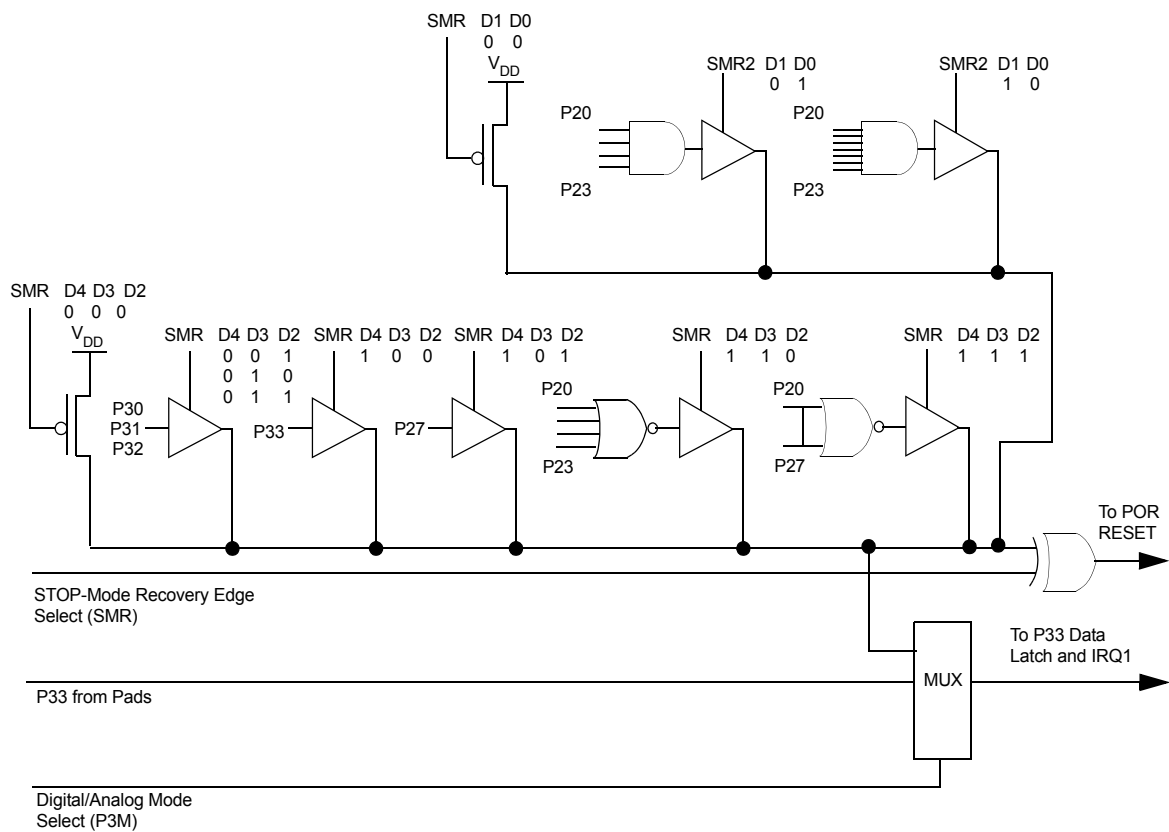


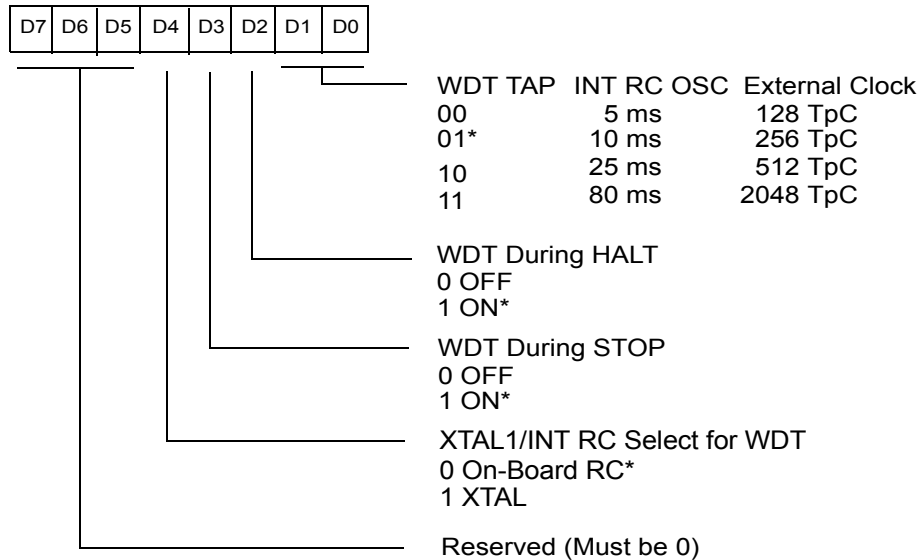
Figure 32. Stop Mode Recovery Source

► **Note:** *WDT time-out in STOP Mode will not reset SMR, SMR2, PCON, WDTMR, P2M, P3M, Ports 2 & 3 Data Registers, but will activate the T_{POR} delay.*

WDTMR Register Accessibility. The WDTMR register is accessible only during the first 60 internal system clock cycles from the execution of the first instruction after Power-On Reset, Watchdog reset or a Stop Mode Recovery (Figure 33 and Figure 34). After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register File at address location 0Fh.

Clock Free WDT Reset. The WDT will enable the Z8 to reset the I/O pins whenever the WDT times out, even without a clock source running on the XTAL1 and XTAL2 pins. WDTMR Bit D4 must be 0 for the clock Free WDT to work. The I/O pins will default to their default settings.

WDTMR (F) 0F



* Default setting after RESET

Figure 33. Watchdog Timer Mode Register Write Only

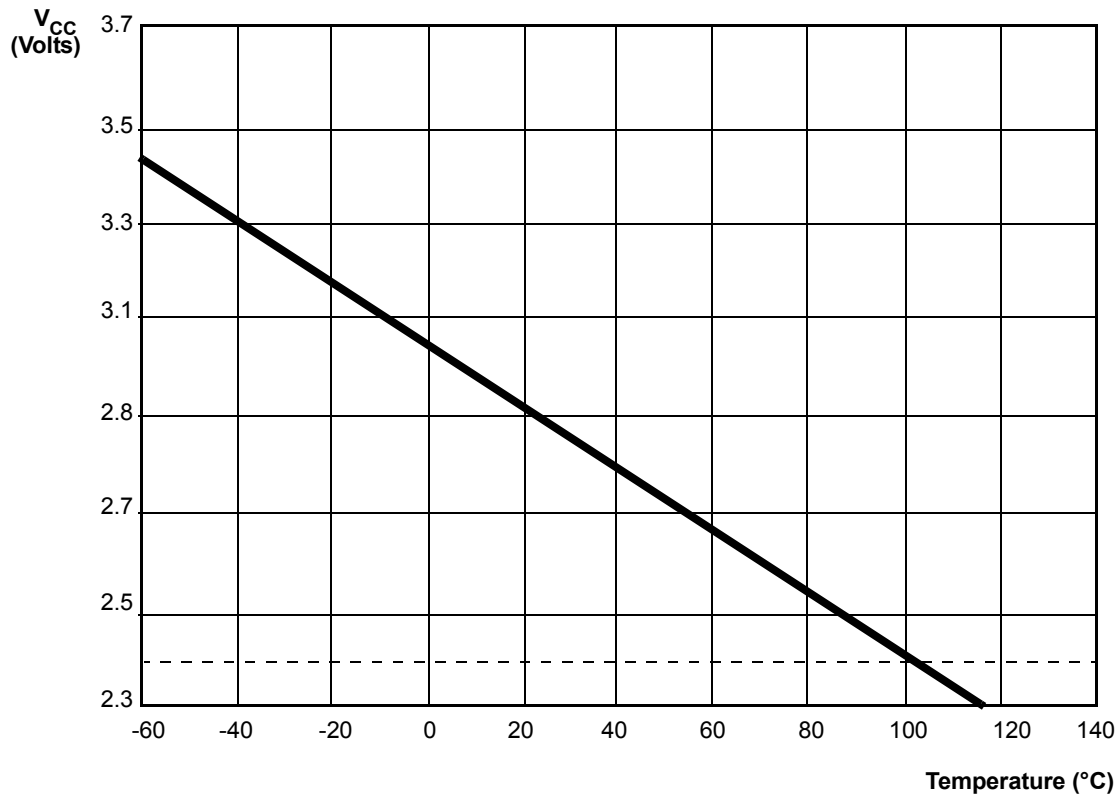


Figure 35. Typical V_{LV} Voltage vs. Temperature

Z8 Control Register Diagrams

Ordering Information

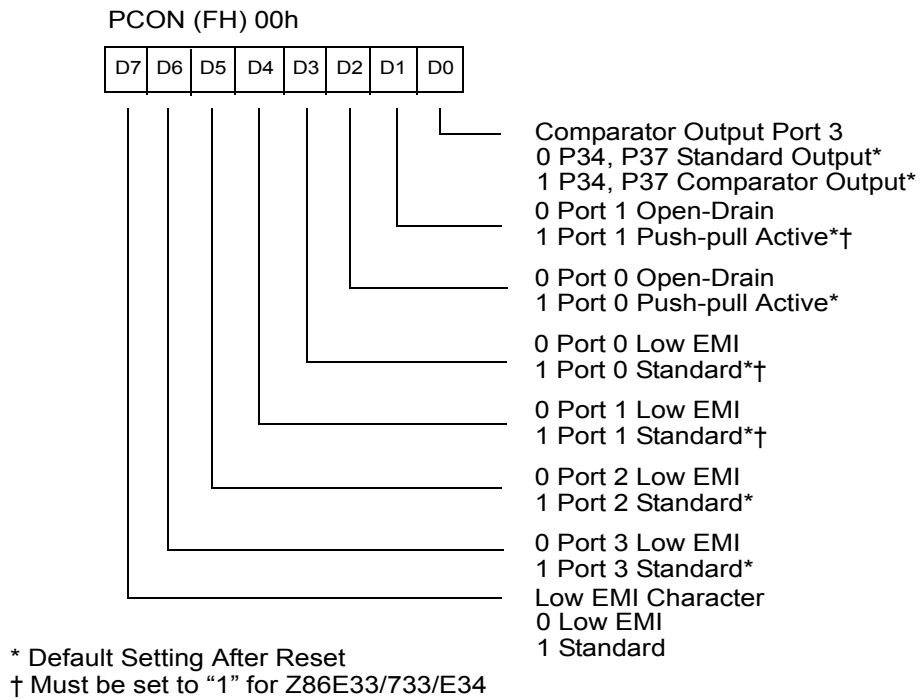
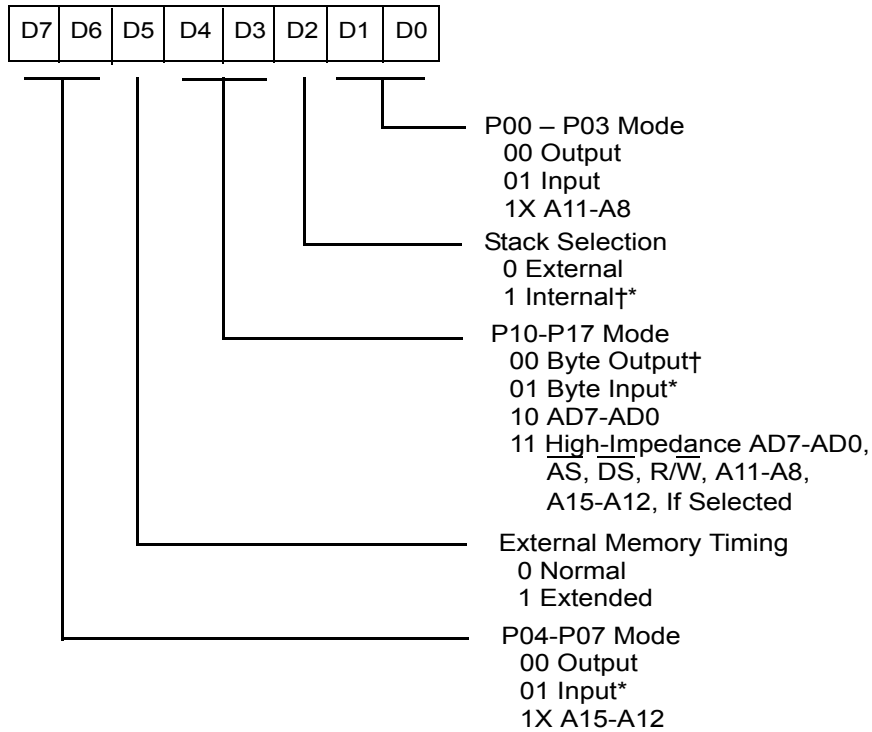


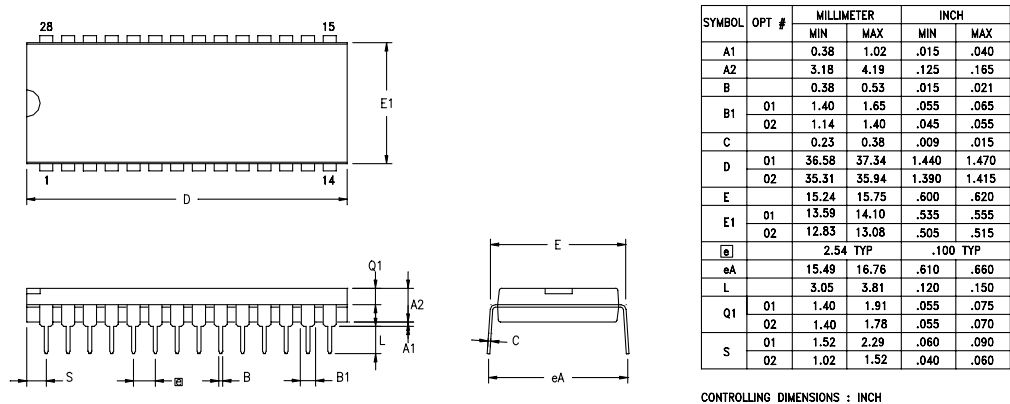
Figure 36. Port Configuration Register (PCON) (Write Only)

R248 P01M



Reset Condition = 0100 1101B
 For ROMless Condition = 1011 0110B
 † Z86E33/733/E34 Must be 00
 * Default after Reset

Figure 48. Port 0 and 1 Mode Register (F8_h: Write Only)



OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

Figure 58. 28-Pin DIP Package Diagram

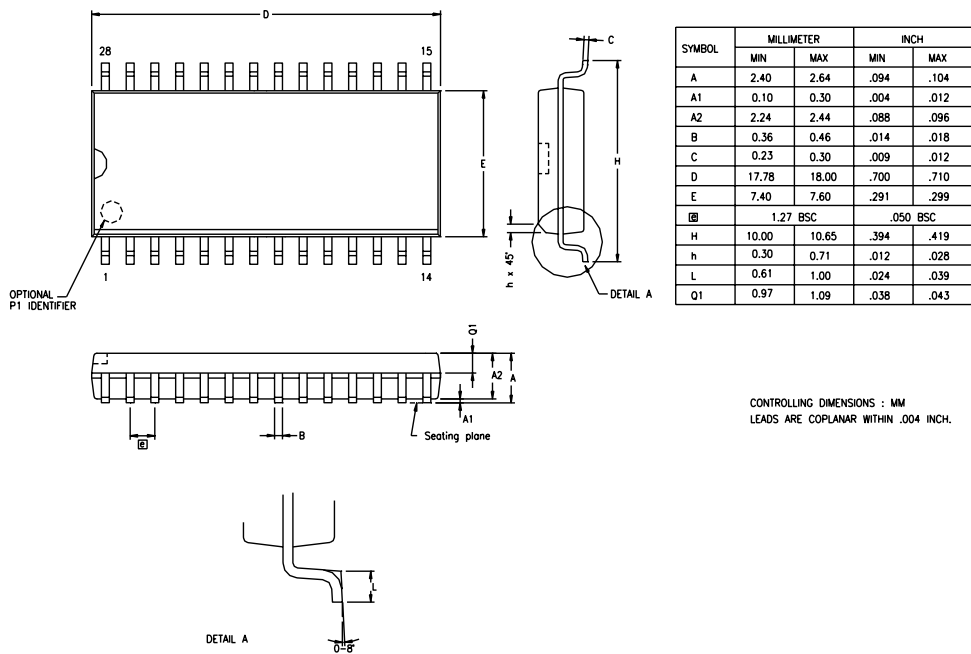


Figure 59. 28-Pin SOIC Package Diagram