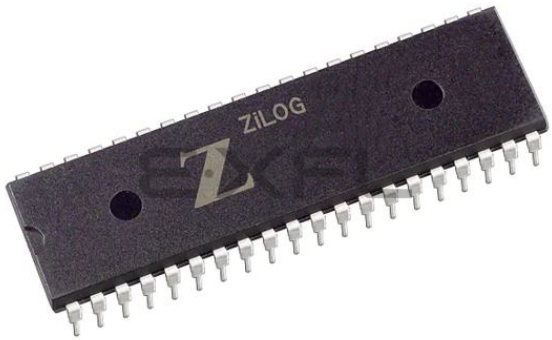

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	EBI/EMI
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.620", 15.75mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e4312psc

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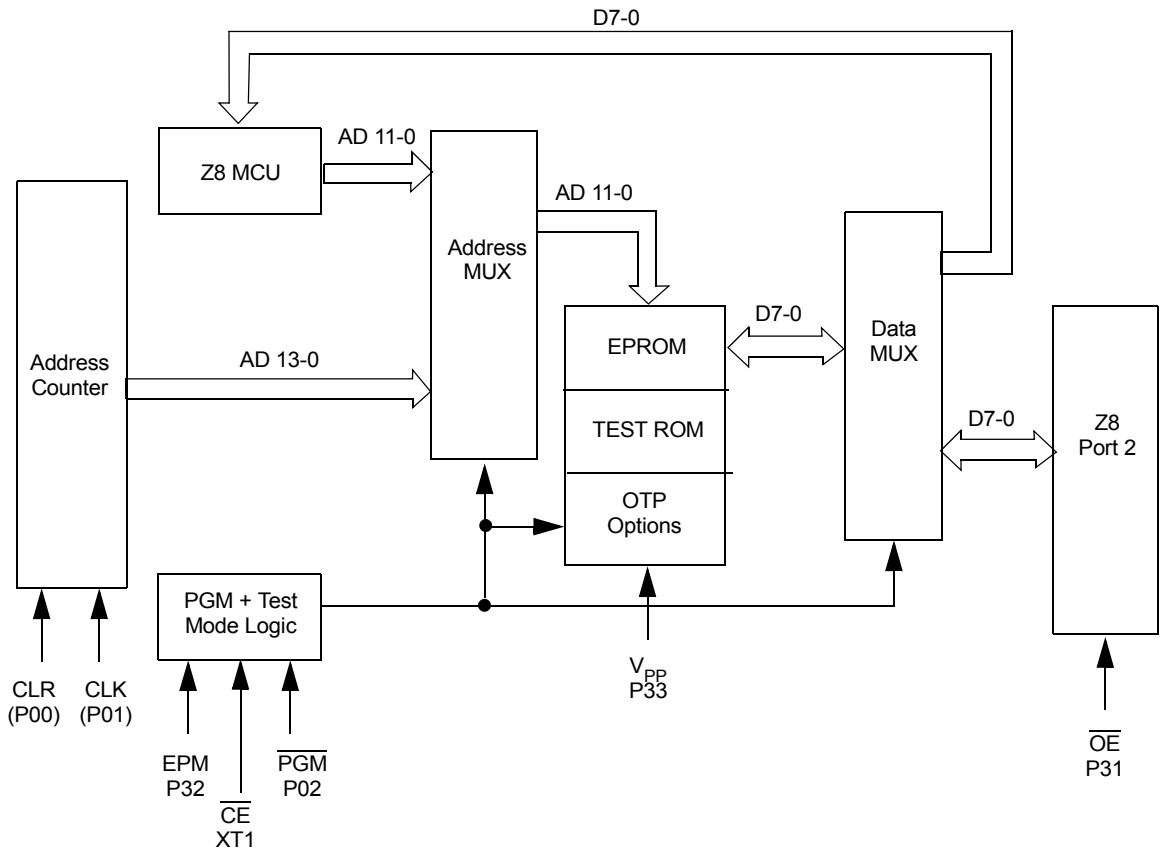


Figure 2. EPROM Programming Block Diagram

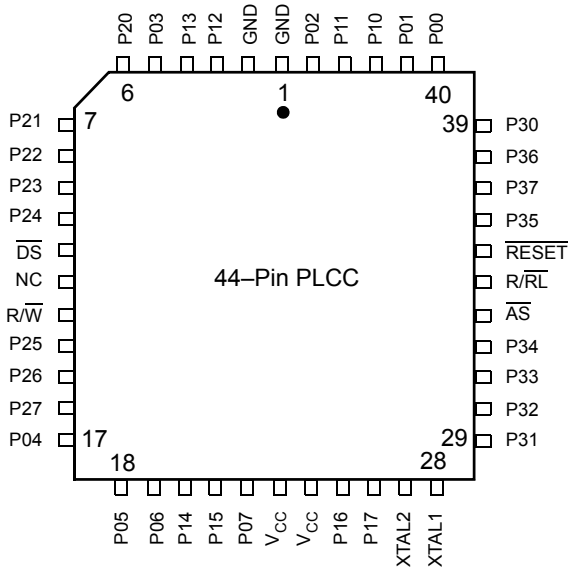


Figure 4. 44-Pin PLCC Pin Configuration Standard Mode

Table 3. 44-Pin PLCC Pin Identification

Pin No	Symbol	Function	Direction
1-2	GND	Ground	
3-4	P12-P13	Port 1, Pins 2,3	Input/Output
5	P03	Port 0, Pin 3	Input/Output
6-10	P20-P24	Port 2, Pins 0,1,2,3,4	Input/Output
11	DS	Data Strobe	Output
12	NC	No Connection	
13	R/$\overline{W}$	Read/Write	Output
14-16	P25-P27	Port 2, Pins 5,6,7	Input/Output
17-19	P04-P06	Port 0, Pins 4,5,6	Input/Output
20-21	P14-P15	Port 1, Pins 4,5	Input/Output
22	P07	Port 0, Pin 7	Input/Output
23-24	V_{CC}	Power Supply	
25-26	P16-P17	Port 1, Pins 6,7	Input/Output

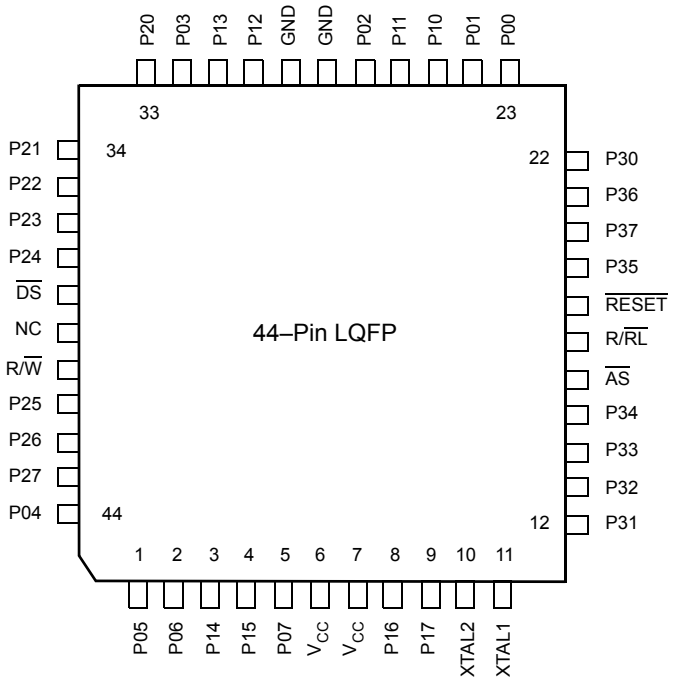


Figure 5. 44-Pin LQFP Pin Configuration Standard Mode

Table 4. 44-Pin LQFP Pin Identification

Pin No	Symbol	Function	Direction
1-2	P05-P06	Port 0, Pins 5,6	Input/Output
3-4	P14-P15	Port 1, Pins 4,5	Input/Output
5	P07	Port 0, Pin 7	Input/Output
6-7	V_{CC}	Power Supply	
8-9	P16-P17	Port 1, Pins 6,7	Input/Output
10	XTAL2	Crystal Oscillator	Output
11	XTAL1	Crystal Oscillator	Input
12-14	P31-P33	Port 3, Pins 1,2,3	Input
15	P34	Port 3, Pin 4	Output
16	AS	Address Strobe	Output
17	R//RL	ROM/ROMless select	Input

Table 5. 40-Pin DIP Package Pin Identification EPROM Mode (Continued)

Pin No	Symbol	Function	Direction
30	/PGM	Prog. Mode	Input
31	GND	Ground	
32-34	NC	No Connection	
35-39	D0-D4	Data 0,1,2,3,4	Input/Output
40	NC	No Connection	

Table 7. 44-Pin LQFP Pin Identification EPROM Programming Mode (Continued)

Pin No	Symbol	Function	Direction
33-37	D0-D4	Data 0,1,2,3,4	Input/Output
38-40	NC	No Connection	
41-43	D5-D7	Data 5,6,7	Input/Output
44	NC	No Connection	

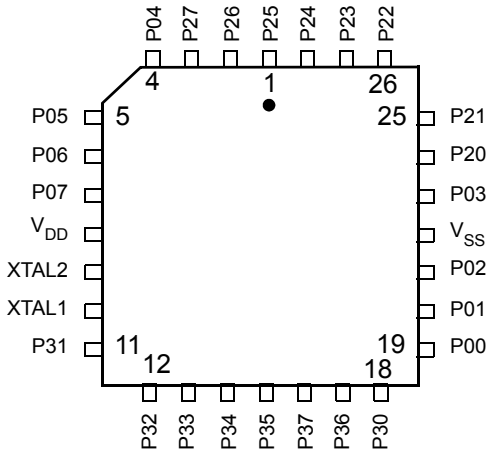


Figure 10. Standard Mode 28-Pin PLCC Pin Configuration

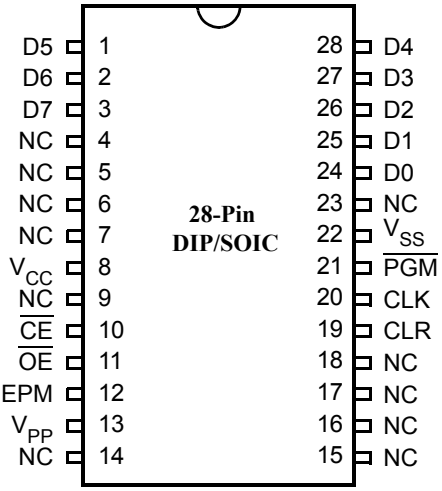


Figure 11. EPROM Programming Mode 28-Pin DIP/SOIC Pin Configuration

Total power dissipation should not exceed 1.21 W for the package. Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{DD} \times [I_{DD} - (\text{sum of } I_{OH}), + \text{sum of } [(V_{DD} - V_{OH}) \times I_{OH}] + \text{sum of } (V_{OL} \times I_{OL})$$

Standard Test Conditions

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Test Load).

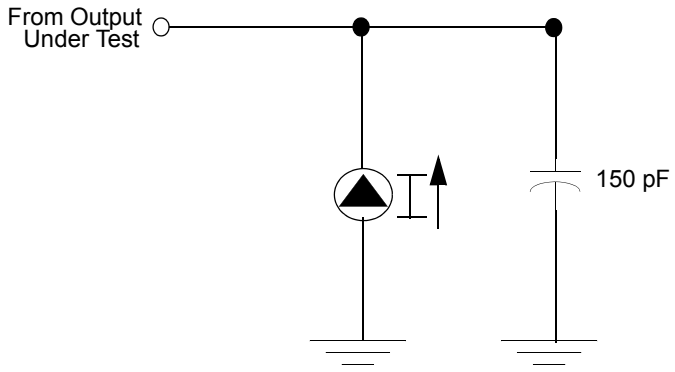


Figure 13. Test Load Diagram

Capacitance

T_A = 25 °C, V_{CC} = GND = 0 V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

Table 18. Additional Timing Table (Divide by Two Mode) T_A = -40 °C to +105 °C (Continued)

No	Symbol	Parameter	V_{CC} [1]	Min	Max	Min	Max	Units	Conditions	Notes
12	Twdt	Watchdog Timer Delay Time Before Timeout	3.5V	7		10		ms	D0 =0	8,9
			5.5V	3.5		5		ms	D1 = 0	5,11
			3.5V	14		20		ms	D0 =1	5,11
			5.5V	7		10		ms	D1 = 0	5,11
			3.5V	28		40		ms	D1 = 0	5,11
			5.5V	14		20		ms	D1 = 1	5,11
			3.5V	112		160		ms	D0 = 1	5,11
			5.5V	56		80		ms	D1 = 1	5,11

Notes
1. The V_{CC} voltage specification of 5.5 V guarantees 5.0 V ± 0.5 V and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V.
2. Timing Reference uses 0.7 VC0 for a logic 1 and 0.2 VGC for a logic 0.
3. SMR D1 = 0.
4. SMR-D5 = 1, POR STOP Mode Delay is on
5. Interrupt request via Port 3 (P31-P33)
6. Interrupt request via Port 3 (P30).
7. Maximum frequency for internal system clock is 2 MHz when using Low EMI OSC PCON Bit D7 = 0
8. Reg. WDTMR.
9. Using internal RC.

Pin Functions

EPROM Programming Mode

D7-D0 Data Bus. The data can be read from or written to external memory through the data bus.

V_{CC} Power Supply. This pin must supply 5 V during the EPROM read mode and 6 V during other modes.

$\overline{CE}$ Chip Enable (active Low). This pin is active during EPROM Read Mode, Program Mode, and Program Verify Mode.

$\overline{OE}$ Output Enable (active Low). This pin drives the direction of the Data Bus. When this pin is Low, the Data Bus is output, when High, the Data Bus is input.

EPM EPROM Program Mode. This pin controls the different EPROM Program Mode by applying different voltages.

V_{PP} Program Voltage. This pin supplies the program voltage.

PGM Program Mode (active Low). When this pin is Low, the data is programmed to the EPROM through the Data Bus.

The Z86E43/743/E44 does not reset WDTMR, SMR, P2M, and P3M registers on a Stop-Mode Recovery operation.

$\overline{\text{ROMless}}$ (input, active Low). This pin, when connected to GND, disables the internal ROM and forces the device to function as a Z86C90/C89 ROMless Z8. (Note that, when left unconnected or pulled High to V_{CC}, the device functions nor

Note: *When using in ROM Mode in High EMI (noisy) environment, the ROMless pins should be connected directly to V_{CC}.*

$\overline{\text{DS}}$ (output, active Low). Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of $\overline{\text{DS}}$. For WRITE operations, the falling edge of $\overline{\text{DS}}$ indicates that output data is valid.

$\overline{\text{AS}}$ (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle for external memory transfer. Address output is from Port 0/Port 1 for all external programs. Memory address transfers are valid at the trailing edge of $\overline{\text{AS}}$. Under program control, $\overline{\text{AS}}$ is placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

Port 0 (P07-P00). Port 0 is an 8-bit, bidirectional, CMOS-compatible I/0 port. These eight I/O lines can be configured under software control as a nibble I/0 port, or as an address port for interfacing external memory. The input buffers are Schmitt-triggered and nibble programmed. Either nibble output that can be globally programmed as push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 0 can be placed under handshake control. In Handshake Mode, Port 3 lines P32 and P35 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to Port 0's upper nibble. The lower nibble must have the same direction as the upper nibble.

For external memory references, Port 0 provides address bits A11-A8 (lower nibble) or Al 5-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. In ROMless mode, after a hardware reset, Port 0 is configured as address lines Al 5-A8, and extended timing is set to accommodate slow memory access. The initialization routine can include re-configuration to eliminate this extended timing mode. In ROM mode, Port 0 is defined as input after reset.

Port 0 can be set in the High-Impedance Mode if selected as an address output state, along with Port 1 and the control signals $\overline{\text{AS}}$, $\overline{\text{DS}}$, and R/$\overline{\text{W}}$ (Figure 18).

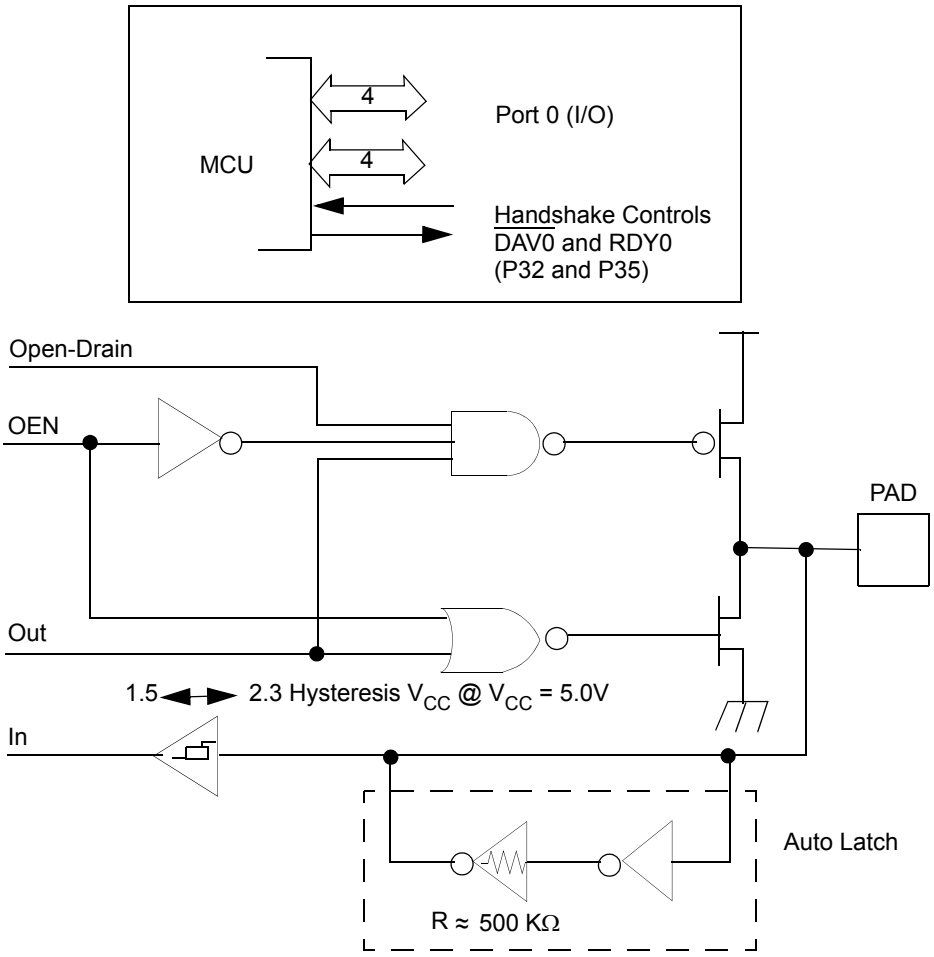


Figure 18. Port 0 Configuration

Port 1 (P17-P10). Port 1 is an 8-bit, bidirectional, CMOS-compatible port with multiplexed Address (A7-A0) and Data (D7-D0) ports. These eight I/O lines can be programmed as inputs or outputs or can be configured under software control as an Address/Data port for interfacing external memory. The input buffers are Schmitt-triggered and the output buffers can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 1 can be placed under handshake control. In this configuration, Port 3, lines P33 and P34 are used as the handshake controls RDY1 and $\overline{\text{DAV1}}$ (Ready and Data Available). To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 outputs the additional lines (see Figure 19).

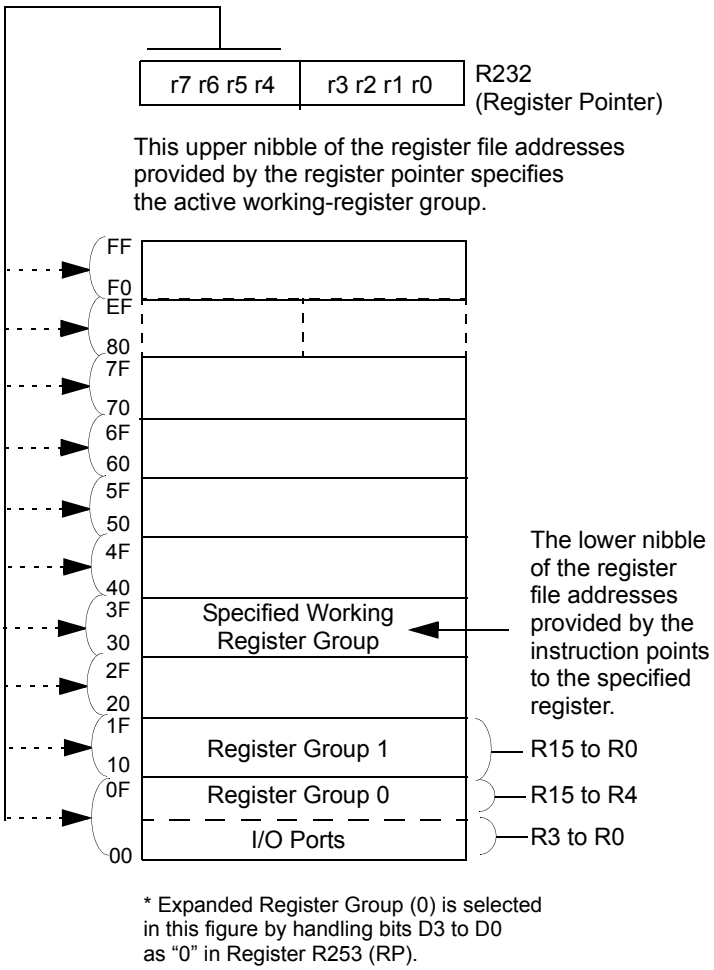


Figure 25. Register Pointer

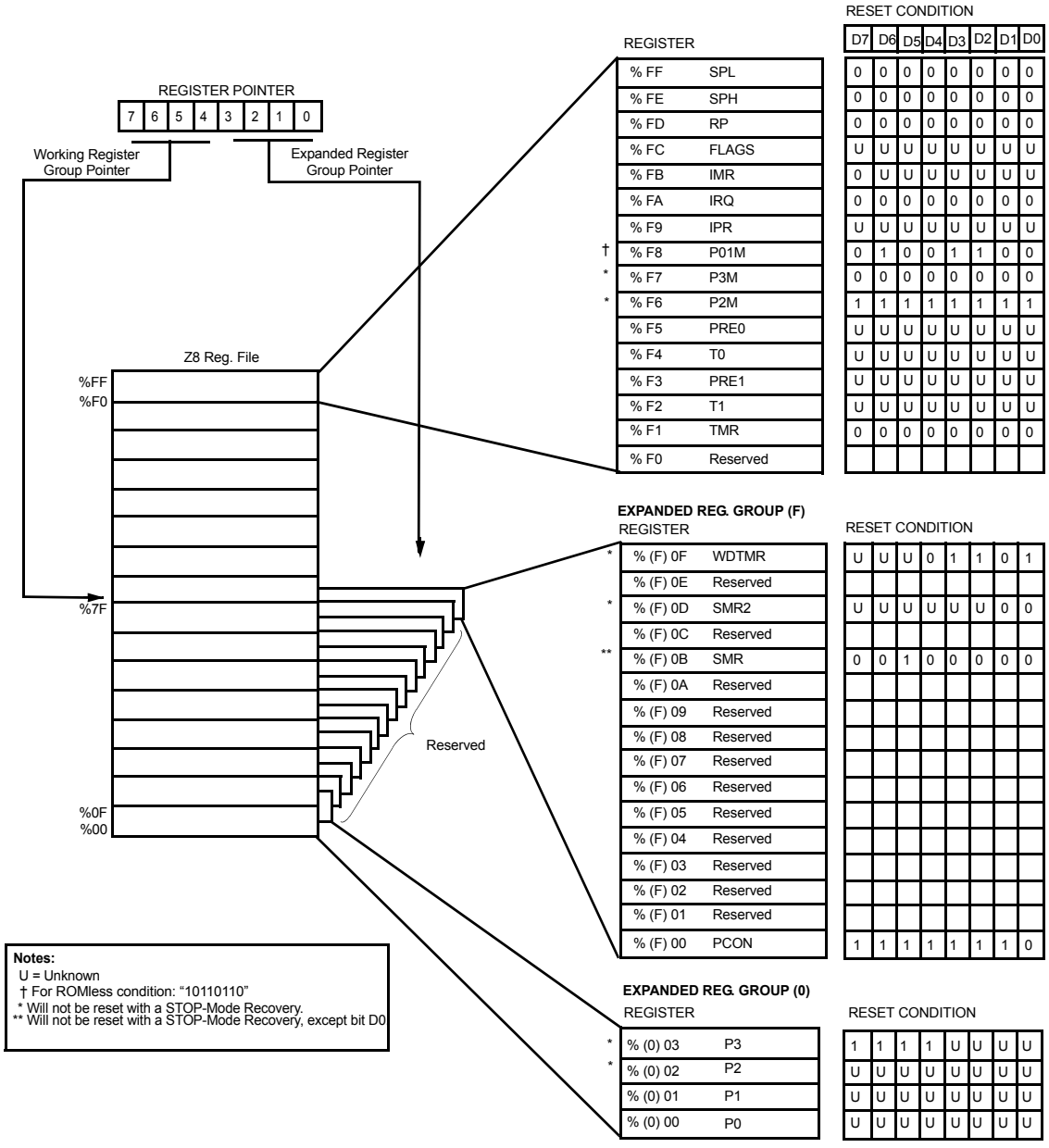


Figure 26. Expanded Register File Architecture

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. The register R254 is general-purpose on Z86E33/733/E34. R254 and R255 are set to 00h after any reset or Stop Mode Recovery.

RAM Protect. The upper portion of the RAM's address spaces 80h to EFh (excluding the control registers) can be protected from reading and writing. This option can be selected during the EPROM Programming Mode. After this option is selected, the user can activate this feature from the internal EPROM. D6 of the IMR control register (R251) is used to turn off/on the RAM protect by loading a 0 or 1, respectively. A "1" in D6 indicates RAM Protect enabled.

Stack. The Z86E43/743/E44 external data memory or the internal register file can be used for the stack. The 16-bit Stack Pointer (R254-R255) is used for the external stack, which can reside anywhere in the data memory for ROMless mode, but only from 4096/8192/16384 to 65535 in ROM mode. An 8-bit Stack Pointer (R255) is used for the internal stack on the Z8 that resides within the 236 general-purpose registers (R4-R239). SPH (R254) can be used as a general-purpose register when using internal stack only. R254 and R255 are set to 00H after any reset or Stop Mode Recovery.

Counter/Timers. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The Ti prescaler is driven by internal or external clock sources; however, the TO prescaler is driven by the internal clock only (see Figure 27).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256), that has been loaded into the counter. When the counter reaches the end of count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counters can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching one (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, can be read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3 line P36 serves as a timer output (T_{OUT}) through which T0, T1, or the internal clock can be output. The counter/timers can be cascaded by connecting the T0 output to the input of T1.

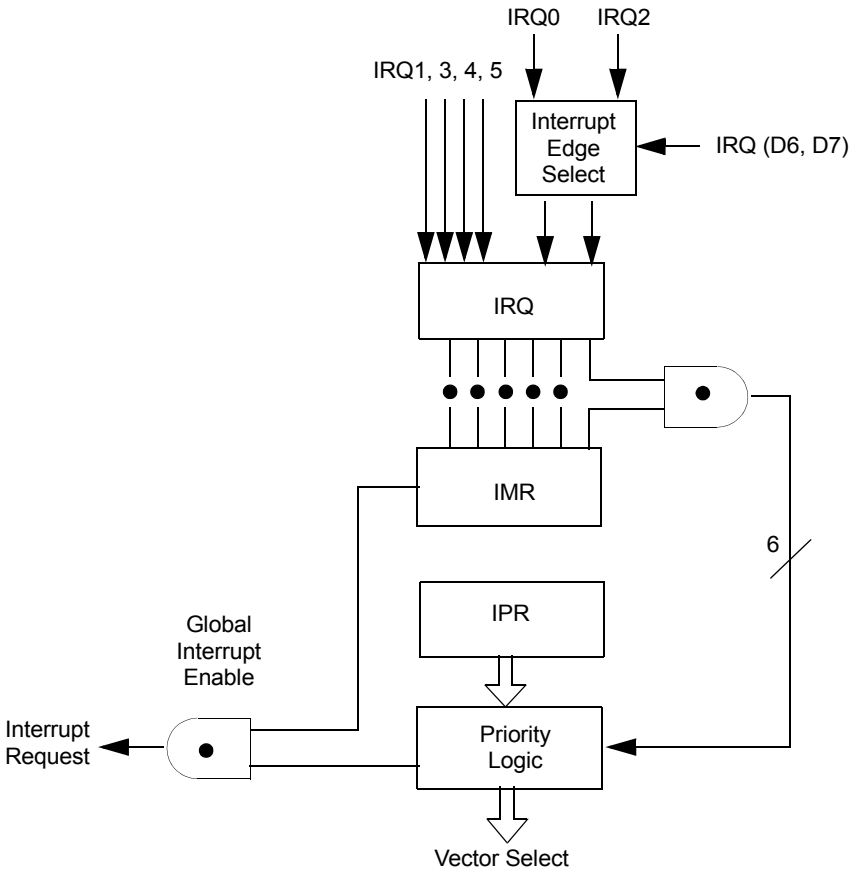


Figure 28. Interrupt Block Diagram

Table 20. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	$\overline{\text{DAV0}}$, IRQ0	0,1	External (P32), Rising/Falling Edge Triggered
IRQ1	IRQ1	2,3	External (P33), Falling Edge Triggered
IRQ2	$\overline{\text{DAV2}}$, IRQ2, T_{IN}	4,5	External (P31), Rising/Falling Edge Triggered
IRQ3	IRQ3	6,7	External (P30), Falling Edge Triggered
1RQ4	T0	8,9	Internal
IRQ5	T1	10,11	Internal

Z8 Control Register Diagrams

Ordering Information

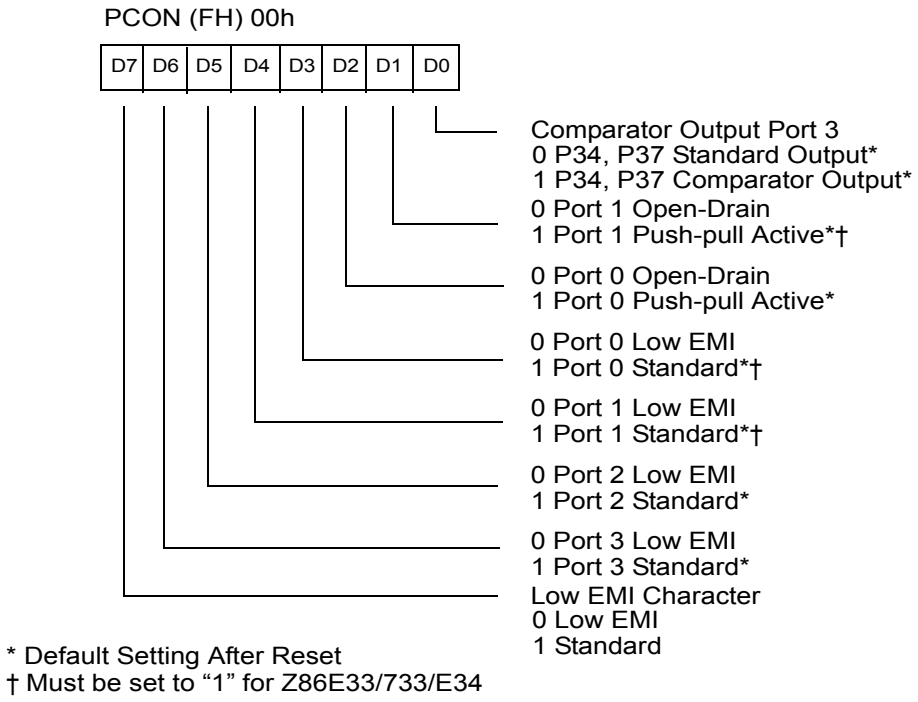
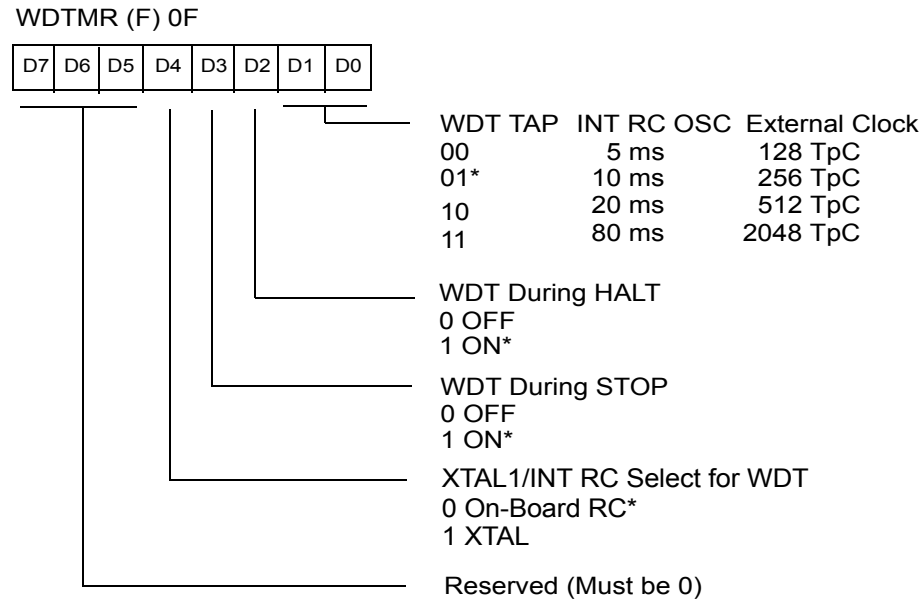
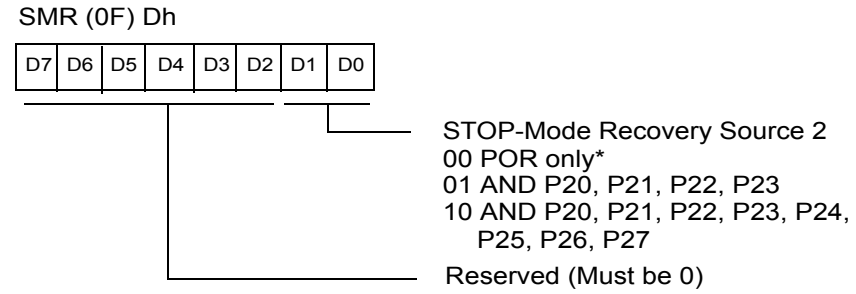


Figure 36. Port Configuration Register (PCON) (Write Only)



* Default setting after RESET

Figure 38. Watchdog Timer Mode Register (Write Only)



Note: Not used in conjunction with SMR Source

Figure 39. Stop Mode Recovery Register2 (Write Only)

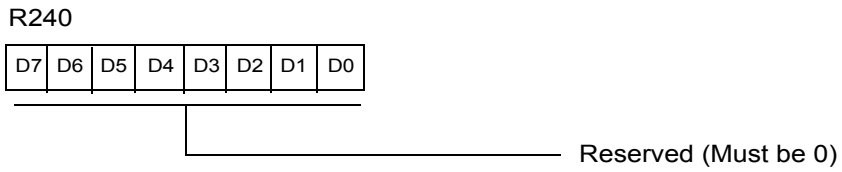


Figure 40. Reserved

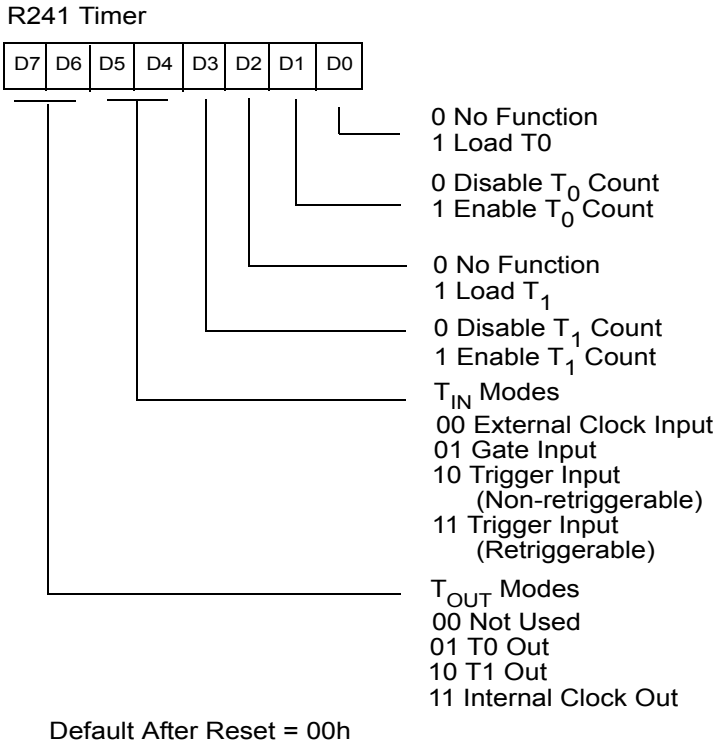


Figure 41. Timer Mode Register ($F1_h$: Read/Write)

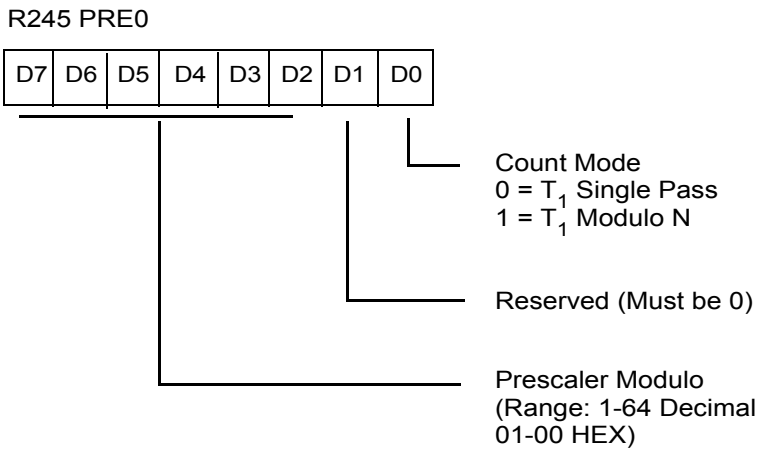


Figure 45. Prescaler 0 Register ($F5_h$: Write Only)

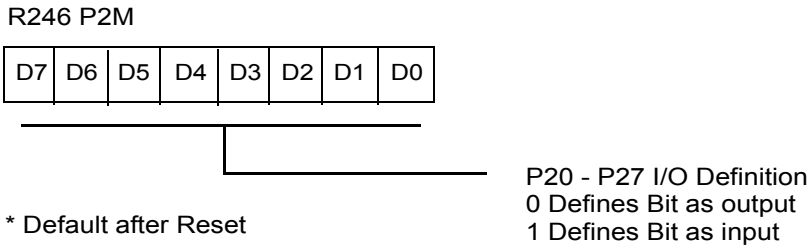


Figure 46. Port 2 Mode Register ($F6_h$: Write Only)

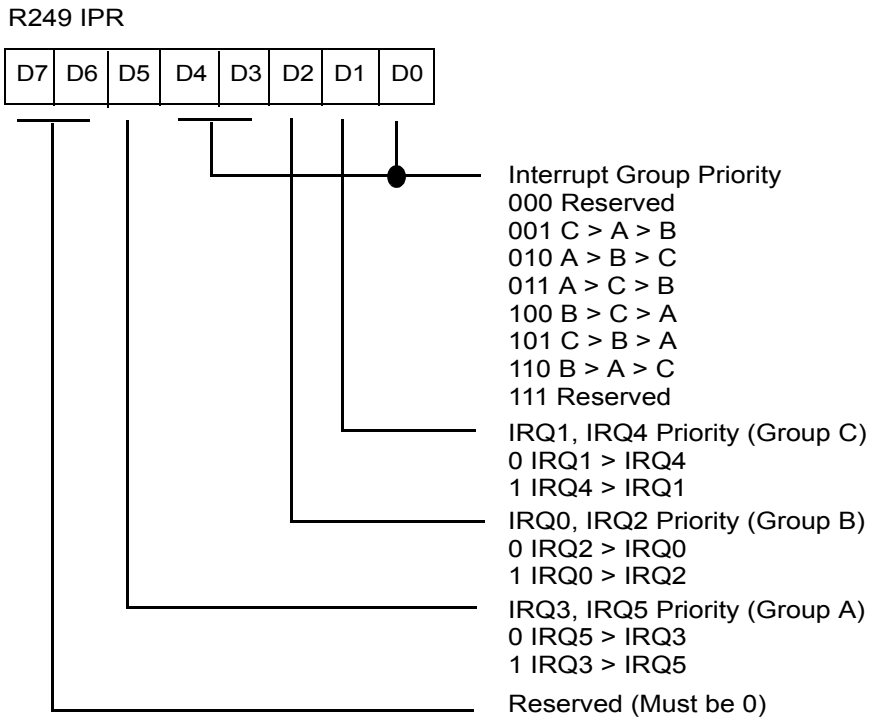


Figure 49. Interrupt Priority Register ($F9_h$: Write Only)

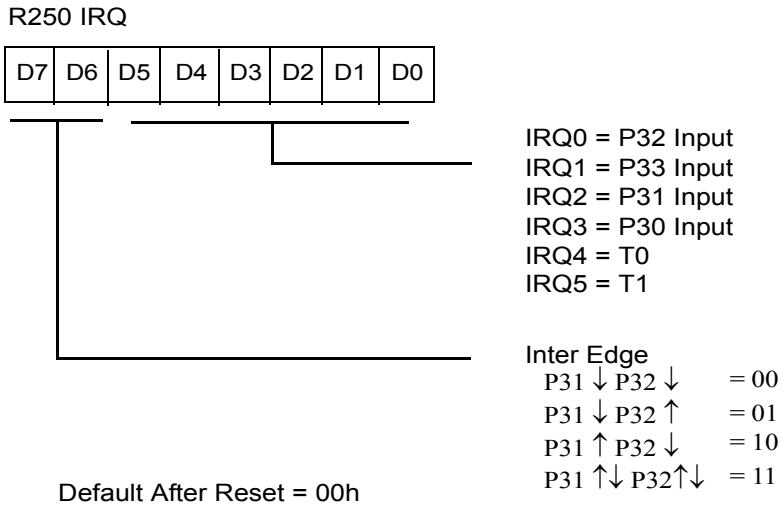


Figure 50. Interrupt Request Register (FA_h: Read/Write)