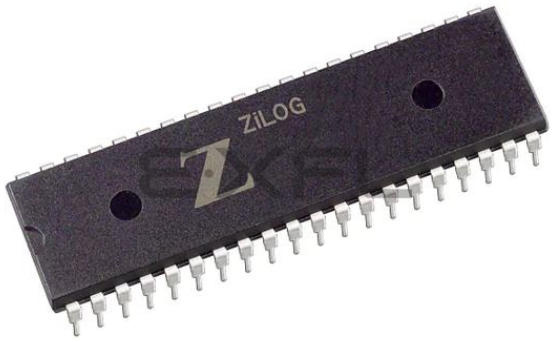

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	EBI/EMI
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.620", 15.75mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e4312psg

Table 1. Z86E33/733/E34, E43/743/E44 Features (Continued)

Device	ROM (KB)	RAM[1] (Bytes)	I/O Lines	Speed (MHz)
Z86E44	16	236	32	12

[1]General-Purpose

- Standard Temperature (V_{CC} = 3.5 V to 5.5 V)
- Extended Temperature (V_{CC} = 3.5 V to 5.5 V)
- Available Packages:
  - 28-Pin DIP/SOIC/PLCC OTP (E33/733/E34)
  - 40-Pin DIP OTP (E43/743/E44)
  - 44-Pin PLCC/LQFP OTP (E43/743/E44)
- Software Enabled Watchdog Timer (WDT)
- Push-Pull/Open-Drain Programmable on Port 0, Port 1, and Port 2
- 24/32 Input/Output Lines
- Clock-Free WDT Reset
- Auto Power-On Reset (POR)
- Programmable OTP Options:
  - RC Oscillator
  - EPROM Protect
  - Auto Latch Disable
  - Permanently Enabled WDT
  - Crystal Oscillator Feedback Resistor Disable
  - RAM Protect
- Low-Power Consumption: 60 mW
- Fast Instruction Pointer: 0.75 µs
- Two Standby Modes: STOP and HALT
- Digital Inputs CMOS Levels, Schmitt-Triggered
- Software Programmable Low EMI Mode
- Two Programmable 8-Bit Counter/Timers Each with a 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Six Different Sources
- Two Comparators

Table 5. 40-Pin DIP Package Pin Identification EPROM Mode (Continued)

Pin No	Symbol	Function	Direction
30	/PGM	Prog. Mode	Input
31	GND	Ground	
32-34	NC	No Connection	
35-39	D0-D4	Data 0,1,2,3,4	Input/Output
40	NC	No Connection	

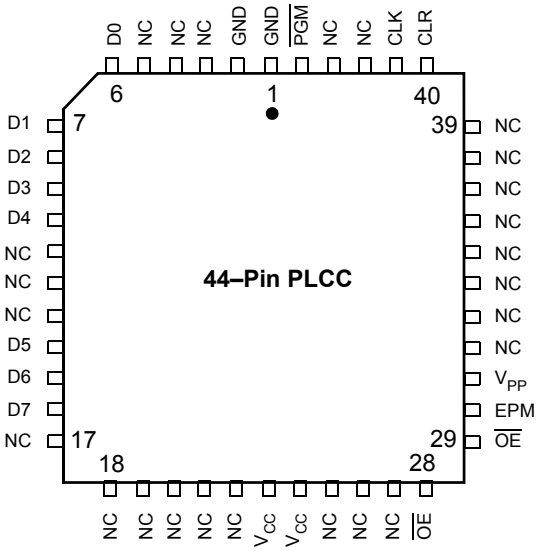


Figure 7. 44-Pin PLCC Pin Configuration EPROM Programming Mode

Table 6. 44-Pin PLCC Pin Configuration EPROM Programming Mode

Pin No	Symbol	Function	Direction
1-2	GND	Ground	
3-5	NC	No Connection	
6-10	D0-D4	Data 0,1,2,3,4	Input/Output
11-13	NC	No Connection	
14-16	D5-D7	Data 5,6,7	Input/Output
17-22	NC	No Connection	
23-24	V_{CC}	Power Supply	
25-27	NC	No Connection	
28	CE	Chip Select	Input
29	OE	Output Enable	Input
30	EPM	EPROM Prog. Mode	Input
31	V_{PP}	Prog. Voltage	Input

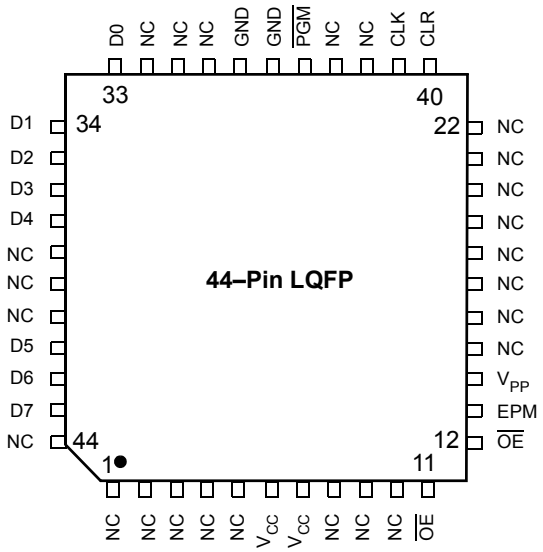


Figure 8. 44-Pin LQFP Pin Configuration EPROM Programming Mode

Table 7. 44-Pin LQFP Pin Identification EPROM Programming Mode

Pin No	Symbol	Function	Direction
1-5	NC	No Connection	
6-7	V_{CC}	Power Supply	
8-10	NC	No Connection	
11	CE	Chip Select	Input
12	OE	Output Enable	Input
13	EPM	EPROM Prog. Mode	Input
14	V_{PP}	Prog. Voltage	Input
15-22	NC	No Connection	
23	CLR	Clear	Input
24	CLK	Clock	Input
25-26	NC	No Connection	
27	/PGM	Prog. Mode	Input
28-29	GND	Ground	
30-32	NC	No Connection	

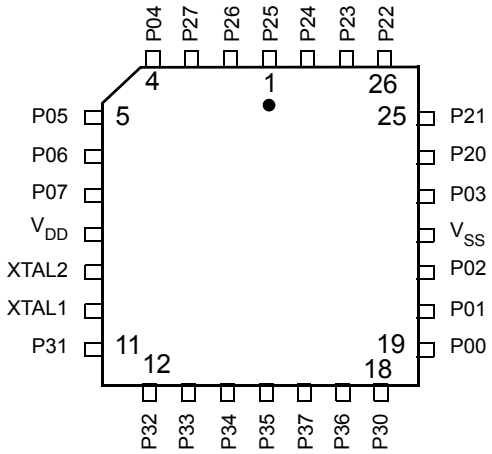


Figure 10. Standard Mode 28-Pin PLCC Pin Configuration

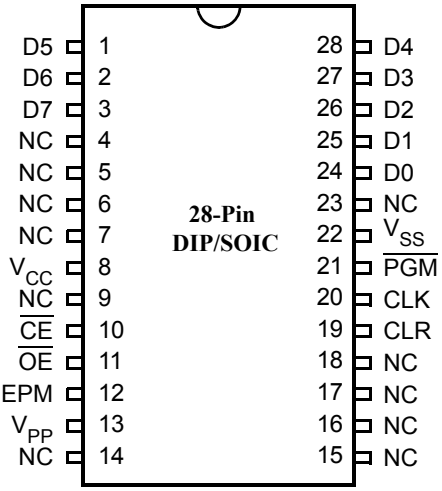


Figure 11. EPROM Programming Mode 28-Pin DIP/SOIC Pin Configuration

Total power dissipation should not exceed 1.21 W for the package. Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{DD} \times [I_{DD} - (\text{sum of } I_{OH}), + \text{sum of } [(V_{DD} - V_{OH}) \times I_{OH}] + \text{sum of } (V_{OL} \times I_{OL})$$

Standard Test Conditions

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Test Load).

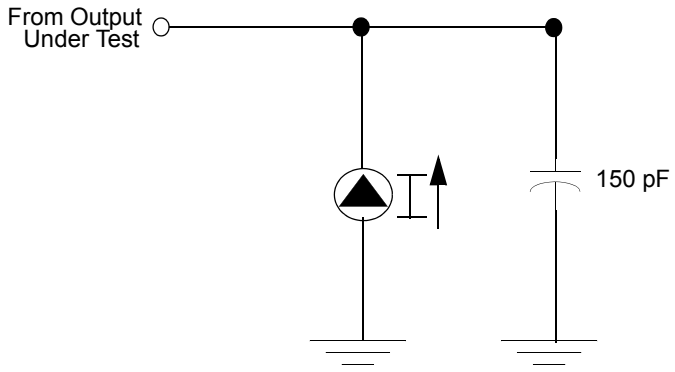


Figure 13. Test Load Diagram

Capacitance

T_A = 25 °C, V_{CC} = GND = 0 V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

Table 13. DC Electrical Characteristics T_A = 0 °C to +70 °C, 12 MHz (Continued)

No.	Symbol	Parameter	V_{CC} [1]	Min	Max	Units	Notes
18	TdDM(AS)	$\overline{DM}$ Valid to $\overline{AS}$ Rise Delay	3.5V	35		ns	2
			5.5V	35		ns	2
19	ThDS(AS)	$\overline{DS}$ Valid to Address Valid Hold Time	3.5V	35		ns	2
			5.5V	35		ns	2

Notes

1. The V_{CC} voltage specification of 5.5 V guarantees 5.0 V ± 0.5 V and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V.
2. Timing numbers given are for minimum TpC.
3. When using extended memory timing, add 2 TpC

Standard Test Load

All timing references use 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

For Standard Mode (not Low-EMI Mode for outputs) with SMR, D1 = 0, D0 = 0.

Table 14. DC Electrical Characteristics T_A = -40 °C to +105 °C, 12 MHz

No.	Symbol	Parameter	V_{CC} [1]	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to $\overline{AS}$ Rise Delay	4.5V	35		ns	2
			5.5V	35		ns	2
2	TdAS(A)	$\overline{AS}$ Rise to Address Float Delay	4.5V	45		ns	2
			5.5V	45		ns	2
3	TdAS(DR)	$\overline{AS}$ Rise to Read Data Req'd Valid	4.5V		250	ns	2,3
			5.5V		250	ns	2,3
4	TwAS	$\overline{AS}$ Low Width	4.5V	55		ns	2
			5.5V	55		ns	2
5	TdAS(DS)	Address Float to $\overline{DS}$ Fall	4.5V	0		ns	
			5.5V	0		ns	
6	TwDSR	$\overline{DS}$ (Read) Low Width	4.5V	200		ns	2,3
			5.5V	200		ns	2,3
7	TwDSW	$\overline{DS}$ (Write) Low Width	4.5V	110		ns	2,3
			5.5V	110		ns	2,3
8	TdDSR(DR)	$\overline{DS}$ Fail to Read Data Req'd Valid	4.5V		150	ns	2,3
			5.5V		150	ns	2,3
9	ThDR(DS)	Read Data to $\overline{DS}$ Rise Hold Time	4.5V	0		ns	2
			5.5V	0		ns	2

Table 18. Additional Timing Table (Divide by Two Mode) T_A = -40 °C to +105 °C

No	Symbol	Parameter	V_{CC}[1]	Min	Max	Min	Max	Units	Conditions	Notes
1	TpC	Input Clock Period	3.5V	62.5	DC	250	DC	ns		2,6,4
			5.5V	62.5	DC	250	DC	ns		2,6,4
2	TrC,TfC	Clock Input Rise & Fall Times	3.5V		15		25	ns		2,6,4
			5.5V		15		25	ns		2,6,4
3	TwC	Input Clock Width	3.5V	31		31		ns		2,6,4
			5.5V	31		31		ns		2,6,4
4	TwTinL	Timer Input Low Width	3.5V	70		70		ns		2,6,4
			5.5V	70		70		ns		2,6,4
5	TwTinH	Timer Input High Width	3.5V	5TpC		5TpC				2,6,4
			5.5V	5TpC		5TpC				2,6,4
6	TpTin	Timer Input Period	3.5V	8TpC		8TpC				2,6,4
			5.5V	8TpC		8TpC				2,6,4
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.5V		100		100	ns		2,6,4
			5.5V		100		100	ns		2,6,4
8A	TwIL	Int. Request Low Time	3.5V	70		70		ns		2,6,4,5
			5.5V	70		70		ns		2,6,4,5
8B	TwIL	Int. Request Low Time	3.5V	5TpC		5TpC				2,6,4,5
			5.5V	5TpC		5TpC				2,6,4,5
9	TwIH	Int. Request Input High Time	3.5V	5TpC		5TpC				2,6,4,5
			5.5V	5TpC		5TpC				2,6,4,5
10	Twsm	Stop Mode Recovery Width Spec	3.5V	12		12		ns		6,7
			5.5V	12		12		ns		6,7
11	Tost	Oscillator Startup Time	3.5V		5TpC		5TpC			6,7
			5.5V		5TpC		5TpC			6,7

CLR Clear (active High). This pin resets the internal address counter at the High Level.

CLK Address Clock. This pin is a clock input. The internal address counter increases by one for each clock cycle.

Application Precaution

The production test-mode environment may be enabled accidentally during normal operation if excessive noise surges above V_{CC} occur on pins P31 and $\overline{\text{RESET}}$.

In addition, processor operation of Z8 OTP devices may be affected by excessive noise surges on the V_{PP}, EPM, $\overline{\text{OE}}$ pins while the microcontroller is in Standard Mode.

Recommendations for dampening voltage surges in both test and OTP mode include the following:

- Using a clamping diode to V_{CC}
- Adding a capacitor to the affected pin
- Enable EPROM/Test Mode Disable OTP option bit.

Standard Mode

XTAL Crystal 1 (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC, RC network, or external single-phase clock to the on-chip oscillator input.

XTAL2 Crystal 2 (time-based output). This pin connects a parallel-resonant crystal, ceramic resonator, LC, or RC network to the on-chip oscillator output.

R/$\overline{\text{W}}$ Read/Write (output, write Low). The R/$\overline{\text{W}}$ signal is Low when the CCP is writing to the external program or data memory (Z86E43/743/E44 only).

$\overline{\text{RESET}}$ Reset (input, active Low). Reset will initialize the MCU. Reset is accomplished either through Power-On, Watchdog Timer reset, Stop Mode Recovery, or external reset. During Power-On Reset and Watchdog Timer Reset, the internally generated reset drives the reset pin low for the POR time. Any devices driving the reset line must be open-drain in order to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally. After the POR time, $\overline{\text{RESET}}$ is a Schmitt-triggered input. ($\overline{\text{RESET}}$ is available on Z86E43/743/E44 only.)

To avoid asynchronous and noisy reset problems, the Z86E43/743/E44 is equipped with a reset filter of four external clocks (4TpC). If the external reset signal is less than 4TpC in duration, no reset occurs. On the fifth clock after the reset is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external reset, whichever is longer. During the reset cycle, $\overline{\text{DS}}$ is held active Low while $\overline{\text{AS}}$ cycles at a rate of TpC/2. Program execution begins at location 000CH, 5-10 TpC cycles after $\overline{\text{RESET}}$ is released. For Power-On Reset, the reset output time is 5 ms.

The Z86E43/743/E44 does not reset WDTMR, SMR, P2M, and P3M registers on a Stop-Mode Recovery operation.

$\overline{\text{ROMless}}$ (input, active Low). This pin, when connected to GND, disables the internal ROM and forces the device to function as a Z86C90/C89 ROMless Z8. (Note that, when left unconnected or pulled High to V_{CC}, the device functions nor

Note: *When using in ROM Mode in High EMI (noisy) environment, the ROMless pins should be connected directly to V_{CC}.*

$\overline{\text{DS}}$ (output, active Low). Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of $\overline{\text{DS}}$. For WRITE operations, the falling edge of $\overline{\text{DS}}$ indicates that output data is valid.

$\overline{\text{AS}}$ (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle for external memory transfer. Address output is from Port 0/Port 1 for all external programs. Memory address transfers are valid at the trailing edge of $\overline{\text{AS}}$. Under program control, $\overline{\text{AS}}$ is placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

Port 0 (P07-P00). Port 0 is an 8-bit, bidirectional, CMOS-compatible I/0 port. These eight I/O lines can be configured under software control as a nibble I/0 port, or as an address port for interfacing external memory. The input buffers are Schmitt-triggered and nibble programmed. Either nibble output that can be globally programmed as push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 0 can be placed under handshake control. In Handshake Mode, Port 3 lines P32 and P35 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to Port 0's upper nibble. The lower nibble must have the same direction as the upper nibble.

For external memory references, Port 0 provides address bits A11-A8 (lower nibble) or Al 5-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. In ROMless mode, after a hardware reset, Port 0 is configured as address lines Al 5-A8, and extended timing is set to accommodate slow memory access. The initialization routine can include re-configuration to eliminate this extended timing mode. In ROM mode, Port 0 is defined as input after reset.

Port 0 can be set in the High-Impedance Mode if selected as an address output state, along with Port 1 and the control signals $\overline{\text{AS}}$, $\overline{\text{DS}}$, and R/$\overline{\text{W}}$ (Figure 18).

Table 19. Port 3 Pin Assignments

Pin	I/O	CTC1	Analog	Interrupt	P0 HS	P1 HS	P2 HS	Ext
P30	IN			IRQ3				
P31	IN	T_{IN}	AN1	IRQ2		D/R		
P32	IN		AN2	IRQ0	D/R			
P33	IN		REF	IRQ1		D/R		
P34	OUT		AN1-Out			R/D		DM
P35	OUT				R/D			
P36	OUT	T_{OUT}				R/D		
P37	OUT		An2-Out					

Comparator Inputs. Port 3, P31, and P32, each have a comparator front end. The comparator reference voltage P33 is common to both comparators. In analog mode, P31 and P32 are the positive input of the comparators and P33 is the reference voltage of the comparators.

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs (except P33-P31) that are not externally driven. Whether this level is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer. Auto Latches are available on Port 0, Port 1, Port 2, and P30. There are no Auto Latches on P31, P32, and P33.

Low EMI Emission. The Z86E43/743/E44 can be programmed to operate in a low EMI Emission Mode in the PCON register. The oscillator and all I/O ports can be programmed as low EMI emission mode independently. Use of this feature results in:

- The pre-drivers slew rate reduced to 10 ns typical.
- Low EMI output drivers have resistance of 200 Ohms (typical).
- Low EMI Oscillator.
- Internal SCLK/TCLK= XTAL operation limited to a maximum of 4 MHz - 250 ns cycle time, when Low EMI Oscillator is selected.

Note: *For emulation only:*
Do not set the emulator to emulate Port 1 in low EMI mode. Port 1 must always be configured in Standard Mode.

Functional Description

The MCU incorporates the following special functions to enhance the standard Z8 architecture to provide the user with increased design flexibility.

RESET. The device is reset in one of three ways:

1. Power-On Reset
2. Watchdog Timer
3. Stop Mode Recovery Source

Note: *Having the Auto Power-On Reset circuitry built-in, the MCU does not need to be connected to an external power-on reset circuit. The reset time is T_{POR}. The MCU does not re-initialize WDTMR, SMR, P2M, and P3M registers to their reset values on a Stop Mode Recovery operation.*

Note: *The device V_{CC} must rise up to the operating V_{CC} specification before the T_{POR} expires.*

Program Memory. The MCU can address up to 4/8/16 KB of Internal Program Memory (see Figure 22). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For EPROM mode, byte 12 (000Ch) to address 4095 (0FFFh)/8191 (1FFFh)/16384 (3FFFh), consists of programmable EPROM. After reset, the program counter points at the address 000Ch, which is the starting address of the user program.

In ROMless mode, the Z86E43/743/E44 can address up to 64 KB of External Program Memory. The ROM/ROMless option is only available on the 44-pin devices.

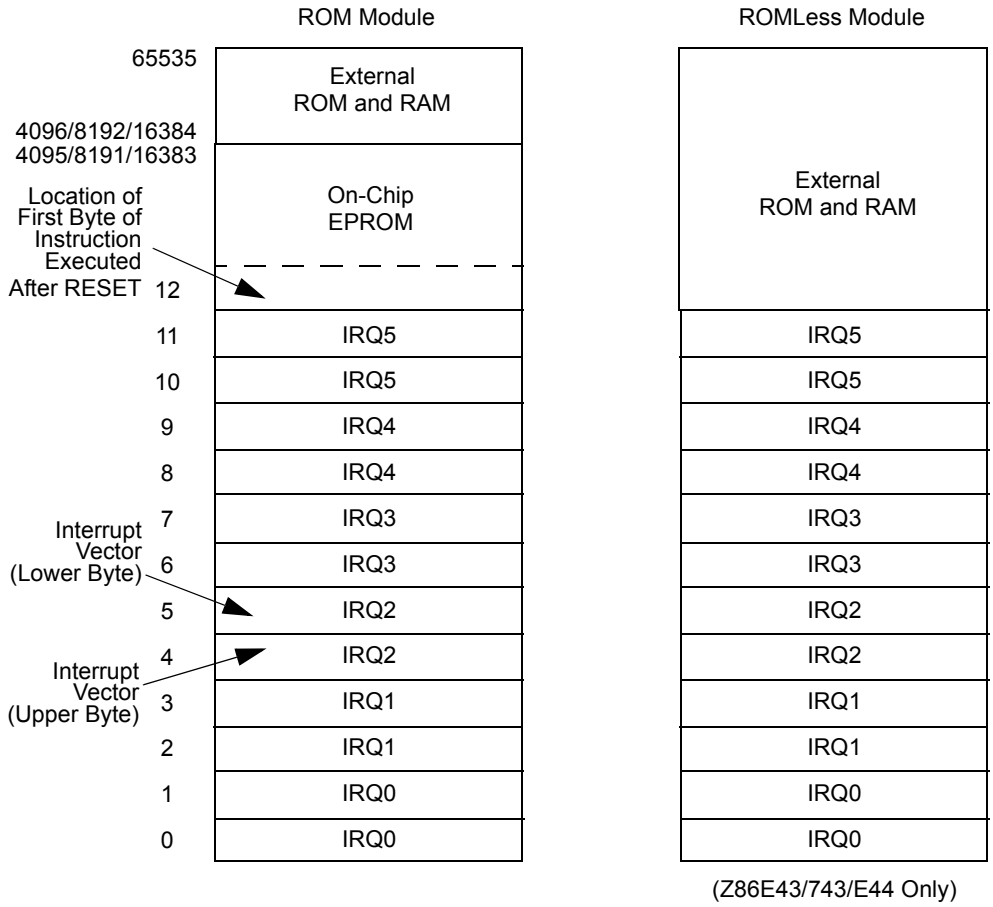


Figure 22. Program Memory Map

EPROM Protect. When in ROM Protect Mode, and executing out of External Program Memory, instructions LDC, LDCI, LDE, and LDEI cannot read Internal Program Memory.

When in EPROM Protect Mode and executing out of Internal Program Memory, instructions LDC, LDCI, LDE, and LDEI can read Internal Program Memory.

Data Memory ($\overline{DM}$). In ROM Mode, the Z86E43/743/E44 can address up to 60156/48 KB of external data memory beginning at location 4096/8192/16384. In ROMless mode, the Z86E43/743/E44 can address up to 64 KB of data memory. External data memory may be included with, or separated from, the external program memory space. $\overline{DM}$, an optional I/0 function that can be programmed to appear on pin P34, is used to distinguish between data and program memory space (Figure 23). The state of the $\overline{DM}$ signal is controlled by the type of instruction being executed. An LDC opcode references PROGRAM ($\overline{DM}$ inactive) memory, and an LDE instruction references data ($\overline{DM}$ active Low) memory.

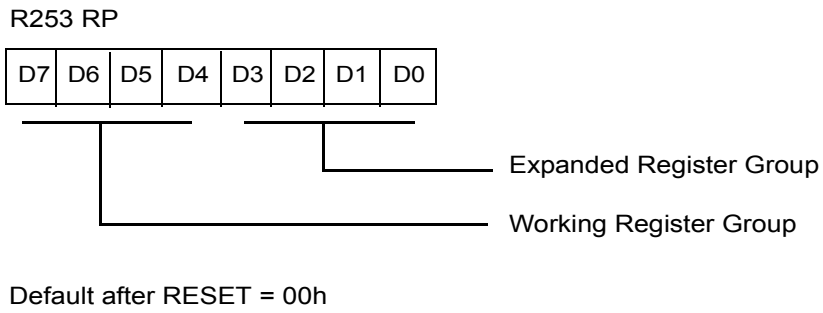


Figure 24. Register Pointer Register

Expanded Register File (ERF). The register file has been expanded to allow for additional system control registers, mapping of additional peripheral devices and input/output ports into the register address area. The Z8 register address space RO through R15 is implemented as 16 groups of 16 registers per group (see Figure 26). These register banks are known as the Expanded Register File (ERF).

The low nibble (D3-D0) of the Register Pointer (RP) select the active ERF Bank, and the high nibble (D7-D4) of register RP select the working register group. Three system configuration registers reside in the Expanded Register File at bank FH: PCON, SMR, and WDTMR. The rest of the Expanded Register is not physically implemented and is reserved for future expansion.

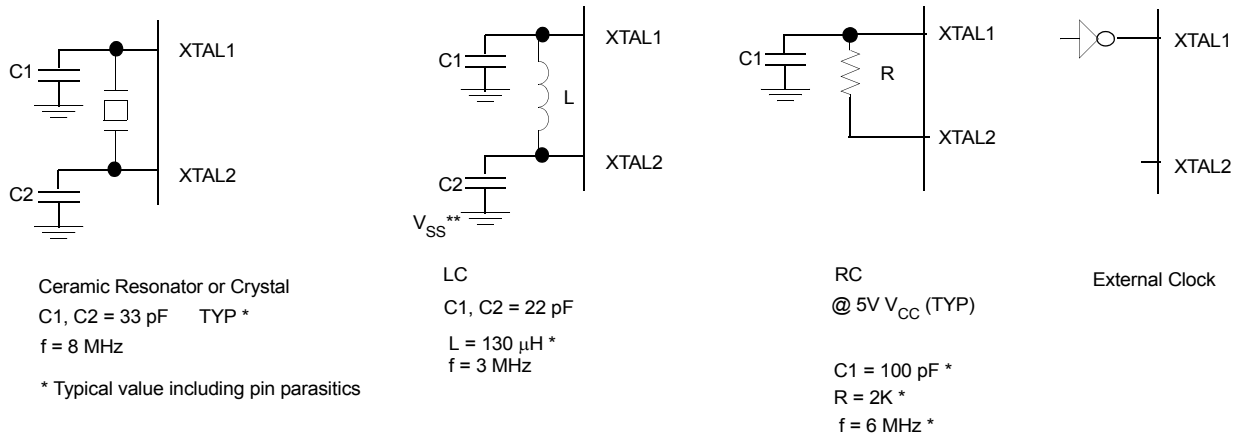


Figure 29. Oscillator Configuration

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR timer allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

1. Power fail to Power OK status
2. Stop Mode Recovery (if D5 of SMR=0)
3. WDT time-out

The POR time is a nominal 5 ms. Bit 5 of the STOP mode Register (SMR) determines whether the POR timer is by-passed after Stop Mode Recovery (typical for an external clock and RC/LC oscillators with fast start up times).

HALT. Turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupt IRQ0, IRQ1, and IRQ2 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT. In order to enter STOP or HALT Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, you must execute a NOP (Opcode = FFh) immediately before the appropriate sleep instruction, that is:

```
FF    NOP    ; clear the pipeline
6F    STOP   ; enter STOP mode
```

or

```
FF    NOP    ; clear the pipeline
7F    HALT   ; enter HALT mode
```

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 microamperes or less. STOP Mode is terminated by one of the following resets: either by WDT time-out, POR, a Stop Mode Recovery Source, which is defined by the SMR register or external reset. This causes the processor to restart the application program at address 000Ch.

Port Configuration Register (PCON). The PCON register configures the ports individually; comparator output on Port 3, open-drain on Port 0 and Port 1, low EMI on Ports 0, 1, 2 and 3, and low EMI oscillator. The PCON register is located in the expanded register file at Bank F, location 00 (Figure 30).

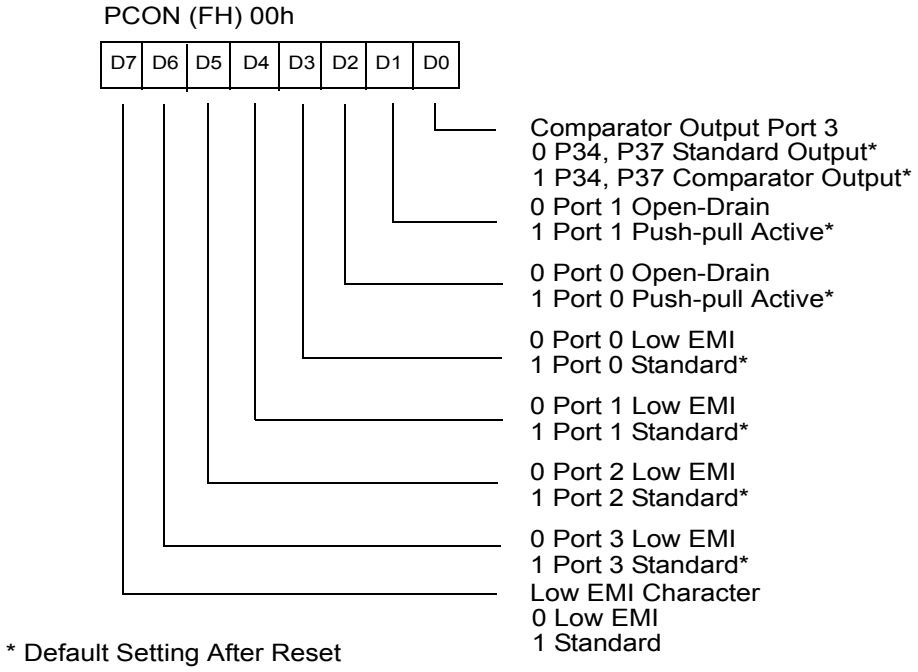


Figure 30. Port Configuration Register (PCON) (Write Only)

Note: *WDT time-out in STOP Mode will not reset SMR,SMR2,PCON, WDTMR, P2M, P3M, Ports 2 & 3 Data Registers, but will activate the T_{POR} delay.*

WDTMR Register Accessibility. The WDTMR register is accessible only during the first 60 internal system clock cycles from the execution of the first instruction after Power-On Reset, Watchdog reset or a Stop Mode Recovery (Figure 33 and Figure 34). After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register File at address location 0Fh.

Clock Free WDT Reset. The WDT will enable the Z8 to reset the I/0 pins whenever the WDT times out, even without a clock source running on the XTAL1 and XTAL2 pins. WDTMR Bit D4 must be 0 for the clock Free WDT to work. The I/O pins will default to their default settings.

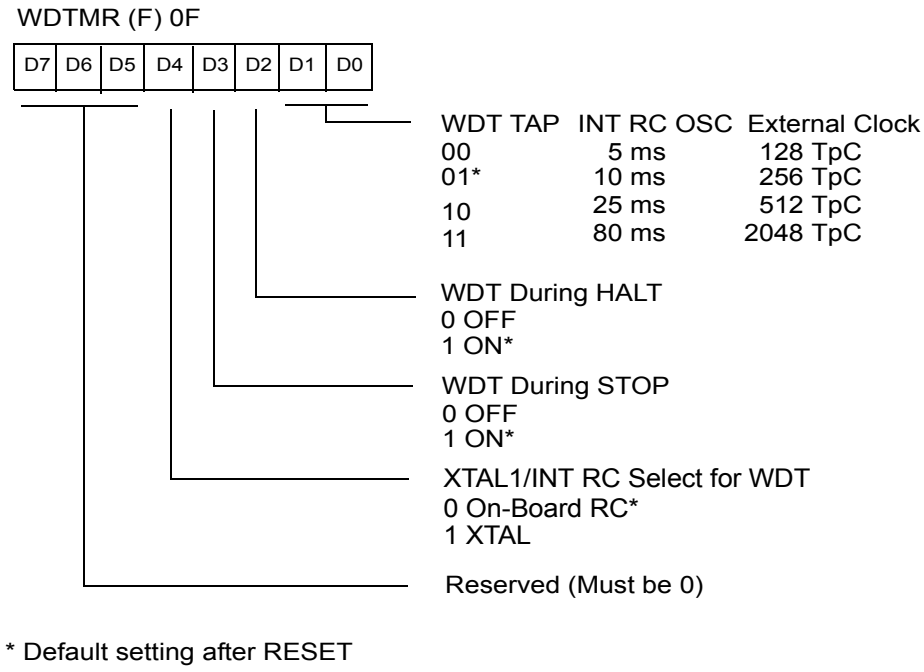
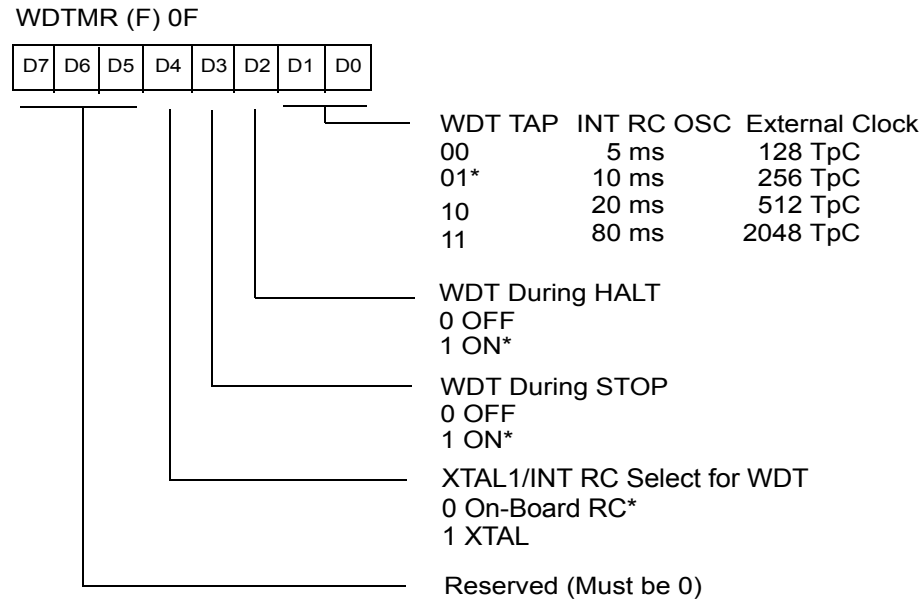
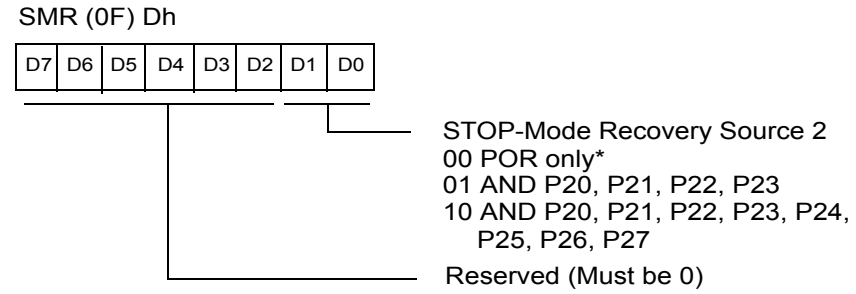


Figure 33. Watchdog Timer Mode Register Write Only



* Default setting after RESET

Figure 38. Watchdog Timer Mode Register (Write Only)



Note: Not used in conjunction with SMR Source

Figure 39. Stop Mode Recovery Register2 (Write Only)

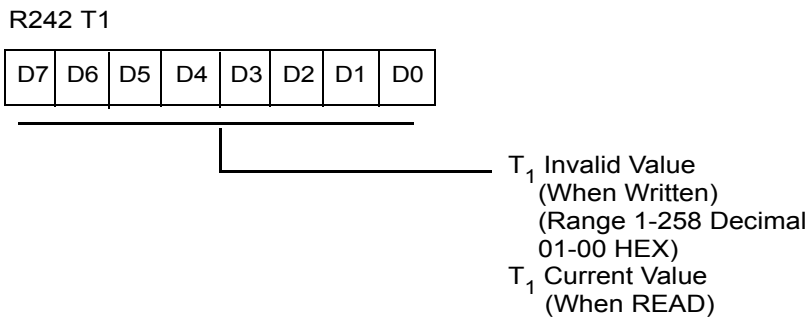


Figure 42. Counter/Timer 1 Register ($F2_h$: Read/Write)

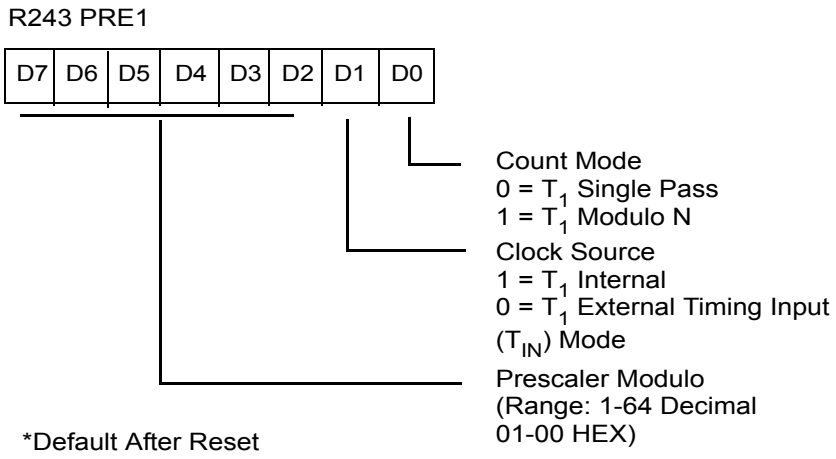


Figure 43. Prescaler 1 Register ($F3_h$: Write Only)

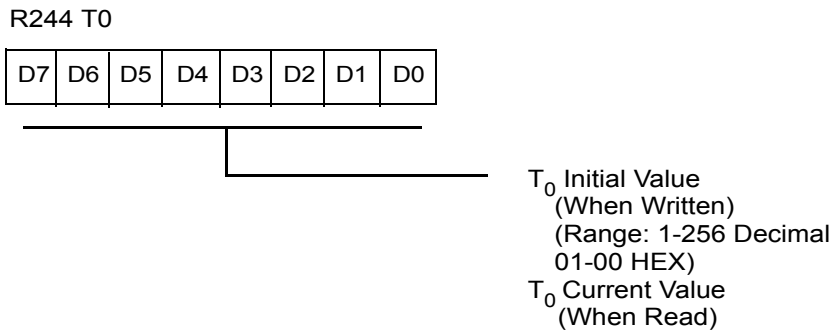


Figure 44. Counter/Timer 0 Register ($F4_h$: Read/Write)

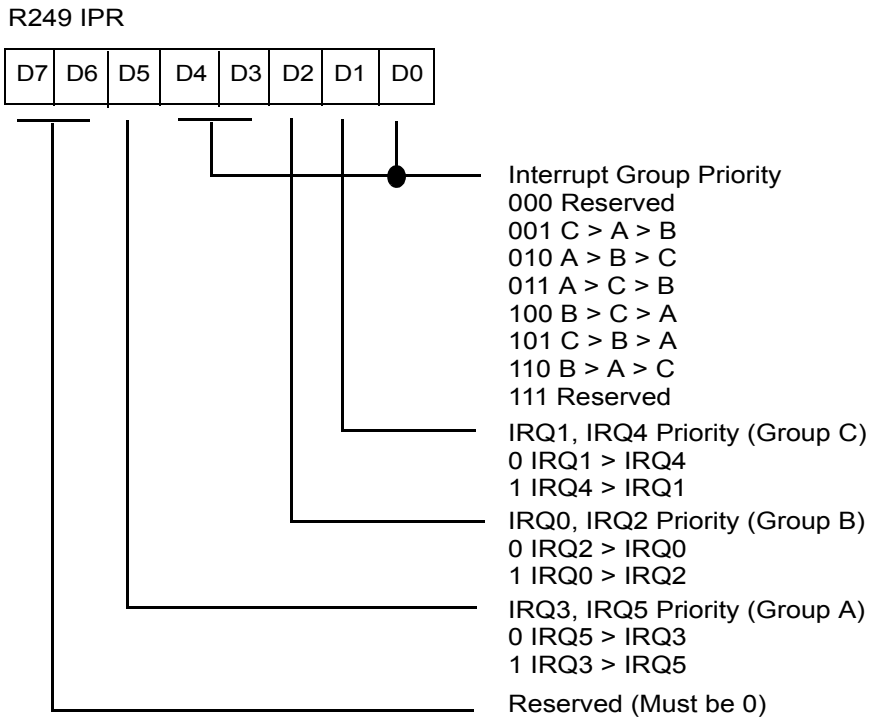


Figure 49. Interrupt Priority Register ($F9_h$: Write Only)

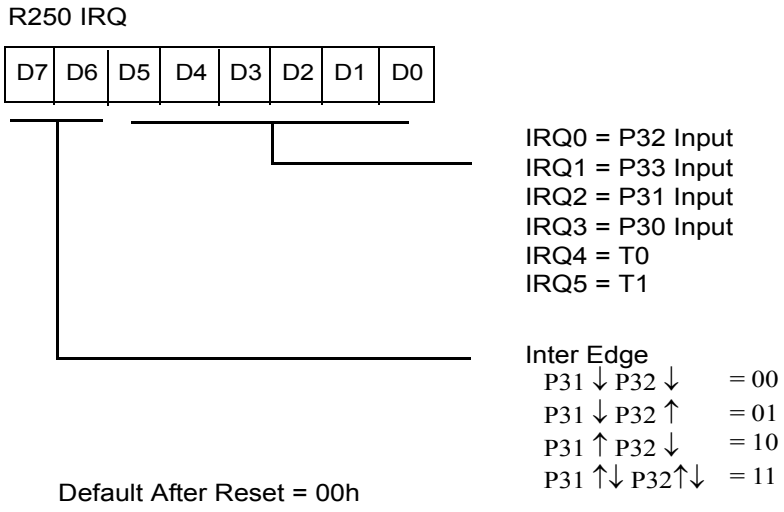


Figure 50. Interrupt Request Register (FA_h: Read/Write)