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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	EBI/EMI
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e4312vsc00tr

Table 1. Z86E33/733/E34, E43/743/E44 Features (Continued)

Device	ROM (KB)	RAM ¹ (Bytes)	I/O Lines	Speed (MHz)
Z86E44	16	236	32	12
¹ General-Purpose				

- Standard Temperature ($V_{CC} = 3.5 \text{ V to } 5.5 \text{ V}$)
- Extended Temperature ($V_{CC} = 3.5 \text{ V to } 5.5 \text{ V}$)
- Available Packages:
 - 28-Pin DIP/SOIC/PLCC OTP (E33/733/E34)
 - 40-Pin DIP OTP (E43/743/E44)
 - 44-Pin PLCC/LQFP OTP (E43/743/E44)
- Software Enabled Watchdog Timer (WDT)
- Push-Pull/Open-Drain Programmable on Port 0, Port 1, and Port 2
- 24/32 Input/Output Lines
- Clock-Free WDT Reset
- Auto Power-On Reset (POR)
- Programmable OTP Options:
 - RC Oscillator
 - EPROM Protect
 - Auto Latch Disable
 - Permanently Enabled WDT
 - Crystal Oscillator Feedback Resistor Disable
 - RAM Protect
- Low-Power Consumption: 60 mW
- Fast Instruction Pointer: 0.75 μs
- Two Standby Modes: STOP and HALT
- Digital Inputs CMOS Levels, Schmitt-Triggered
- Software Programmable Low EMI Mode
- Two Programmable 8-Bit Counter/Timers Each with a 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Six Different Sources
- Two Comparators

Table 3. 44-Pin PLCC Pin Identification (Continued)

Pin No	Symbol	Function	Direction
27	XTAL2	Crystal Oscillator	Output
28	XTAL1	Crystal Oscillator	Input
29-31	P31-P33	Port 3, Pins 1,2,3	Input
32	P34	Port 3, Pin 4	Output
33	AS	Address Strobe	Output
34	R//RL	ROM/ROMless select Input	
35	RESET	Reset	Input
36	P35	Port 3, Pin 5	Output
37	P37	Port 3, Pin 7	Output
38	P36	Port 3, Pin 6	Output
39	P30	Port 3, Pin 0	Input
40-41	P00-P01	Port 0, Pins 0,1	Input/Output
42-43	P10-P11	Port 1, Pins 0,1	Input/Output
44	P02	Port 0, Pin 2	Input/Output

Table 4. 44-Pin LQFP Pin Identification (Continued)

Pin No	Symbol	Function	Direction
18	RESET	Reset	Input
19	P35	Port 3, Pin 5	Output
20	P37	Port 3, Pin 7	Output
21	P36	Port 3, Pin 6	Output
22	P30	Port 3, Pin 0	Input
23-24	P00-P01	Port 0, Pin 0,1	Input/Output
25-26	P10-P11	Port 1, Pins 0,1	Input/Output
27	P02	Port 0, Pin 2	Input/Output
28-29	GND	Ground	
30-31	P12-P13	Port 1, Pins 2,3	Input/Output
32	P03	Port 0, Pin 3	Input/Output
33-37	P20-24	Port 2, Pins 0,1,2,3,4	Input/Output
38	DS	Data Strobe	Output
39	NC	No Connection	
40	$\overline{R/W}$	Read/Write	Output
41-43	P25-P27	Port 2, Pins 5,6,7	Input/Output
44	P04	Port 0, Pin 4	Input/Output

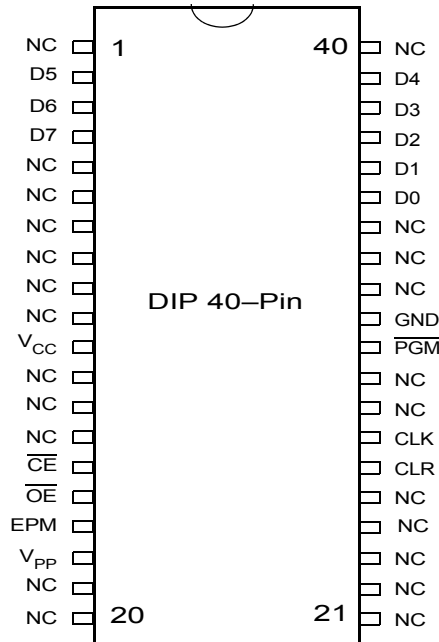


Figure 6. 40-Pin DIP Pin Configuration EPROM Mode

Table 5. 40-Pin DIP Package Pin Identification EPROM Mode

Pin No	Symbol	Function	Direction
1	NC	No Connection	
2-4	D5-D7	Data 5,6,7	Input/Output
5-10	NC	No Connection	
11	V _{CC}	Power Supply	
12-14	NC	No Connection	
15	CE	Chip Select	Input
16	OE	Output Enable	Input
17	EPM	EPROM Prog. Mode	Input
18	V _{PP}	Prog. Voltage	Input
19-25	NC	No Connection	
26	CLR	Clear	Input
27	CLK	Clock	Input
28-29	NC	No Connection	

**Table 7. 44-Pin LQFP Pin Identification EPROM Programming Mode
(Continued)**

Pin No	Symbol	Function	Direction
33-37	D0-D4	Data 0,1,2,3,4	Input/Output
38-40	NC	No Connection	
41-43	D5-D7	Data 5,6,7	Input/Output
44	NC	No Connection	

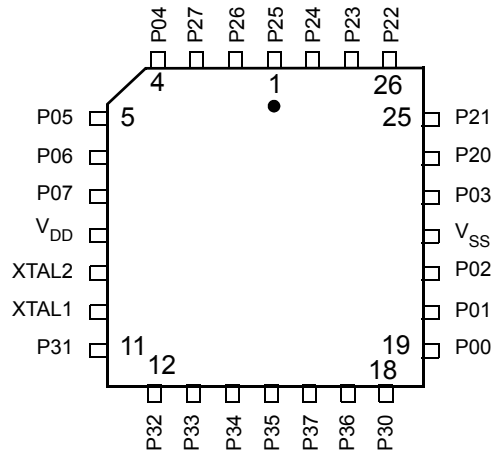


Figure 10. Standard Mode 28-Pin PLCC Pin Configuration

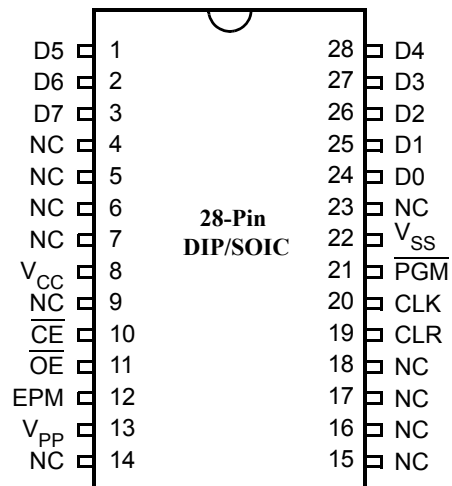


Figure 11. EPROM Programming Mode 28-Pin DIP/SOIC Pin Configuration

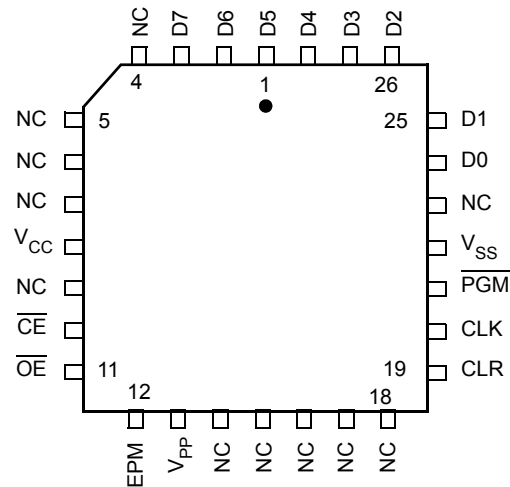


Figure 12. EPROM Programming Mode 28-Pin PLCC Pin Configuration

Table 9. 28-Pin EPROM Pin Identification EPROM Mode

Pin #	Symbol	Function	Direction
1-3	D5-D7	Data 5,6,7	Input/Output
4-7	NC	No Connection	
8	V _{CC}	Power Supply	
9	NC	No connection	
10	CE	Chip Select	Input
11	OE	Output Enable	Input
12	EPM	EPROM Prog. Mode	Input
13	V _{PP}	Prog. Voltage	Input
14-18	NC	No Connection	
19	CLR	Clear	
20	CLK	Clock	
21	/PGM	Prog. Mode	Input
22	V _{SS}	Ground	
23	NC	No Connection	
24-28	D0-D4	Data 0,1,2,3,4	Input/Output

DC Electrical Characteristics

Table 11. DC Electrical Characteristics $T_A = 0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$

Symbol	Parameter	V_{CC}^1	Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.5V	$0.7 V_{CC}$	$V_{CC} + 0.3$	1.8	V	Driven by External Clock Generator	
		5.5V	$0.7 V_{CC}$	$V_{CC} + 0.3$	2.5	V		
V_{CL}	Clock Input Low Voltage	3.5V	GND -0.3	$0.2 V_{CC}$	0.9	V	Driven by External Clock Generator	
		5.5V	GND -0.3	$0.2 V_{CC}$	1.5	V		
V_{IH}	Input High Voltage	3.5V	$0.7 V_{CC}$	$V_{CC} + 0.3$	2.5	V		
		5.5V	$0.7 V_{CC}$	$V_{CC} + 0.3$	2.5	V		
V_{IL}	Input Low Voltage	3.5V	GND -0.3	$0.2 V_{CC}$	1.5	V		
		5.5V	GND -0.3	$0.2 V_{CC}$	1.5	V		
V_{OH}	Output High Voltage Low EMI Mode	3.5V	$V_{CC} - 0.4$		3.3		$I_{OH} = -0.5\text{ mA}$	
		5.5V	$V_{CC} - 0.4$		4.8			
V_{OH1}	Output High Voltage	3.5V	$V_{CC} - 0.4$		3.3	V	$I_{OH} = -2.0\text{ mA}$	
		5.5V	$V_{CC} - 0.4$		4.8	V	$I_{OH} = -2.0\text{ mA}$	
V_{OL}	Output Low Voltage Low EMI Mode	3.5V		0.4	0.2	V	$I_{OL} = 1.0\text{ mA}$	
		5.5V		0.4	0.2	V	$I_{OL} = 1.0\text{ mA}$	
V_{OL1}	Output Low Voltage	3.5V		0.4	0.1	V	$I_{OL} = +4.0\text{ mA}$	2
		5.5V		0.4	0.1	V	$I_{OL} = +4.0\text{ mA}$	2
V_{OL2}	Output Low Voltage	3.5V		1.2	0.5	V	$I_{OL} = +10\text{ mA}$	2
		5.5V		1.2	0.5	V	$I_{OL} = +10\text{ mA}$	2
V_{RH}	Reset Input High Voltage	3.5V	$.8 V_{CC}$	V_{CC}	1.7	V		3
		5.5V	$.8 V_{CC}$	V_{CC}	2.1	V		3
V_{RL}	Reset Input Low Voltage	3.5V	GND -0.3	$0.2 V_{CC}$	1.3	V		3
		5.5V	GND -0.3	$0.2 V_{CC}$	1.7	V		3
V_{OLR}	Reset Output Low Voltage	3.5V		0.6	0.3	V	$I_{OL} = 1.0\text{ mA}$	3
		5.5V		0.6	0.2	V	$I_{OL} = 1.0\text{ mA}$	3

Table 12. DC Electrical Characteristics $T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$ (Continued)

Symbol	Parameter	V_{CC} ¹	Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC2}	Standby Current STOP Mode	4.5V		10	2	μA	$V_{IN} = 0\text{V}$, V_{CC}	7,8,9
		5.5V		10	3	μA	$V_{IN} = 0\text{V}$, V_{CC}	7,8,9
		4.5V		40	10	μA	$V_{IN} = 0\text{V}$, V_{CC}	7,8
		5.5V		40	10	μA	$V_{IN} = 0\text{V}$, V_{CC}	7,8
I_{ALL}	Auto Latch Low Current	4.5V	1.4	20	4.7	μA	$0\text{V} < V_{IN} < V_{CC}$	10
		5.5V	1.4	20	4.7	μA	$0\text{V} < V_{IN} < V_{CC}$	10
I_{ALH}	Auto Latch High Current	4.5V	-1.0	-10	-3.8	μA	$0\text{V} < V_{IN} < V_{CC}$	10
		5.5V	-1.0	-10	-3.8	μA	$0\text{V} < V_{IN} < V_{CC}$	10
T_{POR}	Power-On Reset	4.5V	1.0	14	4	ms		
		5.5V	1.0	14	4	ms		
V_{LV}	Auto Reset Voltage		2.0	3.3	2.8	V		11

Notes

1. The V_{CC} voltage specification of 5.5 V guarantees $5.0\text{ V} \pm 0.5\text{ V}$ and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V.
2. STD Mode (not Low EMI Mode).
3. Z86E43/743/E44 only.
4. For analog comparator inputs when analog comparators are enabled.
5. All outputs unloaded, I/O pins floating, inputs at rail.
6. $CL1=CL2=22\text{ pF}$.
7. Same as note 5 except inputs at V_{CC} .
8. Clock must be forced Low, when XTAL1 is clock driven and XTAL2.
9. WDT is not running.
10. Auto Latch (mask option) selected.
11. Device does function down to the Auto Reset voltage.

Table 13. DC Electrical Characteristics $T_A = 0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$, 12 MHz (Continued)

No.	Symbol	Parameter	V_{CC}^1	Min	Max	Units	Notes
18	TdDM(AS)	$\overline{\text{DM}}$ Valid to $\overline{\text{AS}}$ Rise Delay	3.5V	35		ns	2
			5.5V	35		ns	2
19	ThDS(AS)	$\overline{\text{DS}}$ Valid to Address Valid Hold Time	3.5V	35		ns	2
			5.5V	35		ns	2

Notes

1. The V_{CC} voltage specification of 5.5 V guarantees $5.0\text{ V} \pm 0.5\text{ V}$ and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V.
2. Timing numbers given are for minimum T_{pC} .
3. When using extended memory timing, add 2 T_{pC}

Standard Test Load

All timing references use $0.7\text{ }V_{CC}$ for a logic 1 and $0.2\text{ }V_{CC}$ for a logic 0.

For Standard Mode (not Low-EMI Mode for outputs) with SMR, D1 = 0, D0 = 0.

Table 14. DC Electrical Characteristics $T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$, 12 MHz

No.	Symbol	Parameter	V_{CC}^1	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to $\overline{\text{AS}}$ Rise Delay	4.5V	35		ns	2
			5.5V	35		ns	2
2	TdAS(A)	$\overline{\text{AS}}$ Rise to Address Float Delay	4.5V	45		ns	2
			5.5V	45		ns	2
3	TdAS(DR)	$\overline{\text{AS}}$ Rise to Read Data Req'd Valid	4.5V		250	ns	2,3
			5.5V		250	ns	2,3
4	TwAS	$\overline{\text{AS}}$ Low Width	4.5V	55		ns	2
			5.5V	55		ns	2
5	TdAS(DS)	Address Float to $\overline{\text{DS}}$ Fall	4.5V	0		ns	
			5.5V	0		ns	
6	TwDSR	$\overline{\text{DS}}$ (Read) Low Width	4.5V	200		ns	2,3
			5.5V	200		ns	2,3
7	TwDSW	$\overline{\text{DS}}$ (Write) Low Width	4.5V	110		ns	2,3
			5.5V	110		ns	2,3
8	TdDSR(DR)	$\overline{\text{DS}}$ Fail to Read Data Req'd Valid	4.5V		150	ns	2,3
			5.5V		150	ns	2,3
9	ThDR(DS)	Read Data to $\overline{\text{DS}}$ Rise Hold Time	4.5V	0		ns	2
			5.5V	0		ns	2

Table 15. Additional Timing Table (Divide-By-One Mode) $T_A = 0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$ (Continued)

No	Symbol	Parameter	V_{CC}^1	Min	Max	Min	Max	Units	Notes
5	TwTinH	Timer Input High Width	3.5V	5TpC		5TpC			2,3,4
			5.5V	5TpC		5TpC			2,3,4
6	TpTin	Timer Input Period	3.5V	8TpC		8TpC			2,3,4
			5.5V	8TpC		8TpC			2,3,4
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.5V		100		100	ns	2,3,4
			5.5V		100		100	ns	2,3,4
8A	TwIL	Int. Request Low Time	3.5V	100		100		ns	2,3,4,5
			5.5V	70		70		ns	2,3,4,5
8B	TwIL	Int. Request Low Time	3.5V	5TpC		5TpC			2,3,4,6
			5.5V	5TpC		5TpC			2,3,4,6
9	TwIH	Int. Request Input High Time	3.5V	5TpC		5TpC			2,3,4,5
			5.5V	5TpC		5TpC			2,3,4,5
10	Twsm	Stop Mode Recovery Width Spec	3.5V	12		12		ns	4,7
			5.5V	12		12		ns	4,7
11	Tost	Oscillator Startup Time	3.5V		5TpC		5TpC		4,7,8
			5.5V		5TpC		5TpC		4,7,8

Notes

1. The V_{CC} voltage specification of 5.5 V guarantees 5.0 V $\pm$ 0.5 V and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V.
2. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
3. SMR D1 = 0.
4. Maximum frequency for internal system clock is 4 MHz when using Low EMI OSC PCON Bit D7 = 0.
5. Interrupt request via Port 3 (P31-P33).
6. Interrupt request via Port 3 (P30).
7. SMR-D5 = 1, POR STOP Mode Delay is on.
8. For RC and LC oscillator, and for oscillator driven by clock driver.

Table 16. Additional Timing Table (Divide-By-One Mode) $T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$

No	Symbol	Parameter	V_{CC}^1	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	4.5V	250	DC	166	DC	ns	2,3,4
			5.5V	250	DC	166	DC	ns	2,3,4

Table 17. Additional Timing Table (Divide by Two Mode) $T_A = 0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$ (Continued)

No	Symbol	Parameter	V_{CC} ¹	Min	Max	Min	Max	Units	Conditions	Notes
4	TwTinL	Timer Input Low Width	3.5V	70		70		ns		2,6,4
			5.5V	70		70		ns		2,6,4
5	TwTinH	Timer Input High Width	3.5V	5TpC		5TpC				2,6,4
			5.5V	5TpC		5TpC				2,6,4
6	TpTin	Timer Input Period	3.5V	8TpC		8TpC				2,6,4
			5.5V	8TpC		8TpC				2,6,4
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.5V		100		100	ns		2,6,4
			5.5V		100		100	ns		2,6,4
8A	TwIL	Int. Request Low Time	3.5V	70		70		ns		2,6,4,5
			5.5V	70		70		ns		2,6,4,5
8B	TwIL	Int. Request Low Time	3.5V	5TpC		5TpC				2,6,4,5
			5.5V	5TpC		5TpC				2,6,4,5
9	TwIH	Int. Request Input High Time	3.5V	5TpC		5TpC				2,6,4,5
			5.5V	5TpC		5TpC				2,6,4,5
10	Twsm	Stop Mode Recovery Width Spec	3.5V	12		12		ns		6,7
			5.5V	12		12		ns		6,7
11	Tost	Oscillator Startup Time	3.5V		5TpC		5TpC			6,7
			5.5V		5TpC		5TpC			6,7
12	Twdt	Watchdog Timer Delay Time Before Timeout	3.5V	7		10		ms	D0 = 0	8,9
			5.5V	3.5		5		ms	D1 = 0	5,11
			3.5V	14		20		ms	D0 = 1	5,11
			5.5V	7		10		ms	D1 = 0	5,11
			3.5V	28		40		ms	D1 = 0	5,11
			5.5V	14		20		ms	D1 = 1	5,11
			3.5V	112		160		ms	D0 = 1	5,11
			5.5V	56		80		ms	D1 = 1	5,11

Notes

1. The V_{CC} voltage specification of 5.5 V guarantees $5.0\text{ V} \pm 0.5\text{ V}$ and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V.
2. Timing Reference uses 0.7 V_{C0} for a logic 1 and 0.2 V_{G0} for a logic 0.
3. SMR D1 = 0.
4. SMR-D5 = 1, POR STOP Mode Delay is on
5. Interrupt request via Port 3 (P31-P33)
6. Interrupt request via Port 3 (P30).
7. Maximum frequency for internal system clock is 2 MHz when using Low EMI OSC PCON Bit D7 = 0
8. Reg. WDTMR.
9. Using internal RC.

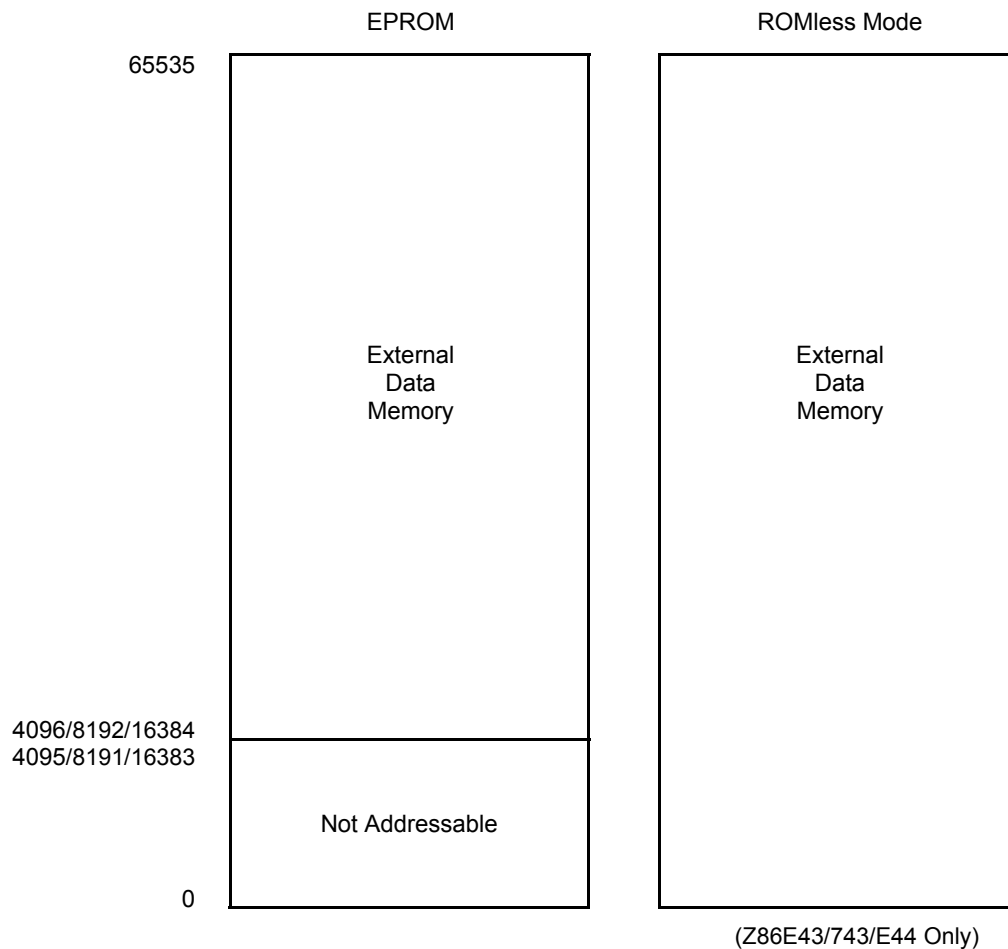


Figure 23. Data Memory Map

Register File. The register file consists of three I/O port registers, 236/125 general-purpose registers, 15 control and status registers, and three system configuration registers in the expanded register group. The instructions can access registers directly or indirectly through an 8-bit address field. This allows a short 4-bit register address using the Register Pointer (see [Figure 24](#)). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

► **Note:** *Register Group E0-EF can only be accessed through working register and indirect addressing modes.*

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority Register (IPR). An interrupt machine cycle is activated when an interrupt request is granted. Thus, disabling all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests need service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling or both edge triggered, and are programmable by the user. The software may poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in bits D7 and D6 of the IRQ Register (R250). The configuration is shown in [Table 21](#).

Table 21. IRQ Register Configuration

IRO		Interrupt Edge	
D7	D6	P31	P32
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes

1. F = Falling Edge
2. R = Rising Edge

Clock. The on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, RC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 10 kHz to 16 MHz max, with a series resistance (RS) less than or equal to 100 Ω .

The crystal should be connected across XTAL1 and XTAL2 using the vendor's recommended capacitor values from each pin directly to device pin Ground. The RC oscillator option can be selected in the programming mode. The RC oscillator configuration must be an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to Ground ([Table 29](#)).

from STOP mode when programmed as analog inputs. When the Stop Mode Recovery sources are selected in this register then SMR2 register bits D0, D1 must be set to zero.

► **Note:** *If the Port 2 pin is configured as an output, this output level will be read by the SMR circuitry.*

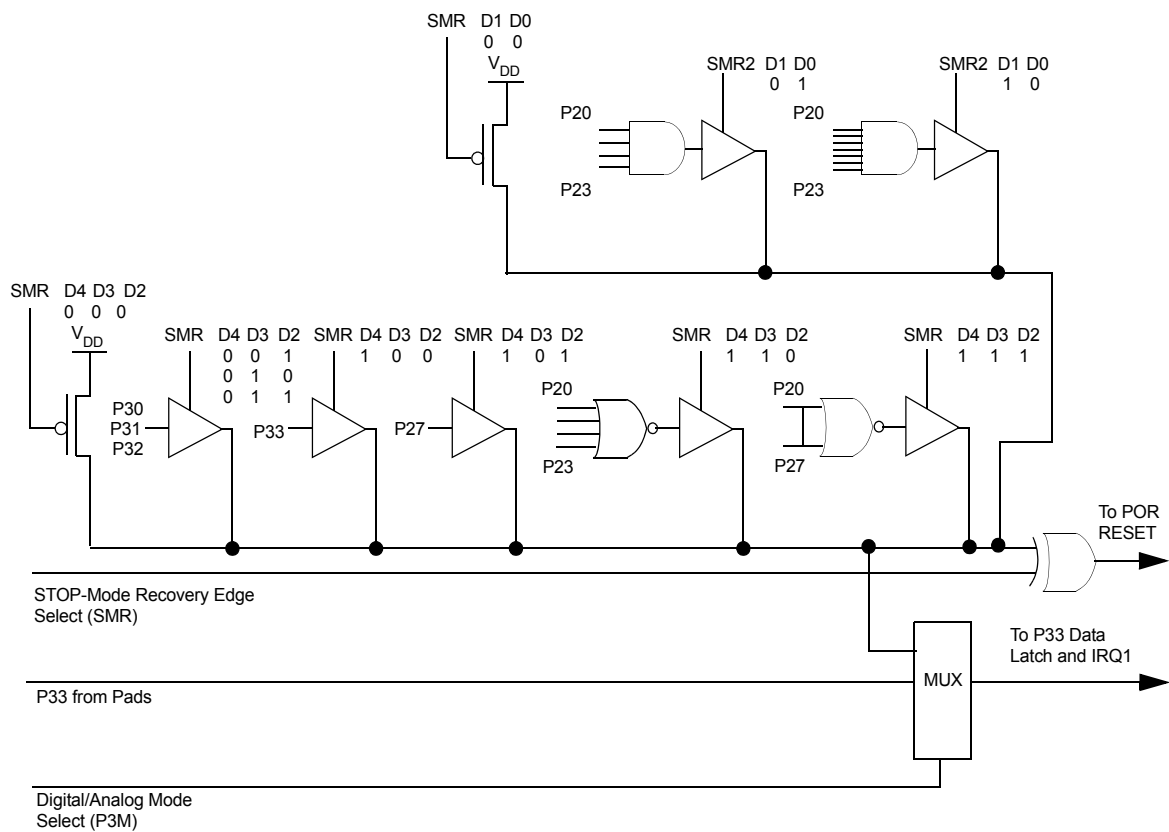


Figure 32. Stop Mode Recovery Source

Reset and initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT is driven either by an on-board RC oscillator or an external oscillator from XTAL1 pin. The POR clock source is selected with bit 4 of the WDT register.

► **Note:** Execution of the WDT instruction affects the Z (Zero), S (Sign), and V (Overflow) flags.

WDT Time-Out Period (D0 and D1). Bits 0 and 1 control a tap circuit that determines the time-out periods that can be obtained (Table 23). The default value of D0 and D1 are 1 and 0, respectively.

Table 23. Time-out Period of WDT

D1	D0	Time-out of the Internal RC OSC	Time-out of the System Clock
0	0	5 ms	128 SCLK
0	1	10 ms ¹	256 SCLK ¹
1	0	20 ms	512 SCLK
1	1	80 ms	2048 SCLK

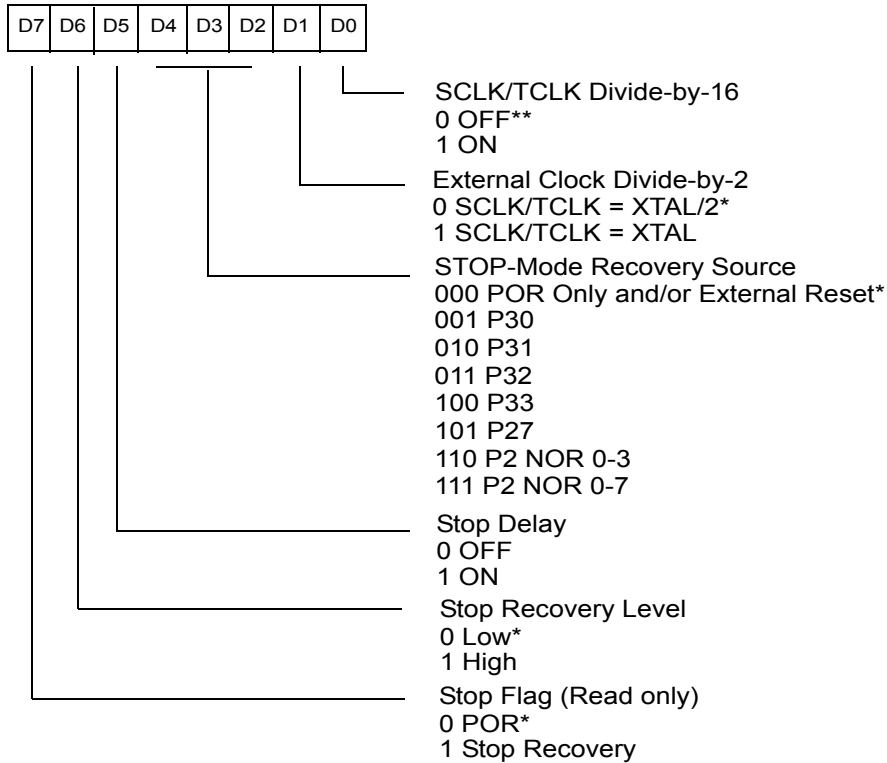
Note: The default setting is 10 ms.

WDT During HALT Mode (D2). This bit determines whether or not the WDT is active during HALT Mode. A “1” indicates that the WDT is active during HALT. A “0” disables the WDT in HALT Mode. The default value is “1”. **WDT During STOP Mode (D3).** This bit determines whether or not the WDT is active during STOP mode. A “1” indicates active during STOP. A “0” disables the WDT during STOP Mode. This is applicable only when the WDT clock source is the internal RC oscillator.

Clock Source For WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1, and the WDT is stopped in STOP Mode. The default configuration of this bit is 0, which selects the RC oscillator.

Permanent WDT. When this feature is enabled, the WDT is enabled after reset and will operate in Run and HALT Mode. The control bits in the WDTMR do not affect the WDT operation. If the clock source of the WDT is the internal RC oscillator, then the WDT will run in STOP mode. If the clock source of the WDT is the XTAL1 pin, then the WDT will not run in STOP mode.

SMR (Fh) 0B

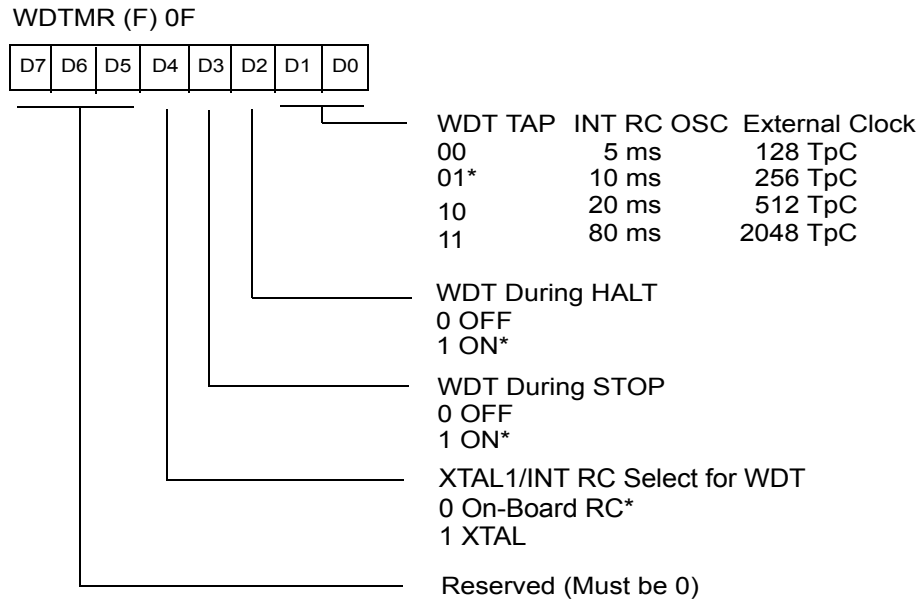


Note: Note used in conjunction with SMR2 Source

* Default setting after RESET

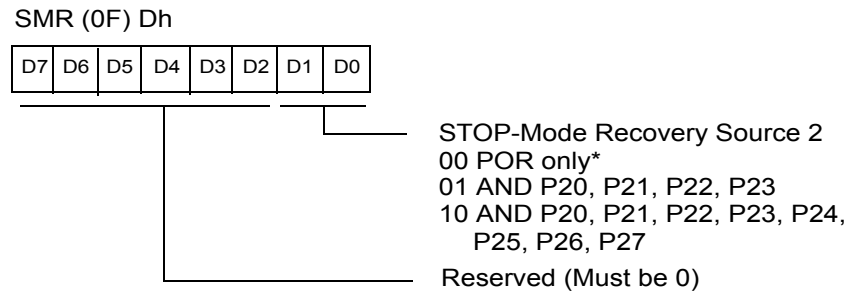
** Default setting after RESET and STOP-Mode Recovery

Figure 37. Stop Mode Recovery Register (Write Only Except Bit D7, Which is Read Only)



* Default setting after RESET

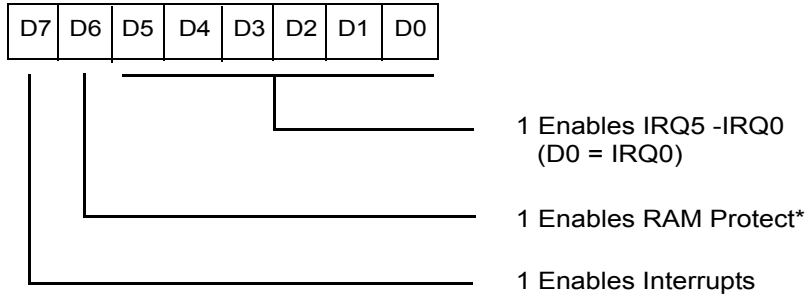
Figure 38. Watchdog Timer Mode Register (Write Only)



Note: Not used in conjunction with SMR Source

Figure 39. Stop Mode Recovery Register2 (Write Only)

R251 IMR



* This option must be selected when ROM code is submitted for ROM Masking, otherwise this control bit is disabled permanently

Figure 51. Interrupt Mask Register (FB_n: Read/Write)

R252 Flags

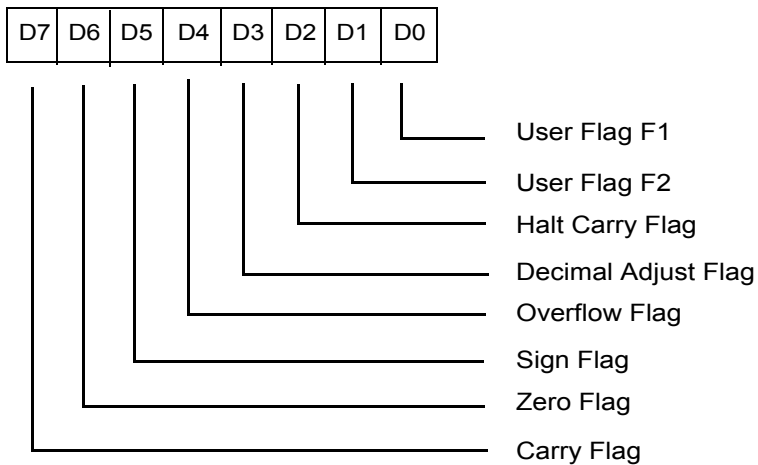
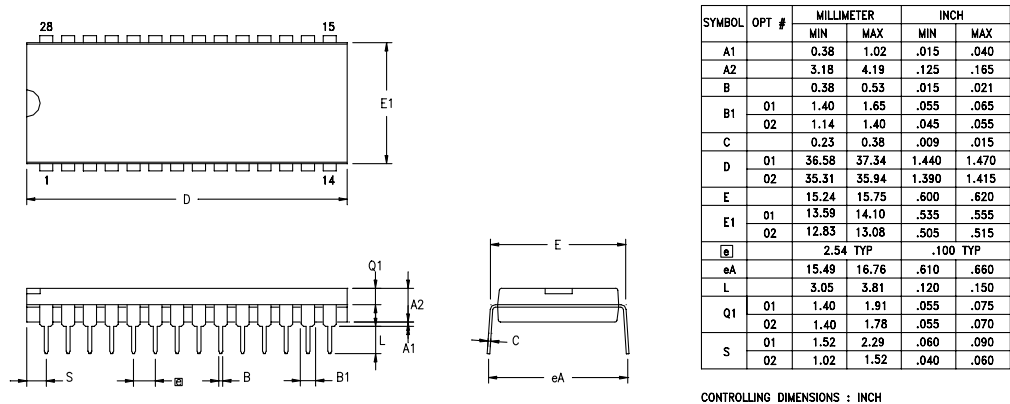


Figure 52. Flag Register (FC_n: Read/Write)



OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

Figure 58. 28-Pin DIP Package Diagram

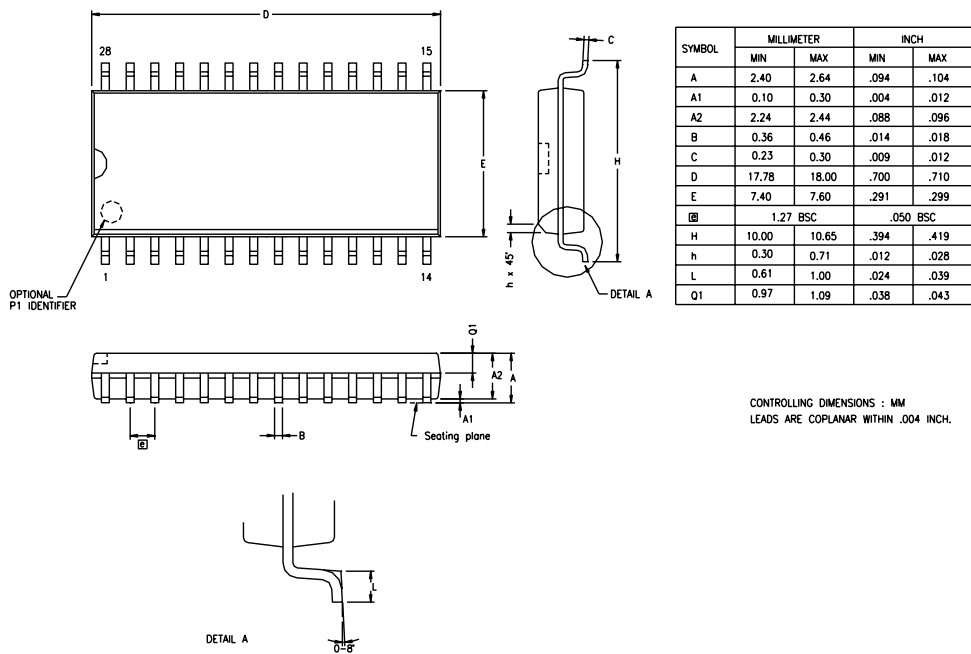


Figure 59. 28-Pin SOIC Package Diagram