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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	EBI/EMI
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e4412fsc00tr



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As used herein

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FS 507510**

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Table 1. Z86E33/733/E34, E43/743/E44 Features (Continued)

Device	ROM (KB)	RAM ¹ (Bytes)	I/O Lines	Speed (MHz)
Z86E44	16	236	32	12
¹ General-Purpose				

- Standard Temperature ($V_{CC} = 3.5 \text{ V to } 5.5 \text{ V}$)
- Extended Temperature ($V_{CC} = 3.5 \text{ V to } 5.5 \text{ V}$)
- Available Packages:
 - 28-Pin DIP/SOIC/PLCC OTP (E33/733/E34)
 - 40-Pin DIP OTP (E43/743/E44)
 - 44-Pin PLCC/LQFP OTP (E43/743/E44)
- Software Enabled Watchdog Timer (WDT)
- Push-Pull/Open-Drain Programmable on Port 0, Port 1, and Port 2
- 24/32 Input/Output Lines
- Clock-Free WDT Reset
- Auto Power-On Reset (POR)
- Programmable OTP Options:
 - RC Oscillator
 - EPROM Protect
 - Auto Latch Disable
 - Permanently Enabled WDT
 - Crystal Oscillator Feedback Resistor Disable
 - RAM Protect
- Low-Power Consumption: 60 mW
- Fast Instruction Pointer: 0.75 μs
- Two Standby Modes: STOP and HALT
- Digital Inputs CMOS Levels, Schmitt-Triggered
- Software Programmable Low EMI Mode
- Two Programmable 8-Bit Counter/Timers Each with a 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Six Different Sources
- Two Comparators

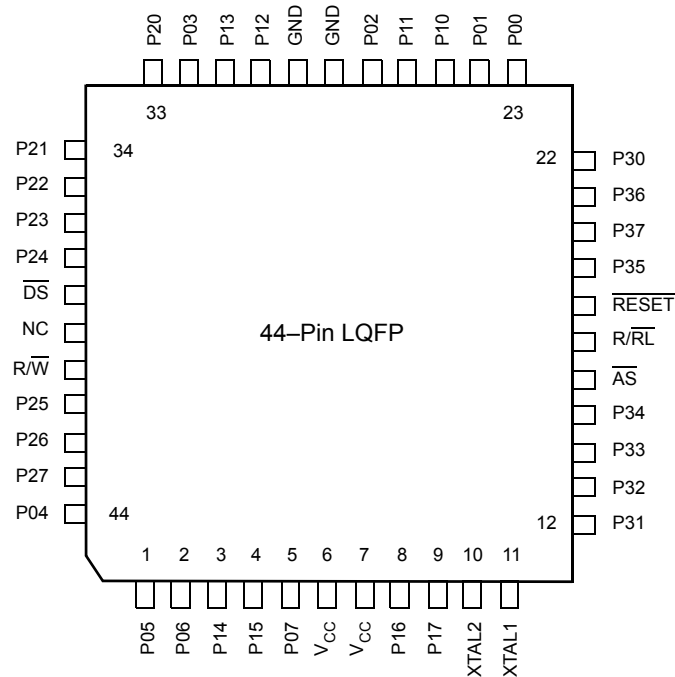


Figure 5. 44-Pin LQFP Pin Configuration Standard Mode

Table 4. 44-Pin LQFP Pin Identification

Pin No	Symbol	Function	Direction
1-2	P05-P06	Port 0, Pins 5,6	Input/Output
3-4	P14-P15	Port 1, Pins 4,5	Input/Output
5	P07	Port 0, Pin 7	Input/Output
6-7	V _{CC}	Power Supply	
8-9	P16-P17	Port 1, Pins 6,7	Input/Output
10	XTAL2	Crystal Oscillator	Output
11	XTAL1	Crystal Oscillator	Input
12-14	P31-P33	Port 3, Pins 1,2,3	Input
15	P34	Port 3, Pin 4	Output
16	AS	Address Strobe	Output
17	R//RL	ROM/ROMless select	Input

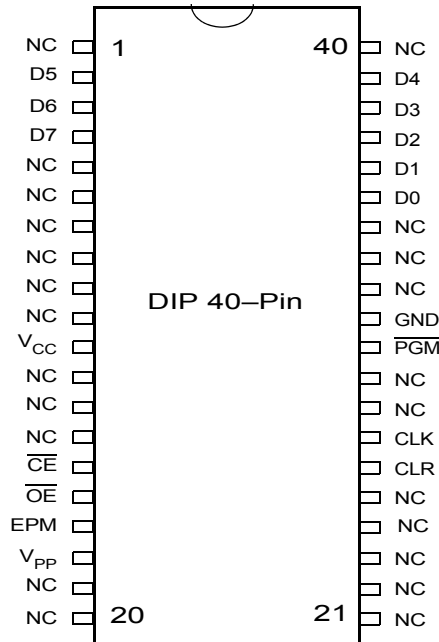


Figure 6. 40-Pin DIP Pin Configuration EPROM Mode

Table 5. 40-Pin DIP Package Pin Identification EPROM Mode

Pin No	Symbol	Function	Direction
1	NC	No Connection	
2-4	D5-D7	Data 5,6,7	Input/Output
5-10	NC	No Connection	
11	V _{CC}	Power Supply	
12-14	NC	No Connection	
15	CE	Chip Select	Input
16	OE	Output Enable	Input
17	EPM	EPROM Prog. Mode	Input
18	V _{PP}	Prog. Voltage	Input
19-25	NC	No Connection	
26	CLR	Clear	Input
27	CLK	Clock	Input
28-29	NC	No Connection	

Table 5. 40-Pin DIP Package Pin Identification EPROM Mode (Continued)

Pin No	Symbol	Function	Direction
30	/PGM	Prog. Mode	Input
31	GND	Ground	
32-34	NC	No Connection	
35-39	D0-D4	Data 0,1,2,3,4	Input/Output
40	NC	No Connection	

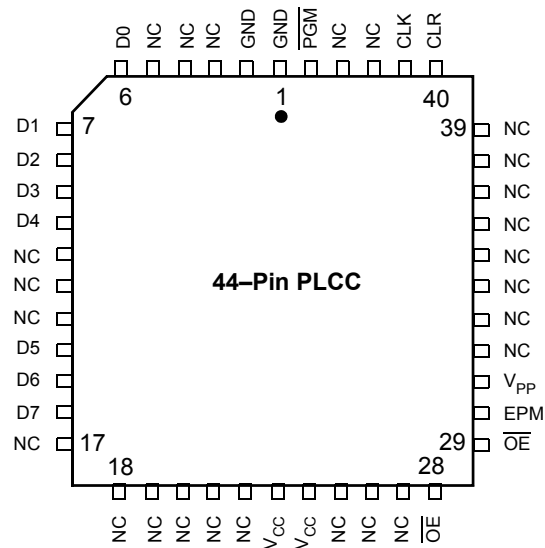


Figure 7. 44-Pin PLCC Pin Configuration EPROM Programming Mode

Table 6. 44-Pin PLCC Pin Configuration EPROM Programming Mode

Pin No	Symbol	Function	Direction
1-2	GND	Ground	
3-5	NC	No Connection	
6-10	D0-D4	Data 0,1,2,3,4	Input/Output
11-13	NC	No Connection	
14-16	D5-D7	Data 5,6,7	Input/Output
17-22	NC	No Connection	
23-24	V _{CC}	Power Supply	
25-27	NC	No Connection	
28	CE	Chip Select	Input
29	OE	Output Enable	Input
30	EPM	EPROM Prog. Mode	Input
31	V _{PP}	Prog. Voltage	Input

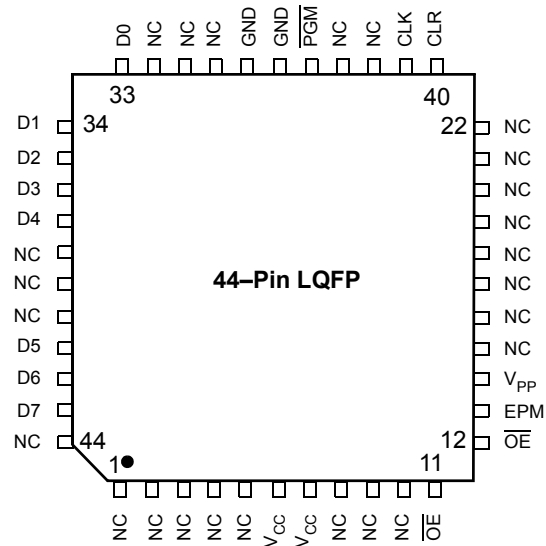


Figure 8. 44-Pin LQFP Pin Configuration EPROM Programming Mode

Table 7. 44-Pin LQFP Pin Identification EPROM Programming Mode

Pin No	Symbol	Function	Direction
1-5	NC	No Connection	
6-7	V _{CC}	Power Supply	
8-10	NC	No Connection	
11	CE	Chip Select	Input
12	OE	Output Enable	Input
13	EPM	EPROM Prog. Mode	Input
14	V _{PP}	Prog. Voltage	Input
15-22	NC	No Connection	
23	CLR	Clear	Input
24	CLK	Clock	Input
25-26	NC	No Connection	
27	/PGM	Prog. Mode	Input
28-29	GND	Ground	
30-32	NC	No Connection	

**Table 7. 44-Pin LQFP Pin Identification EPROM Programming Mode
(Continued)**

Pin No	Symbol	Function	Direction
33-37	D0-D4	Data 0,1,2,3,4	Input/Output
38-40	NC	No Connection	
41-43	D5-D7	Data 5,6,7	Input/Output
44	NC	No Connection	

Electrical Characteristics

Absolute Maximum Ratings

Table 10. Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
Ambient Temperature under Bias	−40	+105	C	
Storage Temperature	−65	+150	C	
Voltage on any Pin with Respect to V_{SS}	−0.6	+7	V	1
Voltage on V_{DD} Pin with Respect to V_{SS}	−0.3	+7	V	
Voltage on XTAL1, P32, P33 and \overline{RESET} Pins with Respect to V_{SS}	−0.6	$V_{DD}+1$	V	2
Total Power Dissipation		1.21	W	
Maximum Allowable Current out of V_{SS}		220	mA	
Maximum Allowable Current into V_{DD}		180	mA	
Maximum Allowable Current into an Input Pin	−600	+600	μA	3
Maximum Allowable Current into an Open-Drain Pin	−600	+600	μA	4
Maximum Allowable Output Current Sunk by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sourced by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sunk by \overline{RESET} Pin		3	mA	

Notes

1. This applies to all pins except XTAL pins and where otherwise noted.
2. There is no input protection diode from pin to V_{DD} .
3. This excludes XTAL pins.
4. Device pin is not at an output Low state.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

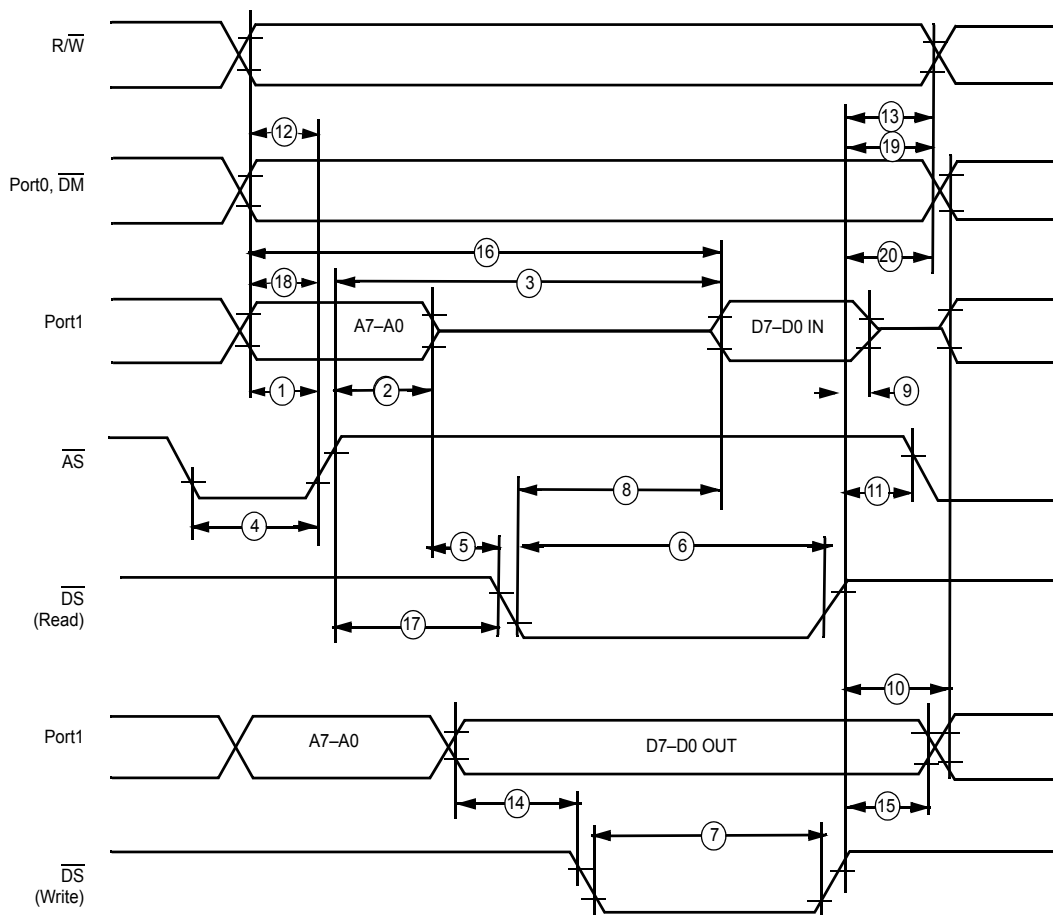


Figure 14. External I/O or Memory Read/Write Timing (Z86E43/743/E44 Only)

Table 13. DC Electrical Characteristics $T_A = 0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$, 12 MHz

No.	Symbol	Parameter	V_{CC}^1	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to \overline{AS} Rise Delay	3.5V	35		ns	2
			5.5V	35		ns	2
2	TdAS(A)	\overline{AS} Rise to Address Float Delay	3.5V	45		ns	2
			5.5V	45		ns	2
3	TdAS(DR)	\overline{AS} Rise to Read Data Req'd Valid	3.5V		250	ns	2,3
			5.5V		250	ns	2,3

Table 13. DC Electrical Characteristics $T_A = 0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$, 12 MHz (Continued)

No.	Symbol	Parameter	V_{CC}^1	Min	Max	Units	Notes
4	TwAS	\overline{AS} Low Width	3.5V	55		ns	2
			5.5V	55		ns	2
5	TdAS(DS)	Address Float to \overline{DS} Fall	3.5V	0		ns	
			5.5V	0		ns	
6	TwDSR	\overline{DS} (Read) Low Width	3.5V	200		ns	2,3
			5.5V	200		ns	2,3
7	TwDSW	\overline{DS} (Write) Low Width	3.5V	110		ns	2,3
			5.5V	110		ns	2,3
8	TdDSR(DR)	\overline{DS} Fail to Read Data Req'd Valid	3.5V		150	ns	2,3
			5.5V		150	ns	2,3
9	ThDR(DS)	Read Data to \overline{DS} Rise Hold Time	3.5V	0		ns	2
			5.5V	0		ns	2
10	TdDS(A)	\overline{DS} Rise to Address Active Delay	3.5V	45		ns	2
			5.5V	55		ns	2
11	TdDS(AS)	\overline{DS} Rise to \overline{AS} Fall Delay	3.5V	30		ns	2
			5.5V	45		ns	2
12	TdR/W(AS)	R/\overline{W} Valid to \overline{AS} Rise Delay	3.5V	45		ns	2
			5.5V	45		ns	2
13	TdDS(R/W)	\overline{DS} Rise to R/\overline{W} Not Valid	3.5V	45		ns	2
			5.5V	45		ns	2
14	TdDW(DSW)	Write Data Valid to \overline{DS} Fall (Write) Delay	3.5V	55		ns	2
			5.5V	55		ns	2
15	TdDS(DW)	\overline{DS} Rise to Write Data Not Valid Delay	3.5V	45		ns	2
			5.5V	55		ns	2
16	TdA(DR)	Address Valid to Read Data Req'd Valid	3.5V		310	ns	2,3
			5.5V		310	ns	2,3
17	TdAS(DS)	\overline{AS} Rise to \overline{DS} Fall Delay	3.5V	65		ns	2
			5.5V	65		ns	2

Table 14. DC Electrical Characteristics $T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$, 12 MHz (Continued)

No.	Symbol	Parameter	V_{CC}^1	Min	Max	Units	Notes
10	TdDS(A)	\overline{DS} Rise to Address Active Delay	4.5V	45		ns	2
			5.5V	55		ns	2
11	TdDS(AS)	\overline{DS} Rise to \overline{AS} Fall Delay	4.5V	45		ns	2
			5.5V	45		ns	2
12	TdR/W(AS)	R/\overline{W} Valid to \overline{AS} Rise Delay	4.5V	45		ns	2
			5.5V	45		ns	2
13	TdDS(R/W)	\overline{DS} Rise to R/\overline{W} Not Valid	4.5V	45		ns	2
			5.5V	45		ns	2
14	TdDW(DSW)	Write Data Valid to \overline{DS} Fall (Write) Delay	4.5V	55		ns	2
			5.5V	55		ns	2
15	TdDS(DW)	\overline{DS} Rise to Write Data Not Valid Delay	4.5V	55		ns	2
			5.5V	55		ns	2
16	TdA(DR)	Address Valid to Read Data Req'd Valid	4.5V		310	ns	2,3
			5.5V		310	ns	2,3
17	TdAS(DS)	\overline{AS} Rise to \overline{DS} Fall Delay	4.5V	65		ns	2
			5.5V	65		ns	2
18	TdDM(AS)	\overline{DM} Valid to \overline{AS} Rise Delay	4.5V	35		ns	2
			5.5V	35		ns	2
19	ThDS(AS)	\overline{DS} Valid to Address Valid Hold Time	4.5V	35		ns	2
			5.5V	35		ns	2

Notes

1. The V_{CC} voltage specification of 5.5 V guarantees $5.0\text{ V} \pm 0.5\text{ V}$ and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V.
2. Timing numbers given are for minimum T_{pC} .
3. When using extended memory timing, add 2 T_{pC} .

Standard Test Load

All timing references use $0.7\text{ }V_{CC}$ for a logic 1 and $0.2\text{ }V_{CC}$ for a logic 0.

For Standard Mode (not Low-EMI Mode for outputs) with SMR, $D1 = 0$, $D0 = 0$.

Handshake Timing Diagrams

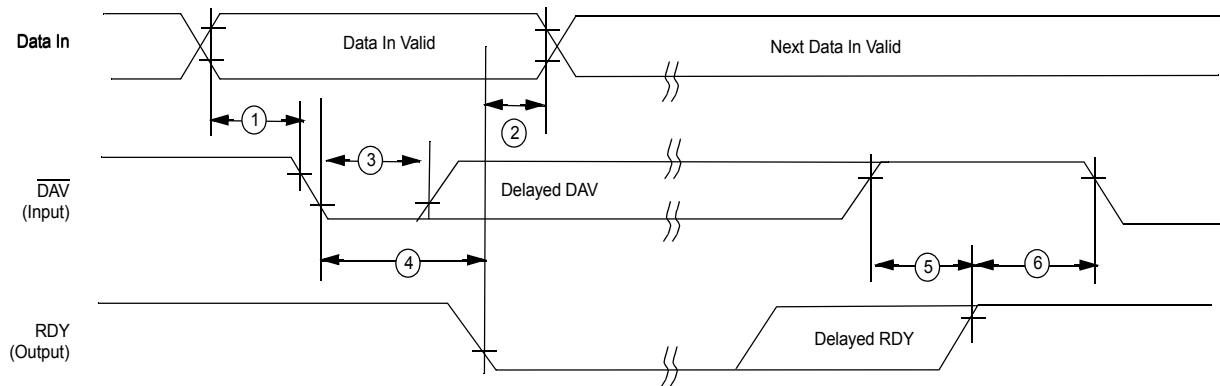


Figure 16. Input Handshake Timing

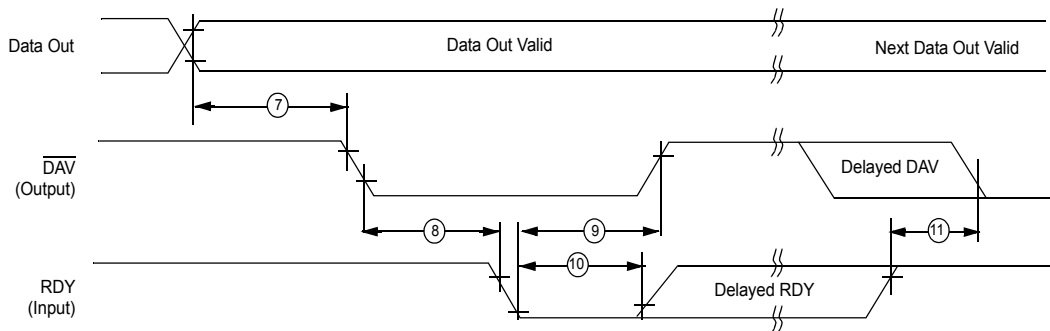


Figure 17. Output Handshake Timing

Table 17. Additional Timing Table (Divide by Two Mode) $T_A = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}$

No	Symbol	Parameter	V_{CC}^1	Min	Max	Min	Max	Units	Conditions	Notes
1	TpC	Input Clock Period	3.5V	62.5	DC	250	DC	ns		2,6,4
			5.5V	62.5	DC	250	DC	ns		2,6,4
2	TrC,TfC	Clock Input Rise & Fall Times	3.5V		15		25	ns		2,6,4
			5.5V		15		25	ns		2,6,4
3	TwC	Input Clock Width	3.5V	31		31		ns		2,6,4
			5.5V	31		31		ns		2,6,4

RAM Protect. The upper portion of the RAM's address spaces 80h to EFh (excluding the control registers) can be protected from reading and writing. This option can be selected during the EPROM Programming Mode. After this option is selected, the user can activate this feature from the internal EPROM. D6 of the IMR control register (R251) is used to turn off/on the RAM protect by loading a 0 or 1, respectively. A "1" in D6 indicates RAM Protect enabled.

Stack. The Z86E43/743/E44 external data memory or the internal register file can be used for the stack. The 16-bit Stack Pointer (R254-R255) is used for the external stack, which can reside anywhere in the data memory for ROMless mode, but only from 4096/8192/16384 to 65535 in ROM mode. An 8-bit Stack Pointer (R255) is used for the internal stack on the Z8 that resides within the 236 general-purpose registers (R4-R239). SPH (R254) can be used as a general-purpose register when using internal stack only. R254 and R255 are set to 00H after any reset or Stop Mode Recovery.

Counter/Timers. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The Ti prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (see [Figure 27](#)).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256), that has been loaded into the counter. When the counter reaches the end of count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counters can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching one (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, can be read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3 line P36 serves as a timer output (T_{OUT}) through which T0, T1, or the internal clock can be output. The counter/timers can be cascaded by connecting the T0 output to the input of T1.

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority Register (IPR). An interrupt machine cycle is activated when an interrupt request is granted. Thus, disabling all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests need service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling or both edge triggered, and are programmable by the user. The software may poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in bits D7 and D6 of the IRQ Register (R250). The configuration is shown in [Table 21](#).

Table 21. IRQ Register Configuration

IRO		Interrupt Edge	
D7	D6	P31	P32
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes

1. F = Falling Edge
2. R = Rising Edge

Clock. The on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, RC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 10 kHz to 16 MHz max, with a series resistance (RS) less than or equal to 100 Ω .

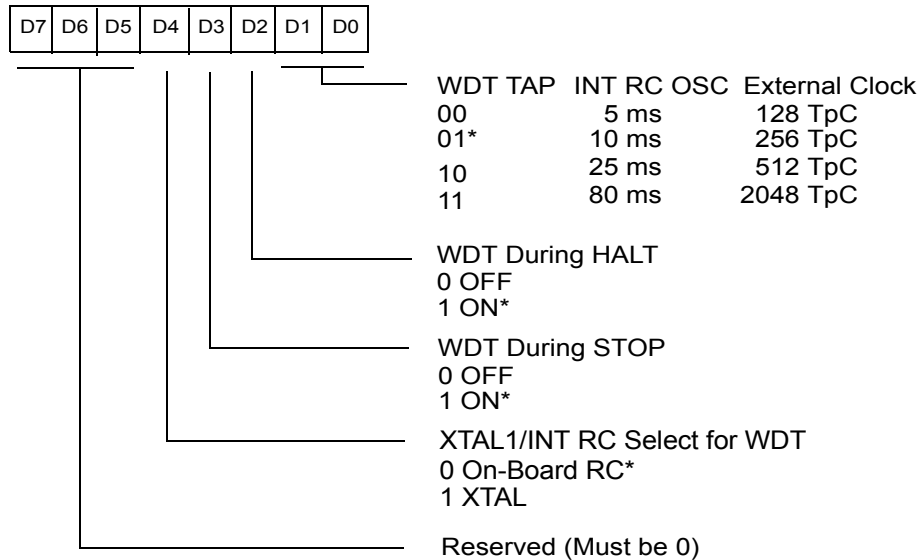
The crystal should be connected across XTAL1 and XTAL2 using the vendor's recommended capacitor values from each pin directly to device pin Ground. The RC oscillator option can be selected in the programming mode. The RC oscillator configuration must be an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to Ground ([Table 29](#)).

► **Note:** *WDT time-out in STOP Mode will not reset SMR, SMR2, PCON, WDTMR, P2M, P3M, Ports 2 & 3 Data Registers, but will activate the T_{POR} delay.*

WDTMR Register Accessibility. The WDTMR register is accessible only during the first 60 internal system clock cycles from the execution of the first instruction after Power-On Reset, Watchdog reset or a Stop Mode Recovery (Figure 33 and Figure 34). After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register File at address location 0Fh.

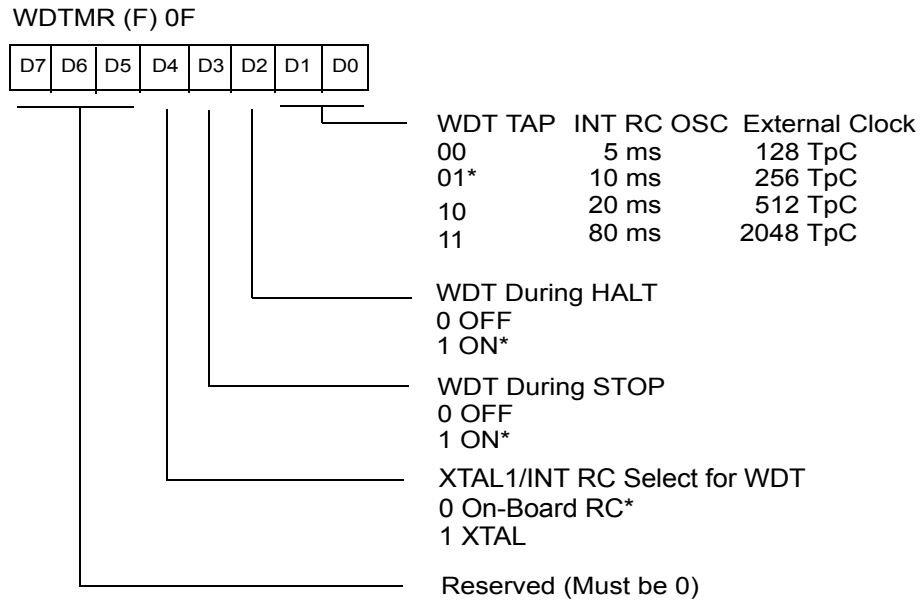
Clock Free WDT Reset. The WDT will enable the Z8 to reset the I/O pins whenever the WDT times out, even without a clock source running on the XTAL1 and XTAL2 pins. WDTMR Bit D4 must be 0 for the clock Free WDT to work. The I/O pins will default to their default settings.

WDTMR (F) 0F



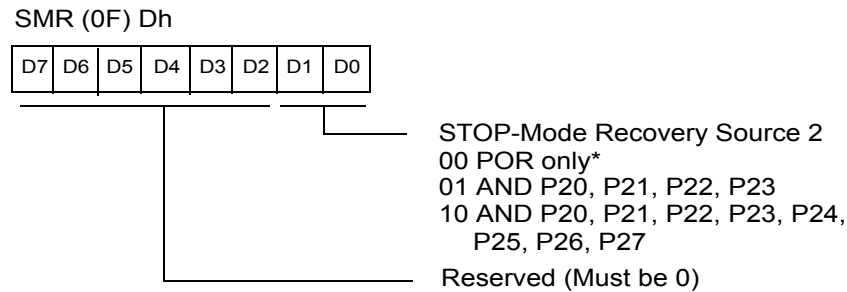
* Default setting after RESET

Figure 33. Watchdog Timer Mode Register Write Only



* Default setting after RESET

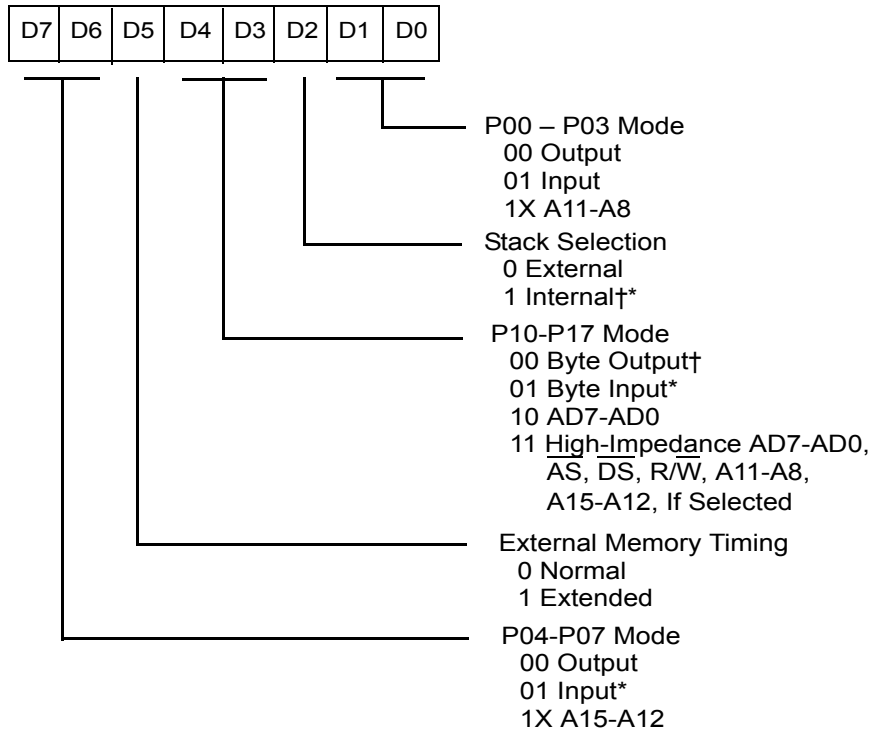
Figure 38. Watchdog Timer Mode Register (Write Only)



Note: Not used in conjunction with SMR Source

Figure 39. Stop Mode Recovery Register2 (Write Only)

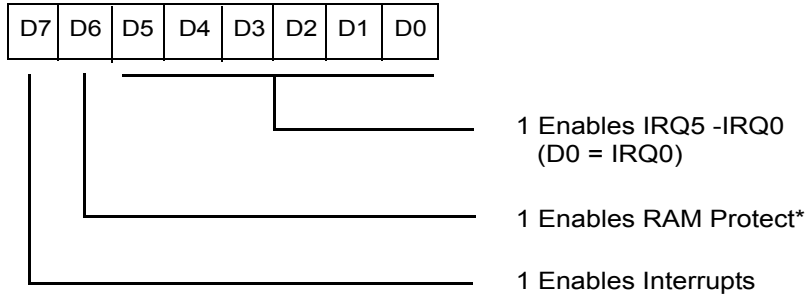
R248 P01M



Reset Condition = 0100 1101B
For ROMless Condition = 1011 0110B
† Z86E33/733/E34 Must be 00
* Default after Reset

Figure 48. Port 0 and 1 Mode Register (F8_h: Write Only)

R251 IMR



* This option must be selected when ROM code is submitted for ROM Masking, otherwise this control bit is disabled permanently

Figure 51. Interrupt Mask Register (FB_n: Read/Write)

R252 Flags

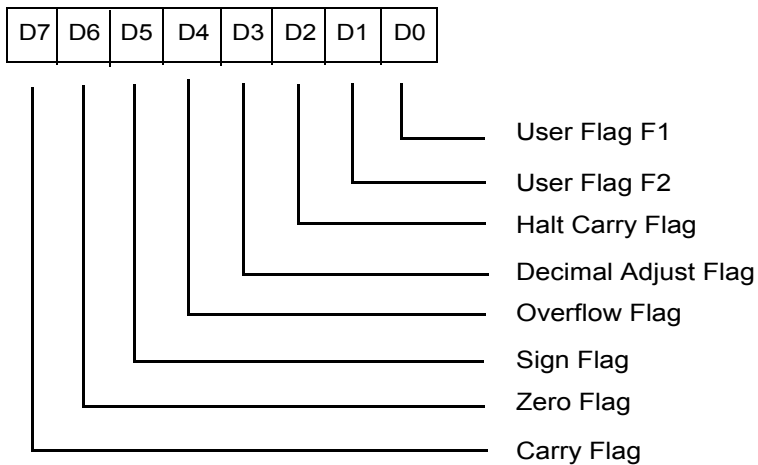


Figure 52. Flag Register (FC_n: Read/Write)

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