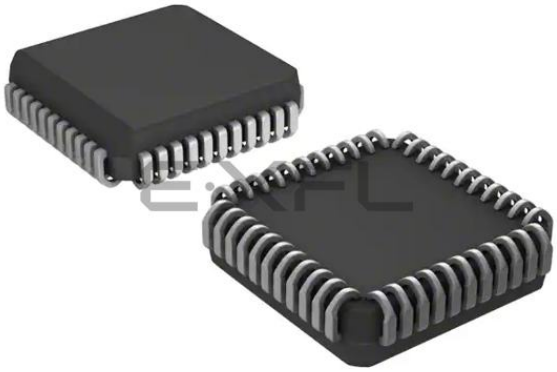

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	EBI/EMI
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e4412vsc

Table 1. Z86E33/733/E34, E43/743/E44 Features (Continued)

Device	ROM (KB)	RAM[1] (Bytes)	I/O Lines	Speed (MHz)
Z86E44	16	236	32	12

[1]General-Purpose

- Standard Temperature (V_{CC} = 3.5 V to 5.5 V)
- Extended Temperature (V_{CC} = 3.5 V to 5.5 V)
- Available Packages:
  - 28-Pin DIP/SOIC/PLCC OTP (E33/733/E34)
  - 40-Pin DIP OTP (E43/743/E44)
  - 44-Pin PLCC/LQFP OTP (E43/743/E44)
- Software Enabled Watchdog Timer (WDT)
- Push-Pull/Open-Drain Programmable on Port 0, Port 1, and Port 2
- 24/32 Input/Output Lines
- Clock-Free WDT Reset
- Auto Power-On Reset (POR)
- Programmable OTP Options:
  - RC Oscillator
  - EPROM Protect
  - Auto Latch Disable
  - Permanently Enabled WDT
  - Crystal Oscillator Feedback Resistor Disable
  - RAM Protect
- Low-Power Consumption: 60 mW
- Fast Instruction Pointer: 0.75 µs
- Two Standby Modes: STOP and HALT
- Digital Inputs CMOS Levels, Schmitt-Triggered
- Software Programmable Low EMI Mode
- Two Programmable 8-Bit Counter/Timers Each with a 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Six Different Sources
- Two Comparators

- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive

Functional Block Diagram

Figure 1 displays the functional block diagram.

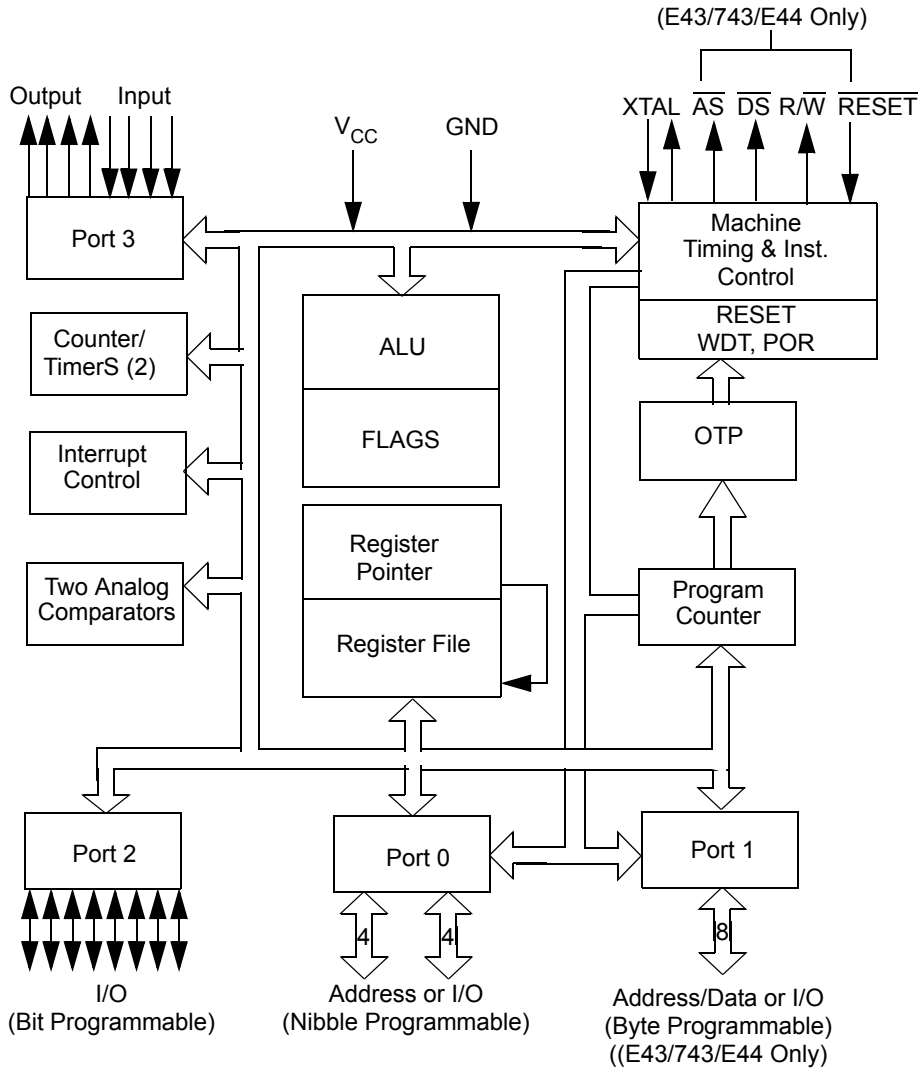


Figure 1. Functional Block Diagram

Table 2. 40-Pin DIP Pin Identification Standard Mode (Continued)

Pin No	Symbol	Function	Direction
15	XTAL1	Crystal Oscillator	Input
16-18	P31-P33	Port 3, Pins 1,2,3	Input
19	P34	Port 3, Pin 4	Output
20	AS	Address Strobe	Output
21	RESET	Reset	Input
22	P35	Port 3, Pin 5	Output
23	P37	Port 3, Pin 7	Output
24	P36	Port 3, Pin 6	Output
25	P30	Port 3, Pin 0	Input
26-27	P00-P01	Port 0, Pins 0,1	Input/Output
28-29	P10-P11	Port 1, Pins 0,1	Input/Output
30	P02	Port 0, Pin 2	Input/Output
31	GND	Ground	
32-33	P12-P13	Port 1, Pins 2,3	Input/Output
34	P03	Port 0, Pin 3	Input/Output
35-39	P20-P24	Port 2, Pins 0, 1,2,3,4	Input/Output
40	DS	Data Strobe	Output

Table 6. 44-Pin PLCC Pin Configuration EPROM Programming Mode (Continued)

Pin No	Symbol	Function	Direction
32-39	NC	No Connection	
40	CLR	Clear	Input
41	CLK	Clock	Input
42-43	NC	No Connection	
44	/PGM	Prog. Mode	Input

Table 7. 44-Pin LQFP Pin Identification EPROM Programming Mode (Continued)

Pin No	Symbol	Function	Direction
33-37	D0-D4	Data 0,1,2,3,4	Input/Output
38-40	NC	No Connection	
41-43	D5-D7	Data 5,6,7	Input/Output
44	NC	No Connection	

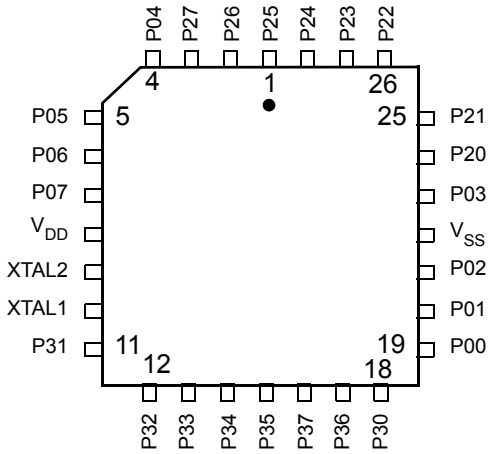


Figure 10. Standard Mode 28-Pin PLCC Pin Configuration

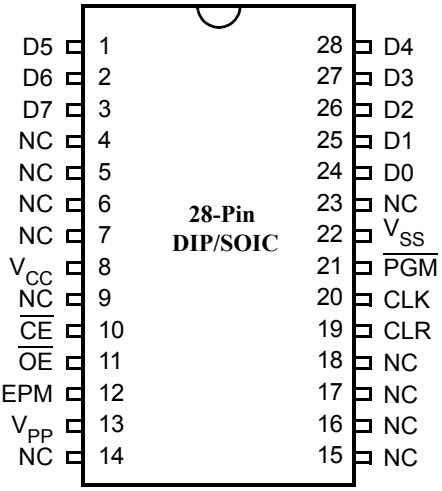


Figure 11. EPROM Programming Mode 28-Pin DIP/SOIC Pin Configuration

Table 12. DC Electrical Characteristics T_A= -40 °C to +105 °C (Continued)

Symbol	Parameter	V_{CC} [1]	Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{OH1}	Output High Voltage	4.5V	V_{CC} -0.4		4.8	V	I_{OH} = -2.0 mA	2
		5.5V	V_{CC} -0.4		4.8	V	I_{OH} = -2.0 mA	2
V_{OL}	Output Low Voltage Low EMI Mode	4.5V		0.4	0.2	V	I_{OL} = 1.0 mA	
		5.5V		0.4	0.2	V	I_{OL} = 1.0 mA	
V_{OL1}	Output Low Voltage	4.5V		0.4	0.1	V	I_{OL} = +4.0 mA	2
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	2
V_{OL2}	Output Low Voltage	4.5V		1.2	0.5	V	I_{OL} = +12 mA	2
		5.5V		1.2	0.5	V	I_{OL} = +12 mA	2
V_{RH}	Reset Input High Voltage	4.5V	.8 V_{CC}	V_{CC}	1.7	V		3
		5.5V	.8 V_{CC}	V_{CC}	2.1	V		3
V_{OLR}	Reset Output Low Voltage	4.5V		0.6	0.3	V	I_{OL} = 1.0 mA	3
		5.5V		0.6	0.2	V	I_{OL} = 1.0 mA	3
V_{OFFSET}	Comparator Input Offset Voltage	4.5V		25	10	mV		
		5.5V		25	10	mV		
V_{ICR}	Input Common Mode Voltage Range	4.5V	0	V_{CC} -1.5V		V		4
		5.5V	0	V_{CC} -1.5V		V		4
I_{IL}	Input Leakage	4.5V	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	4.5V	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	4.5V	-18	-180	-112	µA		3
		5.5V	-18	-180	-112	µA		3
I_{CC}	Supply Current	4.5V		20	15	mA	@ 12 MHz	5,6
		5.5V		20	15	mA	@ 12 MHz	5,6
I_{CC1}	Standby Current HALT Mode	4.5V		6	2	mA	V_{IN} = 0V, V_{CC} @ 12 MHz	5,6
		5.5V		6	4	mA	V_{IN} = 0V, V_{CC} @ 12 MHz	5,6

Handshake Timing Diagrams

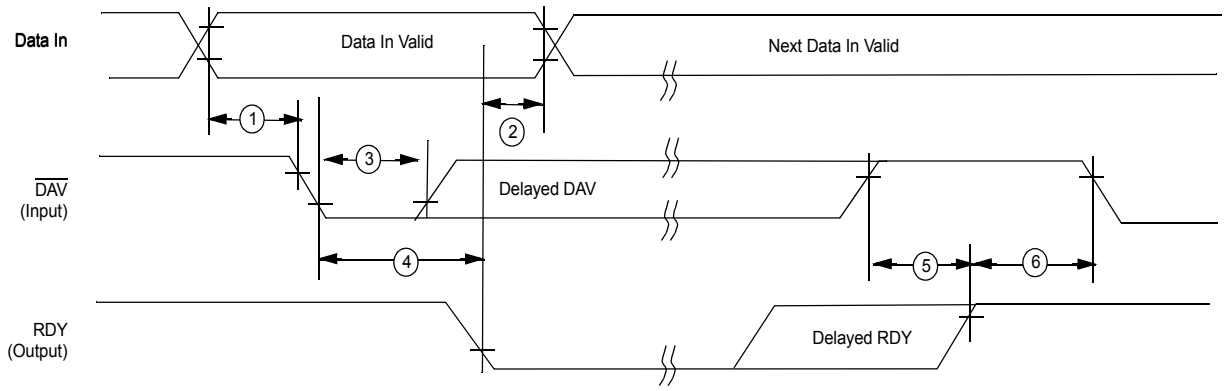


Figure 16. Input Handshake Timing

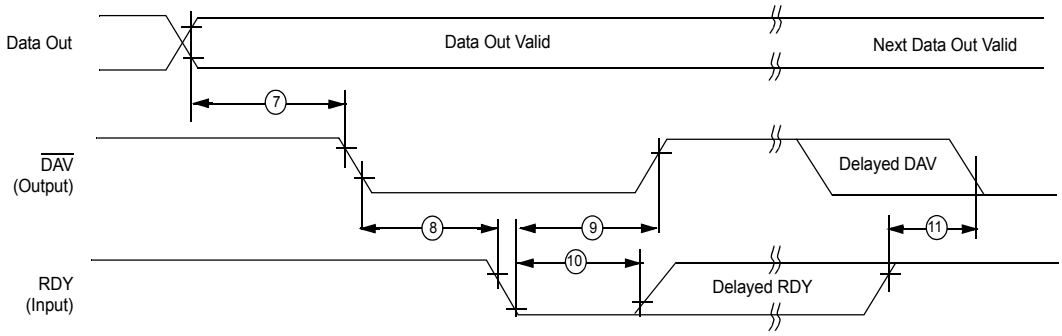


Figure 17. Output Handshake Timing

Table 17. Additional Timing Table (Divide by Two Mode) T_A = 0 °C to +70 °C

No	Symbol	Parameter	V_{CC}[1]	Min	Max	Min	Max	Units	Conditions	Notes
1	TpC	Input Clock Period	3.5V	62.5	DC	250	DC	ns		2,6,4
			5.5V	62.5	DC	250	DC	ns		2,6,4
2	TrC,TfC	Clock Input Rise & Fall Times	3.5V		15		25	ns		2,6,4
			5.5V		15		25	ns		2,6,4
3	TwC	Input Clock Width	3.5V	31		31		ns		2,6,4
			5.5V	31		31		ns		2,6,4

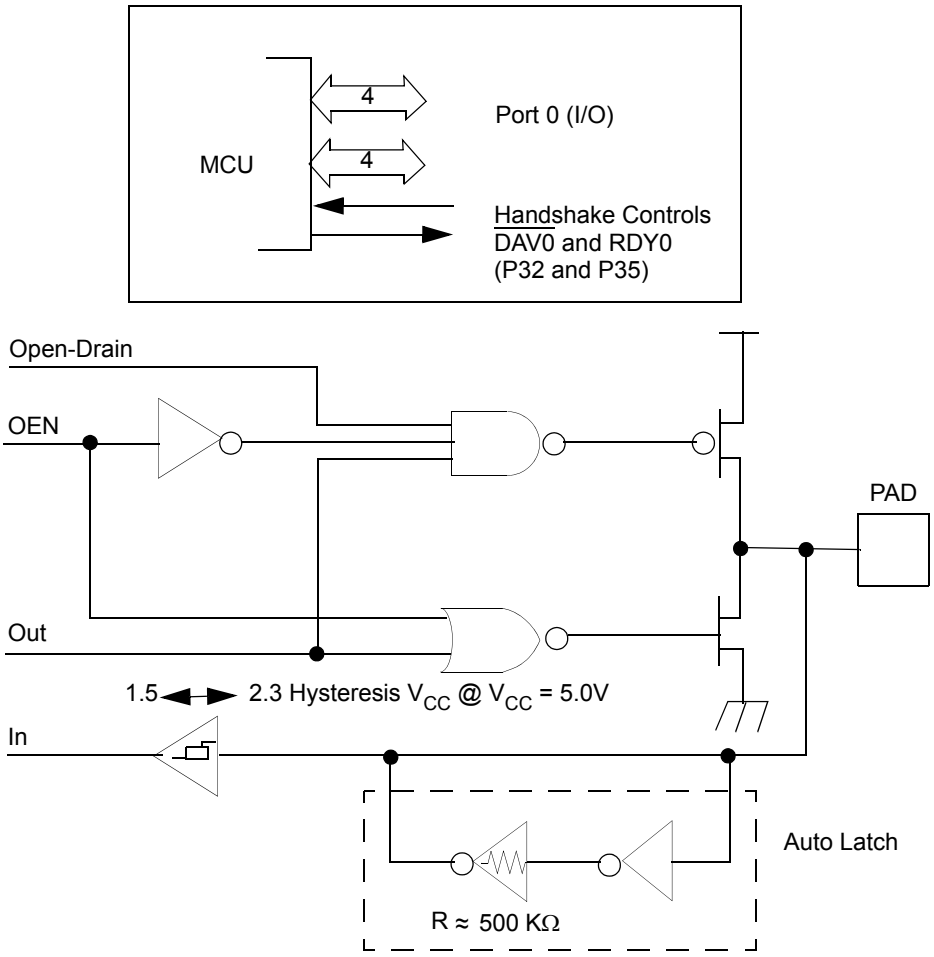


Figure 18. Port 0 Configuration

Port 1 (P17-P10). Port 1 is an 8-bit, bidirectional, CMOS-compatible port with multiplexed Address (A7-A0) and Data (D7-D0) ports. These eight I/O lines can be programmed as inputs or outputs or can be configured under software control as an Address/Data port for interfacing external memory. The input buffers are Schmitt-triggered and the output buffers can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 1 can be placed under handshake control. In this configuration, Port 3, lines P33 and P34 are used as the handshake controls RDY1 and $\overline{\text{DAV1}}$ (Ready and Data Available). To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 outputs the additional lines (see Figure 19).

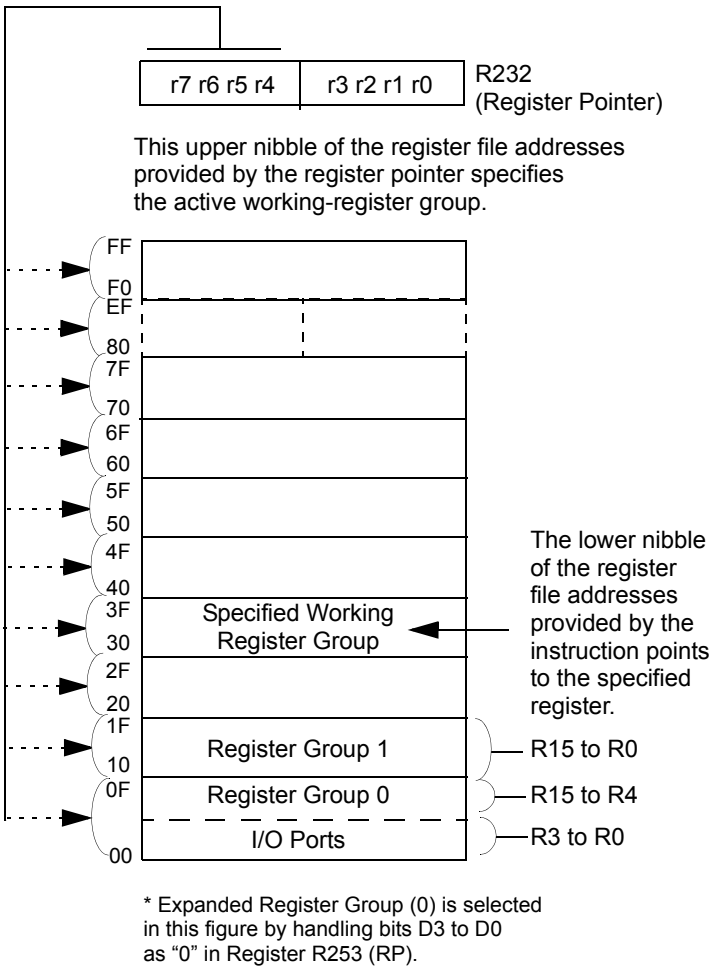


Figure 25. Register Pointer

RAM Protect. The upper portion of the RAM's address spaces 80h to EFh (excluding the control registers) can be protected from reading and writing. This option can be selected during the EPROM Programming Mode. After this option is selected, the user can activate this feature from the internal EPROM. D6 of the IMR control register (R251) is used to turn off/on the RAM protect by loading a 0 or 1, respectively. A "1" in D6 indicates RAM Protect enabled.

Stack. The Z86E43/743/E44 external data memory or the internal register file can be used for the stack. The 16-bit Stack Pointer (R254-R255) is used for the external stack, which can reside anywhere in the data memory for ROMless mode, but only from 4096/8192/16384 to 65535 in ROM mode. An 8-bit Stack Pointer (R255) is used for the internal stack on the Z8 that resides within the 236 general-purpose registers (R4-R239). SPH (R254) can be used as a general-purpose register when using internal stack only. R254 and R255 are set to 00H after any reset or Stop Mode Recovery.

Counter/Timers. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The Ti prescaler is driven by internal or external clock sources; however, the TO prescaler is driven by the internal clock only (see Figure 27).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256), that has been loaded into the counter. When the counter reaches the end of count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counters can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching one (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, can be read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3 line P36 serves as a timer output (T_{OUT}) through which T0, T1, or the internal clock can be output. The counter/timers can be cascaded by connecting the T0 output to the input of T1.

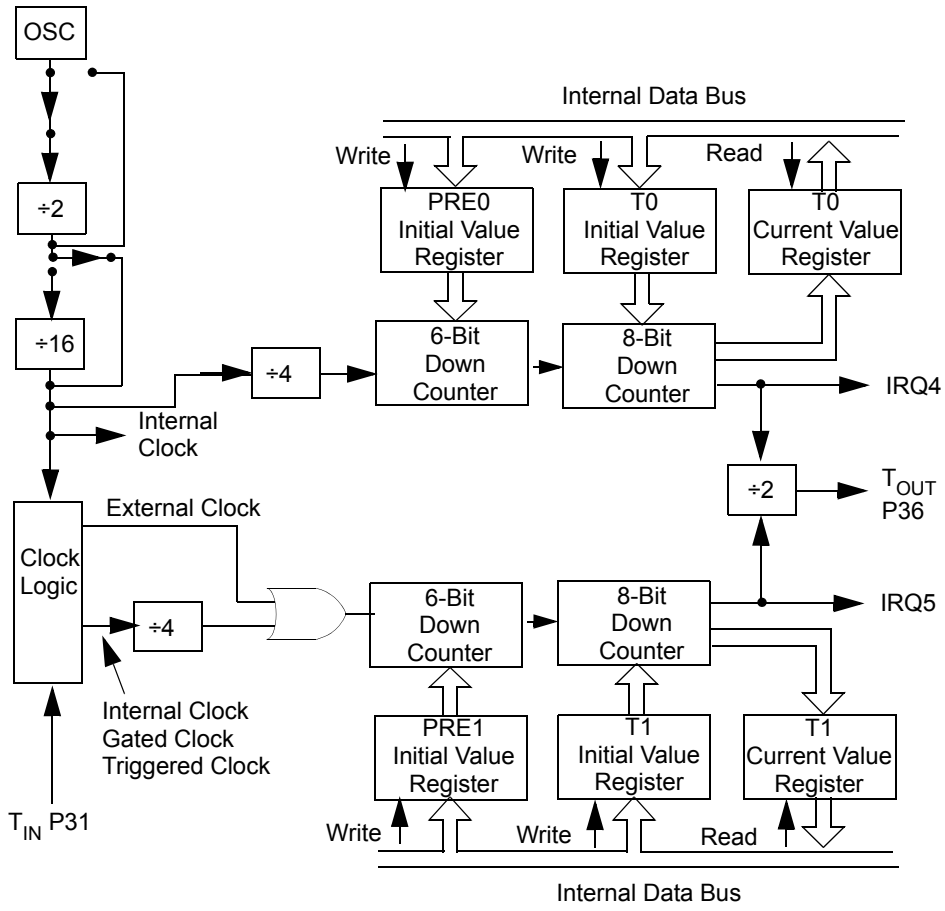


Figure 27. Counter/Timer Block Diagram

Interrupts. The MCU has six different interrupts from six different sources. The interrupts are maskable and prioritized (Figure 28). The six sources are divided as follows: four sources are claimed by Port 3 lines P33-P30) and two in counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 20).

Comparator Output Port 3 (D0). Bit 0 controls the comparator output in Port 3. A "1" in this location brings the comparator outputs to P34 and P37, and a "0" releases the Port to its standard I/O configuration. The default value is 0.

Port 1 Open-Drain (D1). Port 1 can be configured as an open-drain by resetting this bit (D1=0) or configured as push-pull active by setting this bit (D1=1). The default value is 1.

Port 0 Open-Drain (D2). Port 0 can be configured as an open-drain by resetting this bit (D2=0) or configured as push-pull active by setting this bit (D2=1). The default value is 1.

Low EMI Port 0 (D3). Port 0 can be configured as a Low EMI Port by resetting this bit (D3=0) or configured as a Standard Port by setting this bit (D3=1). The default value is 1.

Low EMI Port 1 (D4). Port 1 can be configured as a Low EMI Port by resetting this bit (D4=0) or configured as a Standard Port by setting this bit (D4=1). The default value is 1.

Note: *The emulator does not support Port 1 low EMI mode and must be set D4 = 1.*

Low EMI Port 2 (D5). Port 2 can be configured as a Low EMI Port by resetting this bit (D5=0) or configured as a Standard Port by setting this bit (D5=1). The default value is 1.

Low EMI Port 3 (D6). Port 3 can be configured as a Low EMI Port by resetting this bit (D6=0) or configured as a Standard Port by setting this bit (D6=1). The default value is 1.

Low EMI OSC (D7). This bit of the PCON Register controls the low EMI noise oscillator. A "1" in this location configures the oscillator with standard drive. While a "0" configures the oscillator with low noise drive, however, it does not affect the relationship of SCLK and XTAL. The low EMI mode will reduce the drive of the oscillator (OSC). The default value is 1.

Note: *4 MHz is the maximum external clock frequency when running in the low EMI oscillator mode.*

Stop-Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of Stop Mode Recovery (Figure 31). All bits are Write Only except bit 7 which is a Read Only. Bit 7 is a flag bit that is hardware set on the condition of STOP Recovery and reset by a power-on cycle. Bit 6 controls whether a low or high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4 of the SMR register specify the Stop Mode Recovery Source. The SMR is located in Bank F of the Expanded Register File at address 0BH.

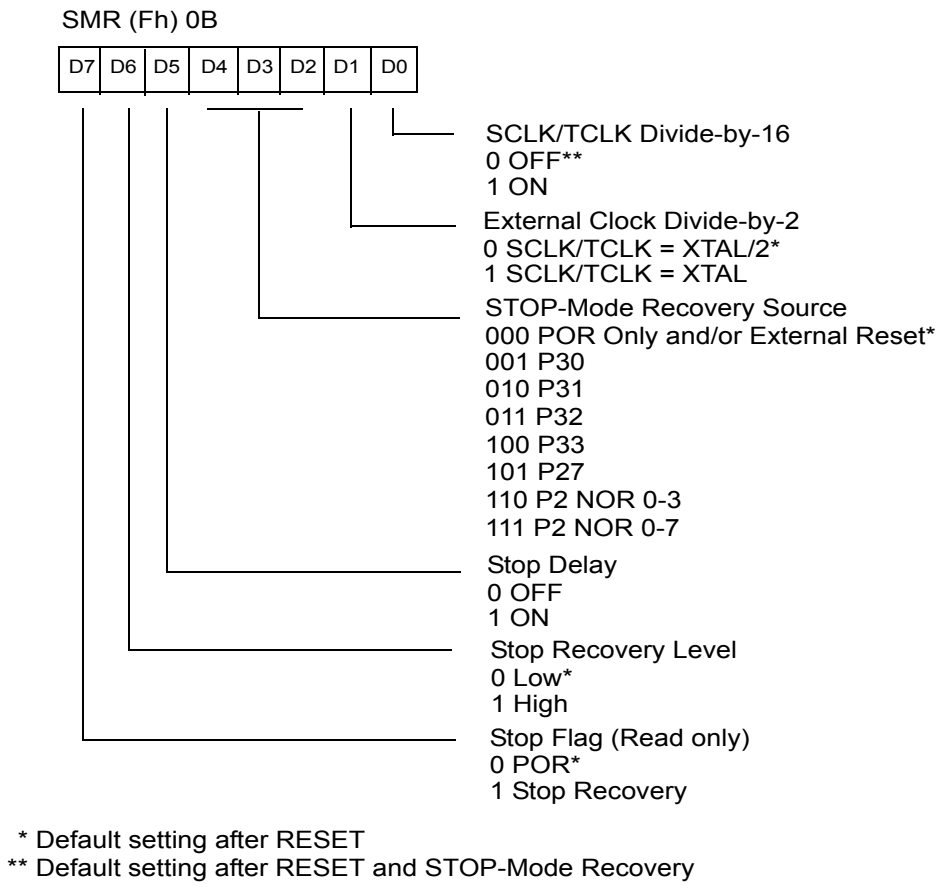


Figure 31. Stop Mode Recovery Register (Write-Only Except Bit D7, Which Is Read-Only)

SCLK/TCLK Divide-by-16 Select (D0). This bit of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources counter/timers and interrupt logic).

External Clock Divide-by-Two (D1). This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, the System Clock (SCLK) and Timer Clock (TCLK) are equal to the external clock frequency divided by two. The SCLK/TCLK is equal to the external clock frequency when this bit is set (D1=1). Using this bit together with D7 of PCON further helps lower EMI (that is, D7 (PCON) = 0, D1 (SMR) = 1). The default setting is zero.

Stop Mode Recovery Source (D2, D3, and D4). These three bits of the SMR register specify the wake up source of the Stop Mode Recovery (Figure 32). Table 22 shows the SMR source selected with the setting of D2 to D4. P33-P31 cannot be used to wake up

Table 22. Stop Mode Recovery Source

D4	D3	D2	SMR Source selection
0	0	0	POR recovery only
0	0	1	P30 transition
0	1	0	P31 transition (Not in analog mode)
0	1	1	P32 transition (Not in analog mode)
1	0	0	P33 transition (Not in analog mode)
1	0	1	P27 transition
1	1	0	Logical NOR of Port 2 bits 0-3
1	1	1	Logical NOR of Port 2 bits 0-7

Stop Mode Recovery Delay Select (D5). The 5 ms RESET delay after Stop Mode Recovery is disabled by programming this bit to a zero. A "1" in this bit will cause a 5 ms RESET delay after Stop Mode Recovery. The default condition of this bit is 1. If the fast wake up mode is selected, the Stop Mode Recovery source needs to be kept active for at least 5TpC.

Stop Mode Recovery Level Select (D6). A "1" in this bit defines that a high level on any one of the recovery sources wakes the MCU from STOP Mode. A 0 defines low level recovery. The default value is 0.

Cold or Warm Start (D7). This bit is set by the device upon entering STOP Mode. A "0" in this bit indicates that the device has been reset by POR (cold). A "1" in this bit indicates the device was awakened by a SMR source (warm).

Stop Mode Recovery Register 2 (SMR2). This register contains additional Stop Mode Recovery sources. When the Stop Mode Recovery sources are selected in this register then SMR Register Bits D2, D3, and D4 must be 0.

SMR:10		Operation
D1	DO	Description of Action
0	0	POR and/or external reset recovery
0	1	Logical AND of P20 through P23
1	0	Logical AND of P20 through P27

Watchdog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is disabled after Power-On

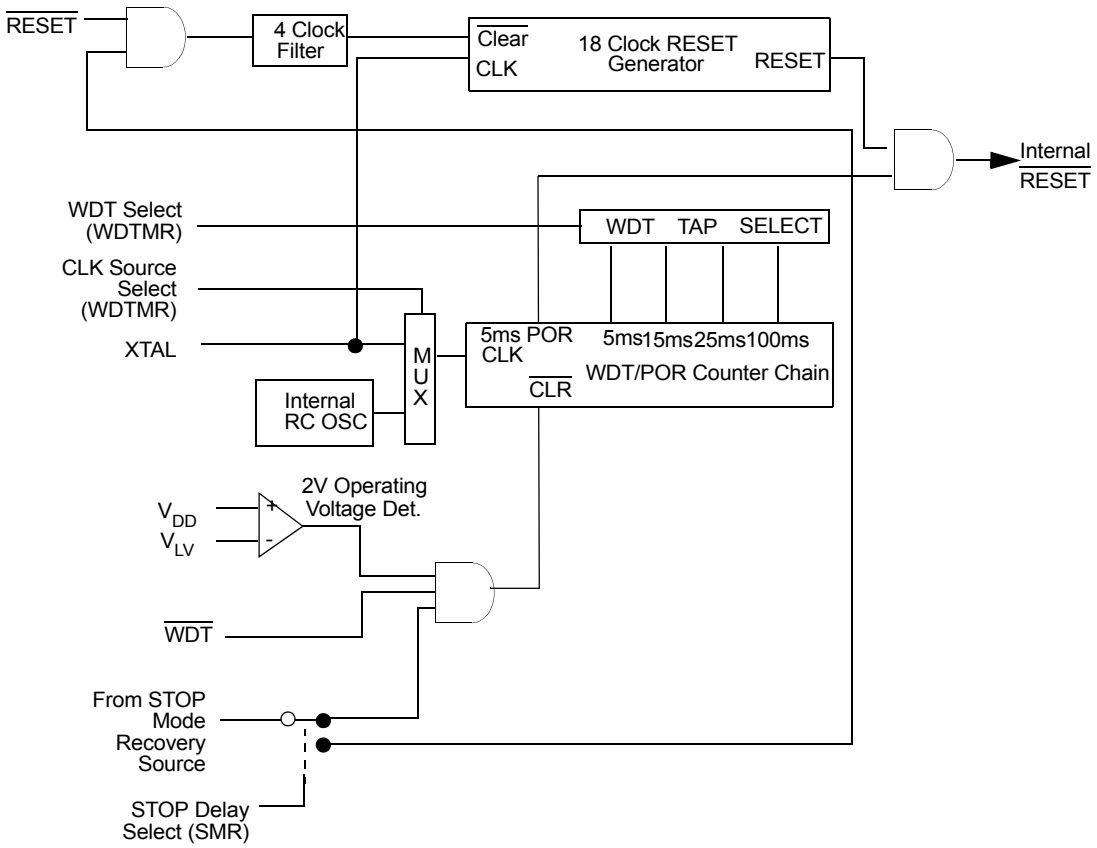


Figure 34. Resets and WDT

Auto Reset Voltage. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. Reset is globally driven if V_{CC} is below VLV (Figure 35).

Z8 Control Register Diagrams

Ordering Information

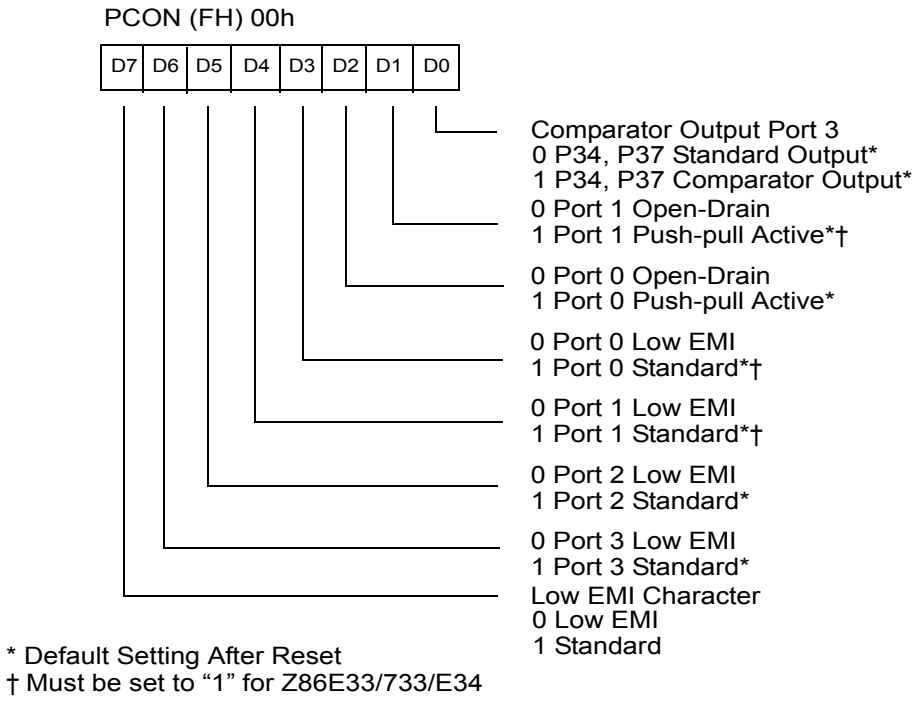
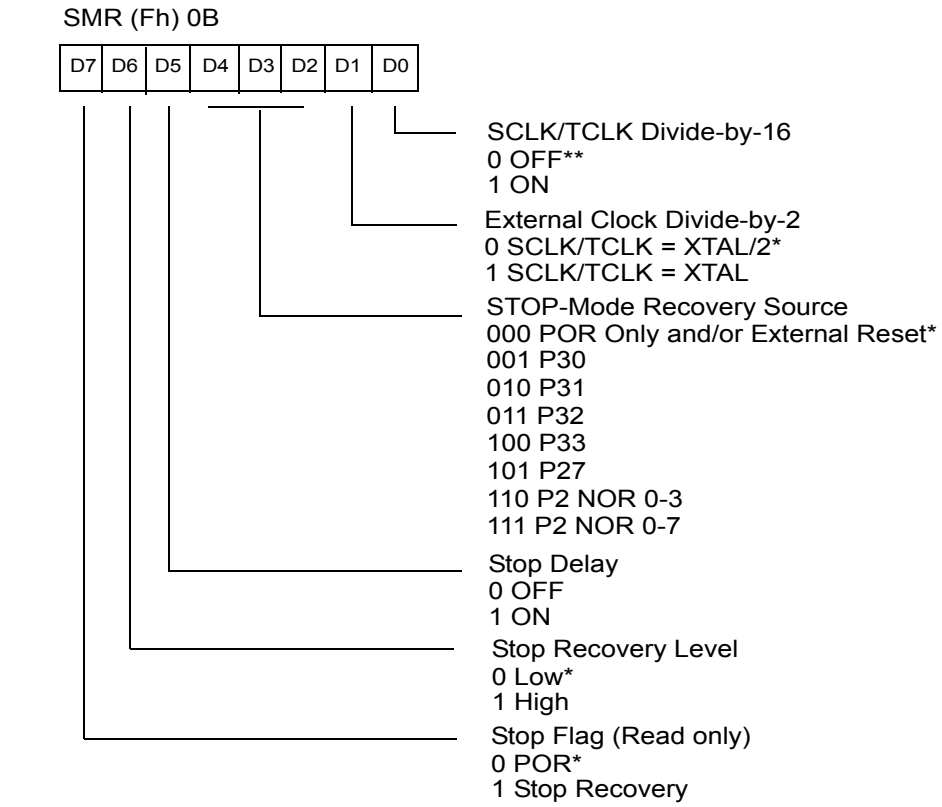


Figure 36. Port Configuration Register (PCON) (Write Only)



Note: Note used in conjunction with SMR2 Source
* Default setting after RESET
** Default setting after RESET and STOP-Mode Recovery

Figure 37. Stop Mode Recovery Register (Write Only Except Bit D7, Which is Read Only)

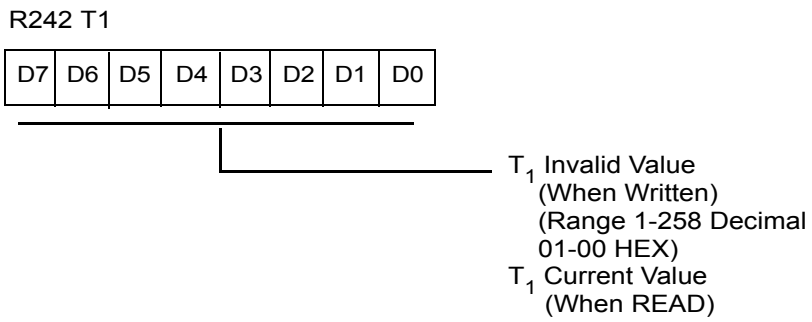


Figure 42. Counter/Timer 1 Register ($F2_h$: Read/Write)

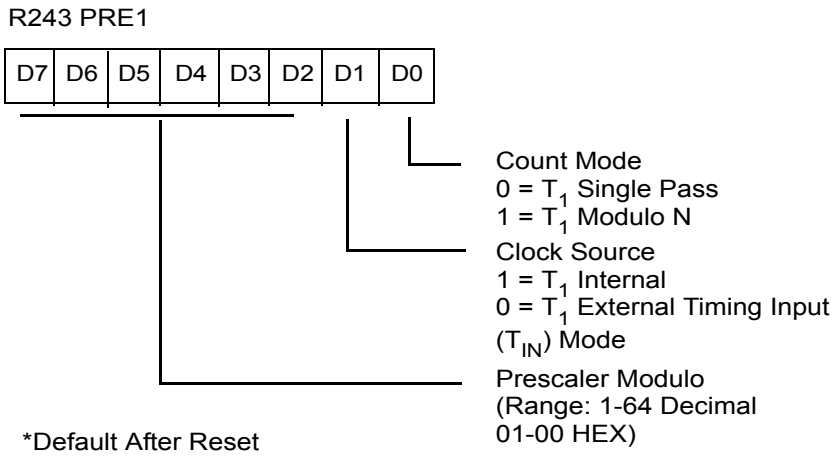


Figure 43. Prescaler 1 Register ($F3_h$: Write Only)

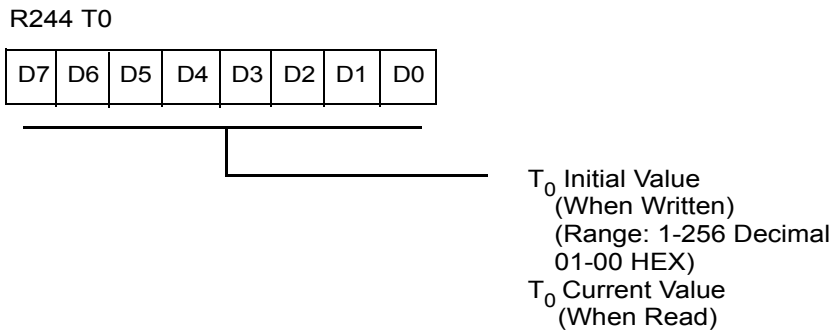


Figure 44. Counter/Timer 0 Register ($F4_h$: Read/Write)

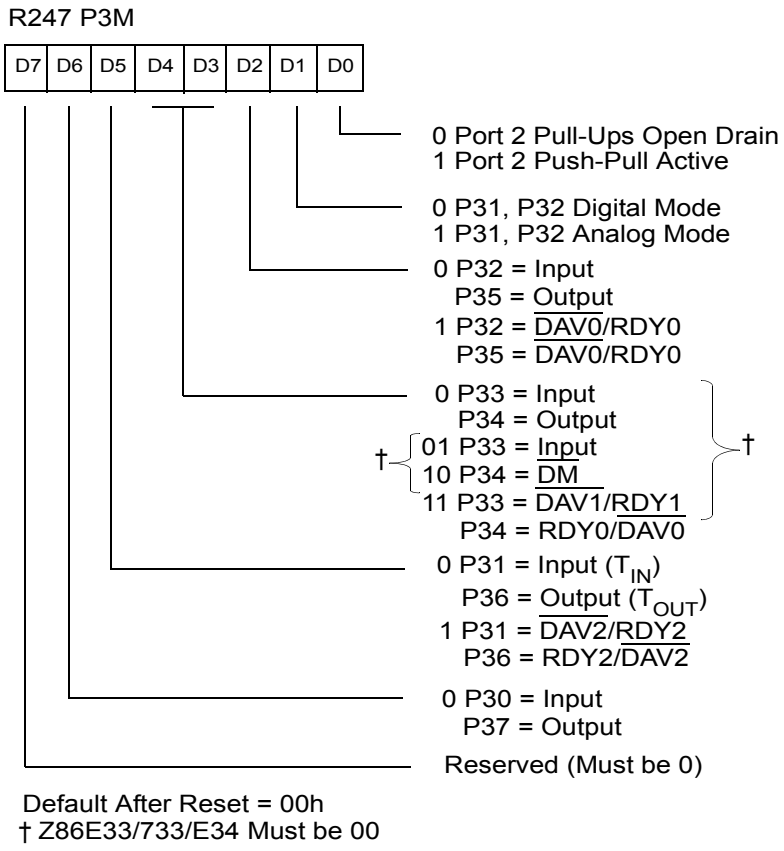


Figure 47. Port 3 Mode Register ($F7_h$: Write Only)