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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	LCD, LVD, PWM, WDT
Number of I/O	37
Program Memory Size	36KB (36K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08lh36clh

1 Addendum for Revision 6

Table 1. MC9S08LH64 Data Sheet Rev 6 Addendum

Location	Description
Section 3.7, “Supply Current Characteristics”/Table 9/Page 23	In the table, for numbers 3 and 4, change “LPS” to “LPR”.

2 Revision History

Table 2 provides a revision history for this document.

Table 2. Revision History Table

Rev. Number	Substantive Changes	Date of Release
1.0	Initial release. Correct errors in the following sections: • Section 3.7, “Supply Current Characteristics”	07/2012

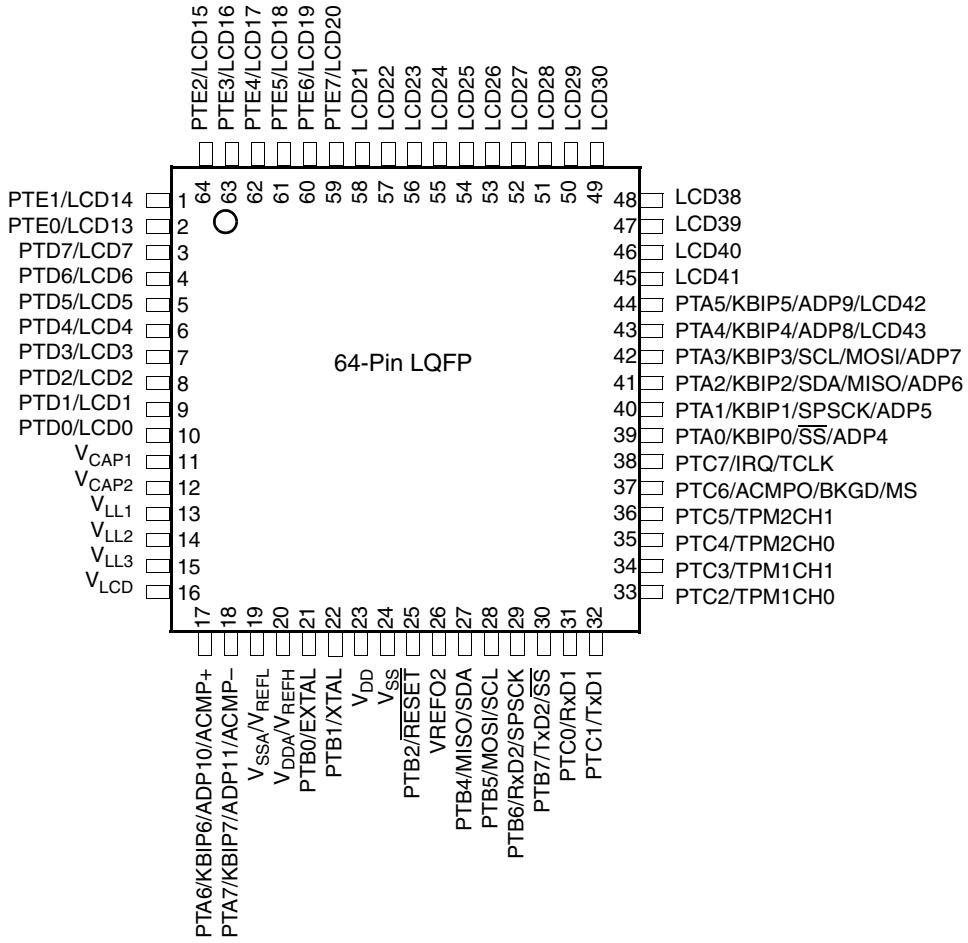


Figure 2. 64-Pin LQFP

Table 2. Pin Availability by Package Pin-Count (continued)

		<-- Lowest **Priority** --> Highest				
80	**64**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt3**	**Alt4**
9	5	PTD5	LCD5			
10	6	PTD4	LCD4			
11	7	PTD3	LCD3			
12	8	PTD2	LCD2			
13	9	PTD1	LCD1			
14	10	PTD0	LCD0			
15	11	V_{CAP1}				
16	12	V_{CAP2}				
17	13	V_{LL1}				
18	14	V_{LL2}				
19	15	V_{LL3}				
20	16	V_{LCD}				
21	17	PTA6	KBIP6	ADP10	ACMP+	
22	18	PTA7	KBIP7	ADP11	ACMP–	
23	19	V_{SSA}				
24		V_{REFL}				
25		DADP0				
26		DADM0				
27		VREFO1				
28	20	V_{REFH}				
29		V_{DDA}				
30	21	PTB0		EXTAL		
31	22	PTB1		XTAL		
32	23	V_{DD}				
33	24	V_{SS}				
34	25	PTB2	$\overline{\text{RESET}}$			
	26	VREFO2				
35	27	PTB4	MISO	SDA		
36	28	PTB5	MOSI	SCL		
37	29	PTB6	RxD2	SPSCK		
38	30	PTB7	TxD2	$\overline{\text{SS}}$		
39	31	PTC0	RxD1			
40	32	PTC1	TxD1			
41	33	PTC2	TPM1CH0			
42	34	PTC3	TPM1CH1			
43	35	PTC4	TPM2CH0			
44	36	PTC5	TPM2CH1			
45	37	PTC6	ACMPO	BKGD	MS	

Table 2. Pin Availability by Package Pin-Count (continued)

		<-- Lowest **Priority** --> Highest				
80	**64**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt3**	**Alt4**
46	38	PTC7	IRQ	TCLK		
47	39	PTA0	KBIP0		$\overline{SS}$	ADP4
48	40	PTA1	KBIP1		SPSCK	ADP5
49	41	PTA2	KBIP2	SDA	MISO	ADP6
50	42	PTA3	KBIP3	SCL	MOSI	ADP7
51	43	PTA4	KBIP4	ADP8	LCD43	
52	44	PTA5	KBIP5	ADP9	LCD42	
53	45	LCD41				
54	46	LCD40				
55	47	LCD39				
56	48	LCD38				
57		LCD37				
58		LCD36				
59		LCD35				
60		LCD34				
61		LCD33				
62		LCD32				
63		LCD31				
64	49	LCD30				
65	50	LCD29				
66	51	LCD28				
67	52	LCD27				
68	53	LCD26				
69	54	LCD25				
70	55	LCD24				
71	56	LCD23				
72	57	LCD22				
73	58	LCD21				
74	59	PTE7	LCD20			
75	60	PTE6	LCD19			
76	61	PTE5	LCD18			
77	62	PTE4	LCD17			
78	63	PTE3	LCD16			
79	64	PTE2	LCD15			
80	1	PTE1	LCD14			

Table 4. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +3.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	± 25	mA
Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins, except for PTB2 are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 5. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H –40 to 85	°C
Maximum junction temperature	T_J	95	°C
Thermal resistance Single-layer board			
80-pin LQFP	θ_{JA}	55	°C/W
64-pin LQFP		73	
Thermal resistance Four-layer board			
80-pin LQFP	θ_{JA}	42	°C/W
64-pin LQFP		54	

The average chip-junction temperature (T_J) in °C can be obtained from:

Table 6. ESD and Latch-up Test Conditions (continued)

Latch-up	Minimum input voltage limit		–2.5	V
	Maximum input voltage limit		7.5	V

Table 7. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	±2000	—	V
2	Charge device model (CDM)	V_{CDM}	±500	—	V
3	Latch-up current at T_A = 85 °C	I_{LAT}	±100	—	mA

1 Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

3.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 8. DC Characteristics

Num	C	Characteristic	Symbol	Condition	Min	Typ[1]	Max	Unit
1		Operating Voltage			1.8		3.6	V
2	C	Output high voltage — PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7][2], low-drive strength	V_{OH}	V_{DD} >1.8 V, I_{Load} = –0.6 mA	V_{DD} – 0.5	—	—	V
	P	Output high voltage — PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7][2], high-drive strength		V_{DD} > 2.7 V, I_{Load} = –10 mA	V_{DD} – 0.5	—	—	
	C			V_{DD} > 1.8 V, I_{Load} = –3 mA	V_{DD} – 0.5	—	—	
3	C	Output high voltage — PTA[4:5], PTD[0:7], PTE[0:7], low-drive strength	V_{OH}	V_{DD} > 1.8 V, I_{Load} = –0.5 mA	V_{DD} – 0.5	—	—	V
	P	Output high voltage — PTA[4:5], PTD[0:7], PTE[0:7], high-drive strength		V_{DD} > 2.7 V, I_{Load} = –2.5 mA	V_{DD} – 0.5	—	—	
	C			V_{DD} > 1.8 V, I_{Load} = –1 mA	V_{DD} – 0.5	—	—	
4	D	Output high current — Max total I_{OH} for all ports	I_{OHT}		—	—	100	mA
5	C	Output low voltage — PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7], low-drive strength	V_{OL}	V_{DD} >1.8 V, I_{Load} = 0.6 mA	—	—	0.5	V
	P	Output low voltage — PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7], high-drive strength		V_{DD} > 2.7 V, I_{Load} = 10 mA	—	—	0.5	
	C			V_{DD} > 1.8 V, I_{Load} = 3 mA	—	—	0.5	

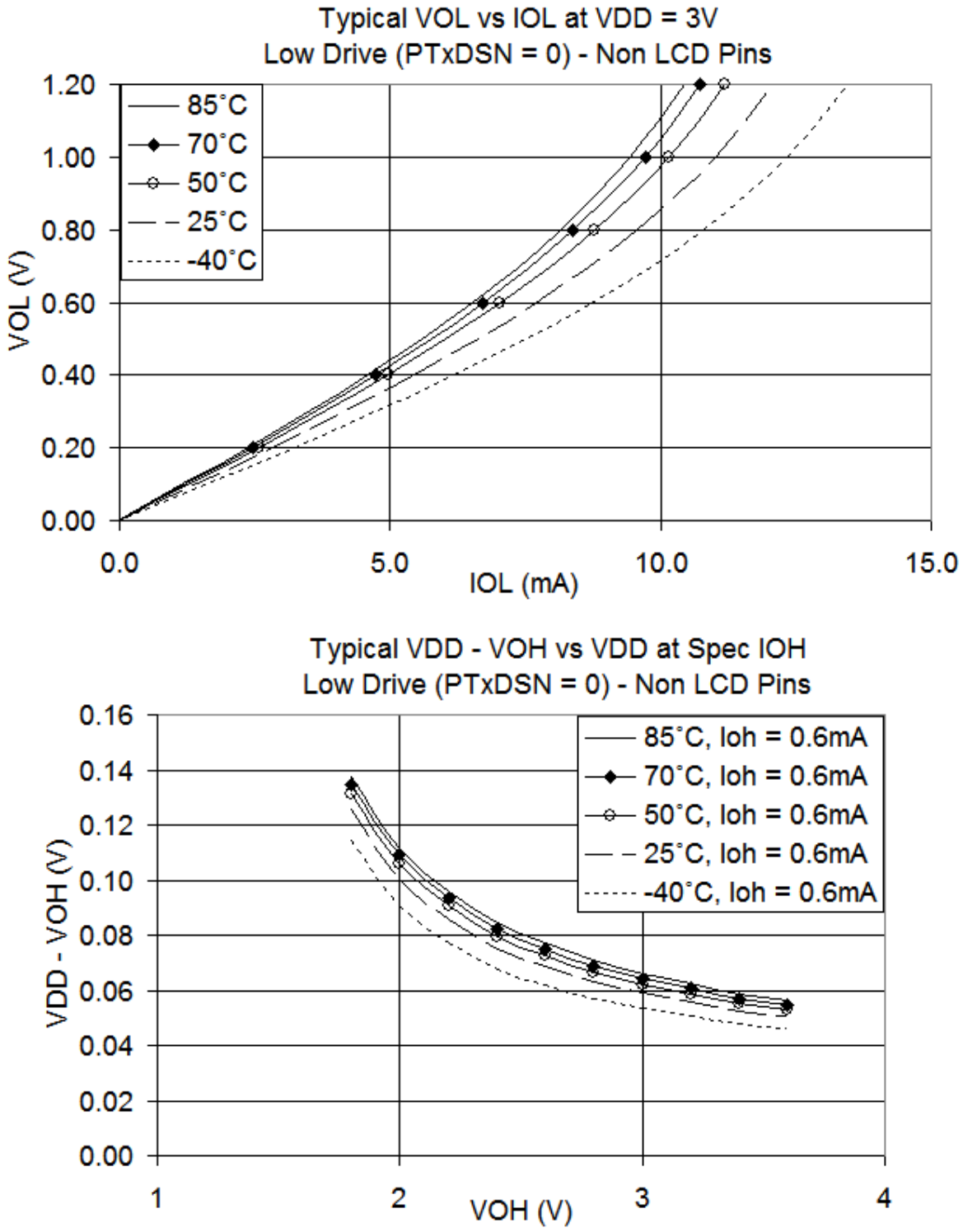


Figure 7. Typical High-Side (Source) Characteristics (Non LCD Pins)— Low Drive (PTxDSn = 0)

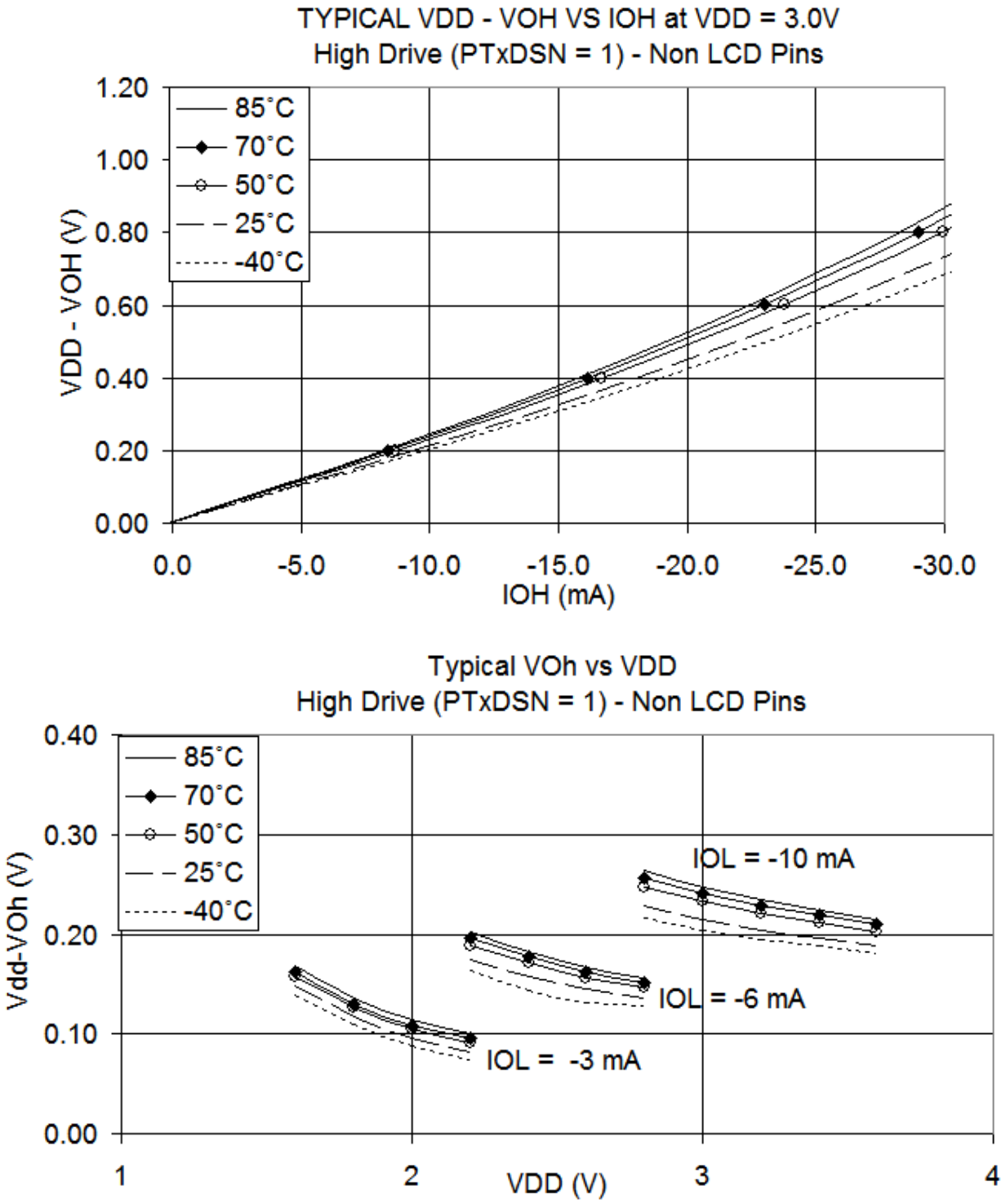


Figure 8. Typical High-Side (Source) Characteristics(Non LCD Pins) — High Drive (PTxDSn = 1)

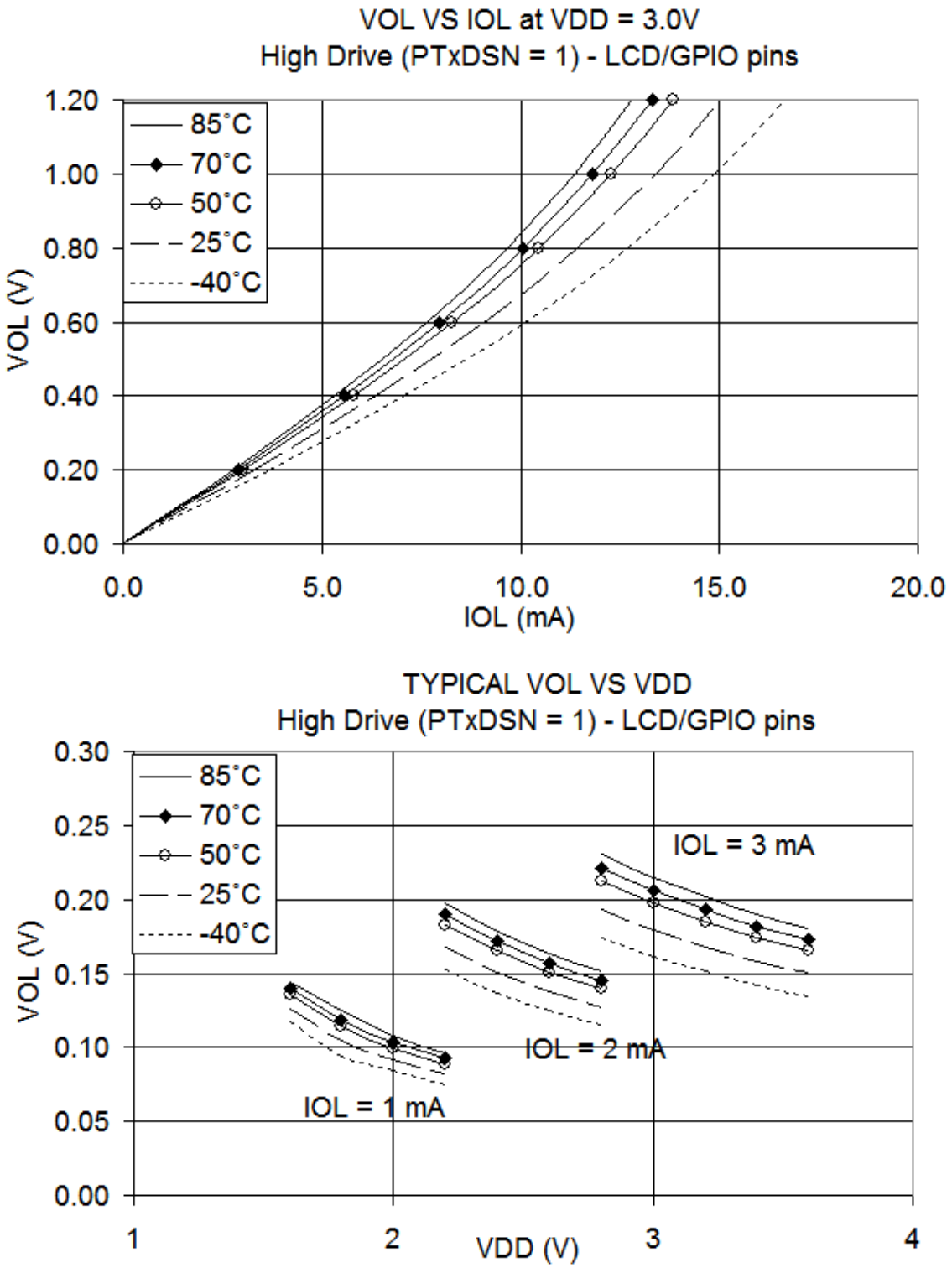


Figure 10. Typical Low-Side Driver (Sink) Characteristics (LCD/GPIO Pins) — High Drive (PTxDSn = 1)

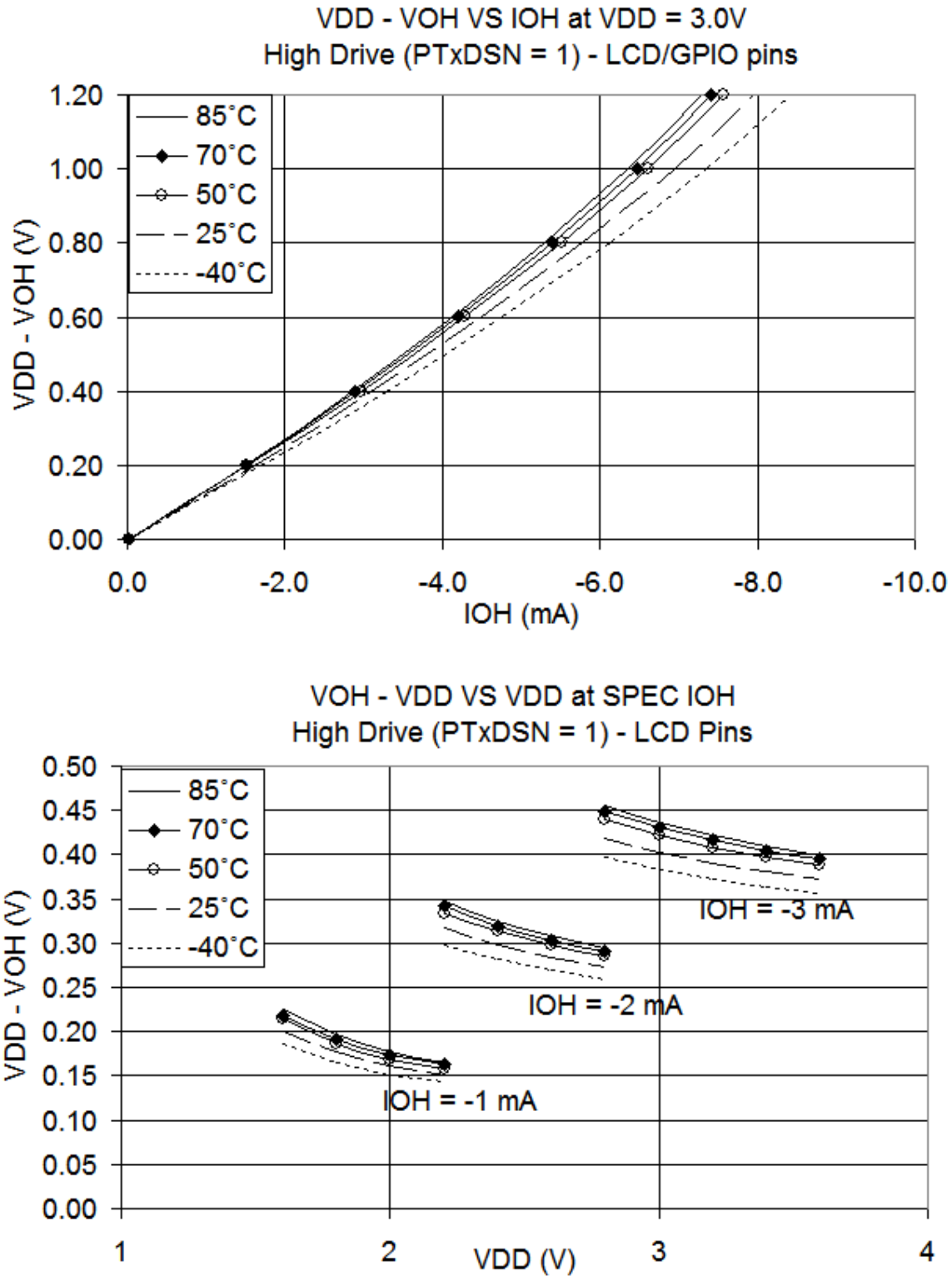


Figure 12. Typical High-Side (Source) Characteristics (LCD/GPIO Pins) — High Drive (PTxDSn = 1)

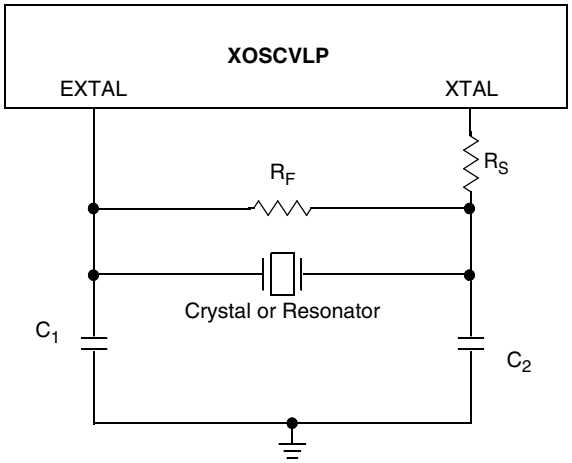


Figure 14. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

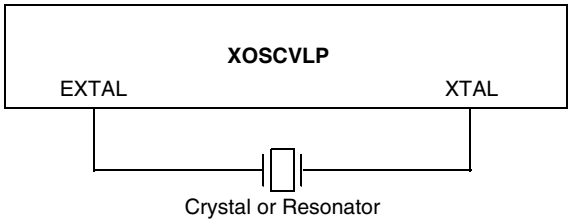


Figure 15. Typical Crystal or Resonator Circuit: Low Range/Low Power

3.9 Internal Clock Source (ICS) Characteristics

Table 12. ICS Frequency Specifications (Temperature Range = –40 to 85 °C Ambient)

Num	C	Characteristic		Symbol	Min	Typ[1]	Max	Unit
1	C	Average internal reference frequency — untrimmed		f_{int_ut}	25	32.7	41.66	kHz
2	P	Average internal reference frequency — user-trimmed		f_{int_t}	31.25	—	39.06	kHz
3	P	Average internal reference frequency — factory-trimmed		f_{int_t}	—	32.7	—	kHz
4	T	Internal reference start-up time		t_{IRST}	—	60	100	µs
5	P	DCO output frequency range — untrimmed	Low range (DFR = 00)	f_{dco_ut}	12.8	16.8	21.33	MHz
	C		Mid range (DFR = 01)		25.6	33.6	42.67	
6	P	DCO output frequency range — trimmed	Low range (DFR = 00)	f_{dco_t}	16	—	20	MHz
	P		Mid range (DFR = 01)		32	—	40	
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$
8	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.2	±0.4	$\%f_{dco}$

Table 12. ICS Frequency Specifications (Temperature Range = –40 to 85 °C Ambient) (continued)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
9	C	Total deviation of trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	+0.5 –1.0	±2	$\%f_{dco}$
10	C	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0 °C to 70 °C	Δf_{dco_t}	—	±0.5	±1	$\%f_{dco}$
11	C	FLL acquisition time[2]	$t_{Acquire}$	—	—	1	ms
12	C	Long term jitter of DCO output clock (averaged over 2-ms interval)[3]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1 Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

2 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

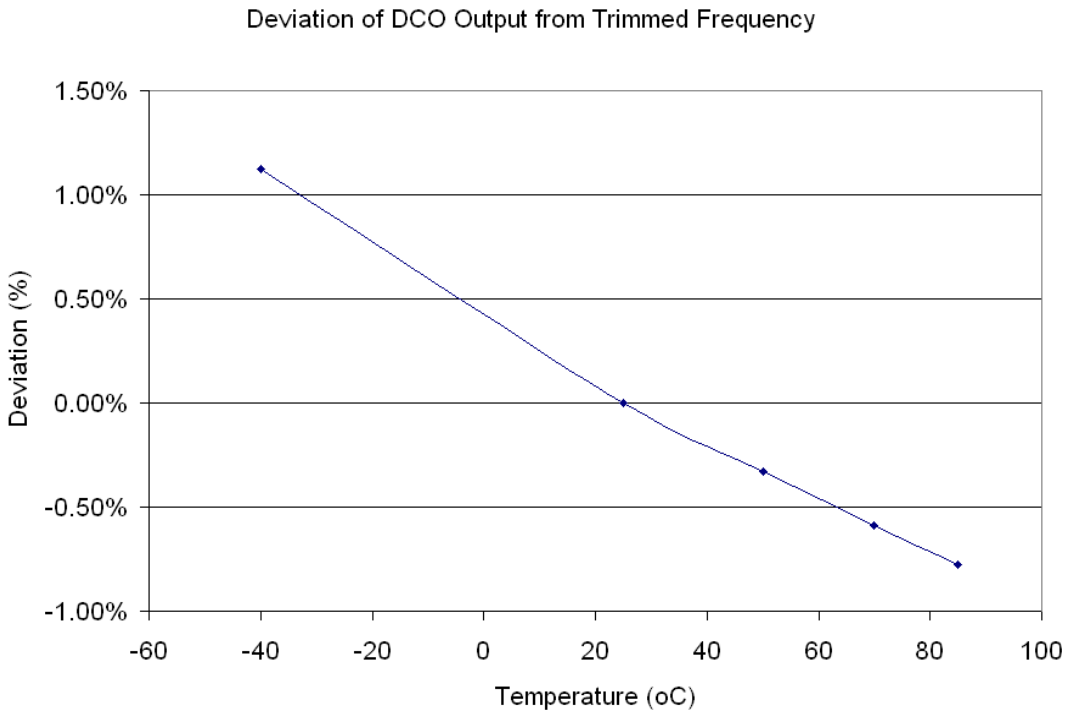


Figure 16. Deviation of DCO Output from Trimmed Frequency (20 MHz, 3.0 V)

3.10 AC Characteristics

This section describes timing characteristics for each peripheral system.

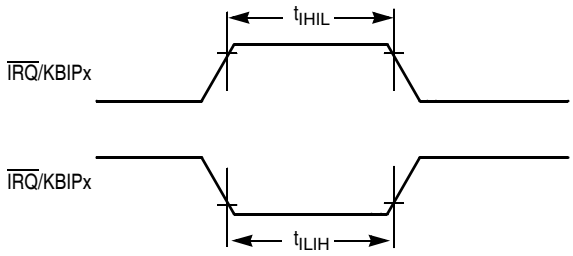


Figure 18. IRQ/KBIPx Timing

3.10.2 TPM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 14. TPM Input Timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

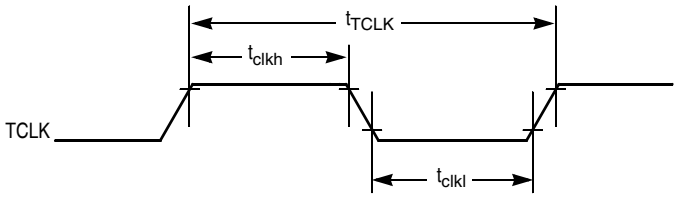


Figure 19. Timer External Clock

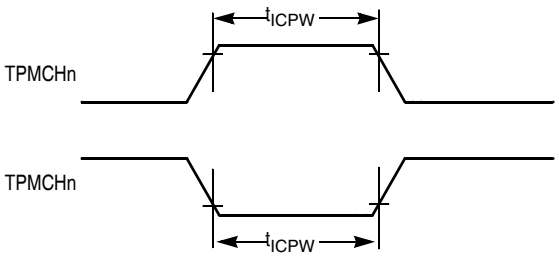
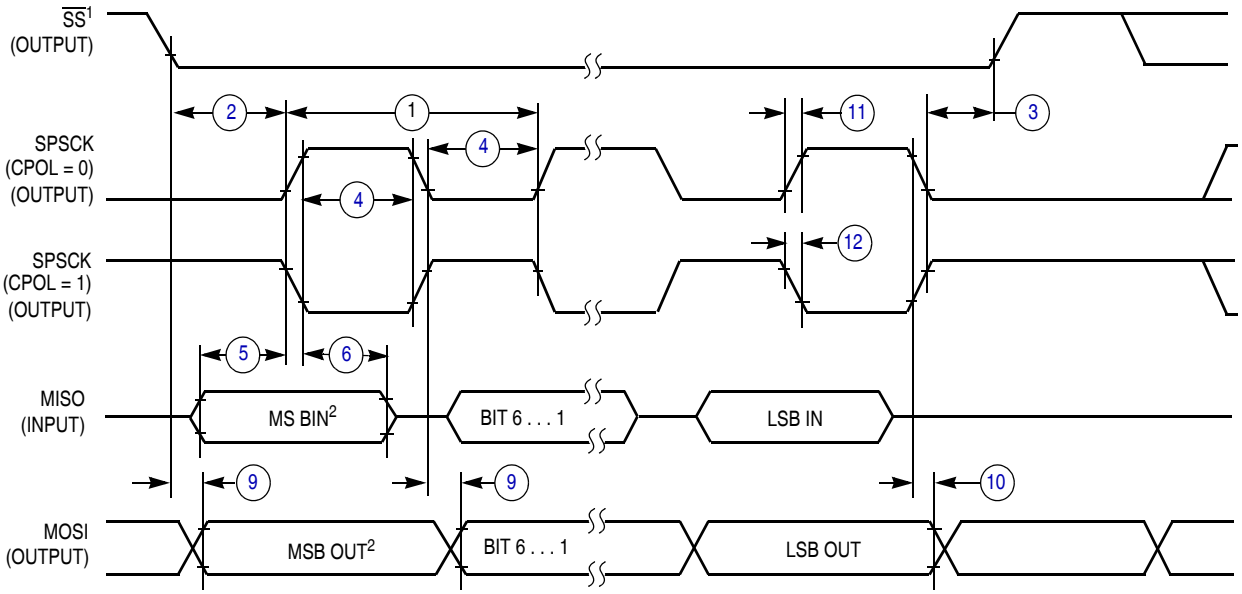


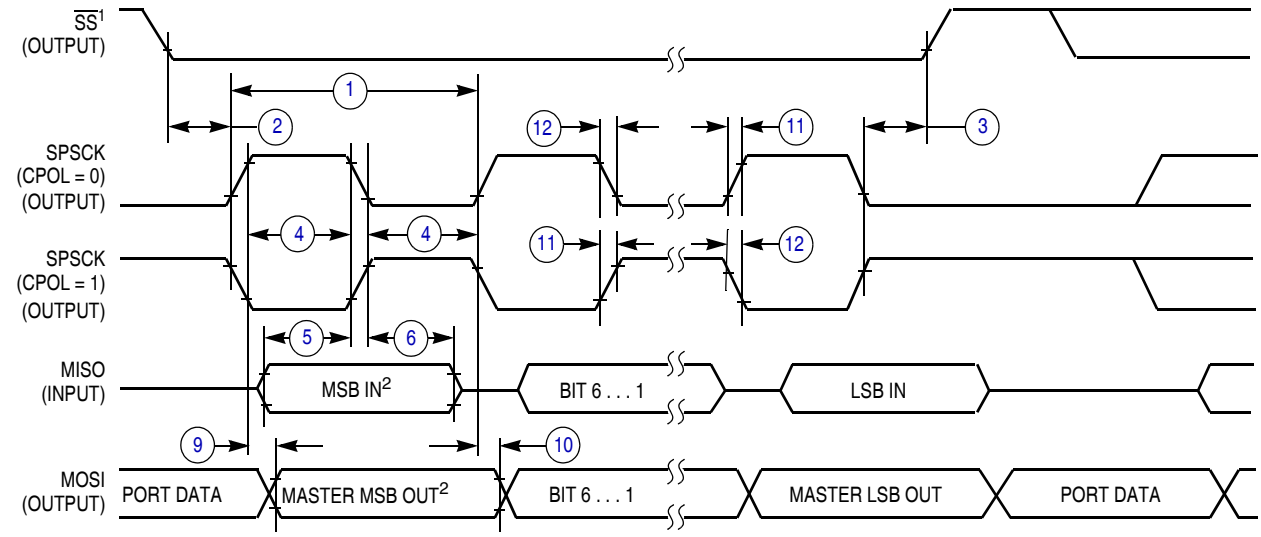
Figure 20. Timer Input Capture Pulse



NOTES:

1. SS output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

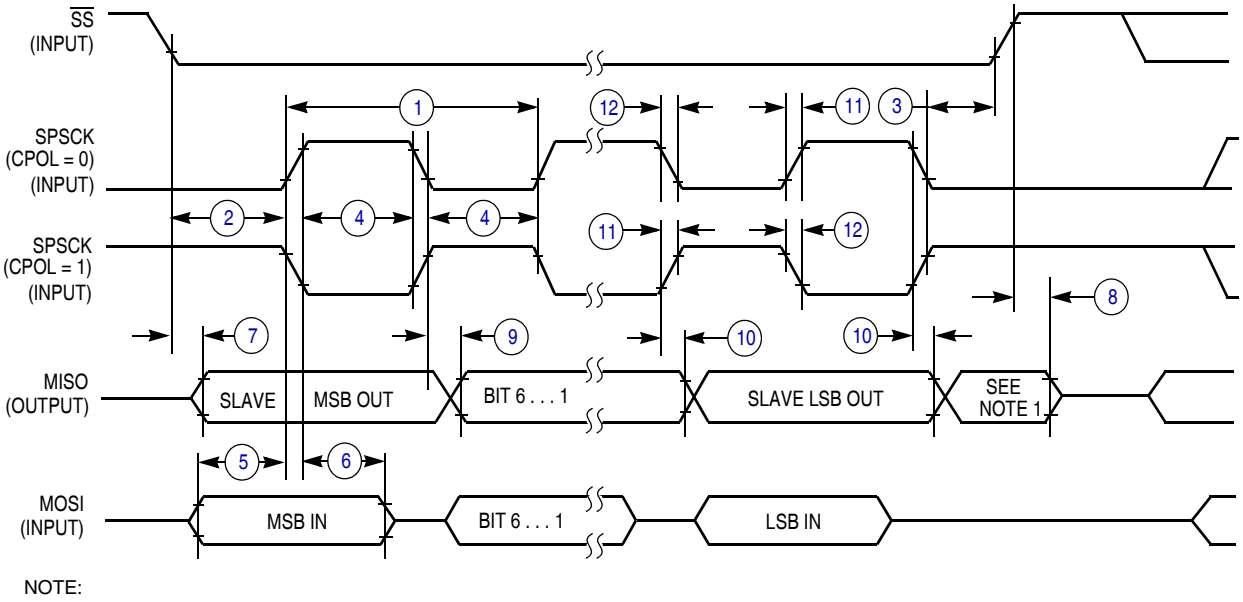
Figure 21. SPI Master Timing (CPHA = 0)



NOTES:

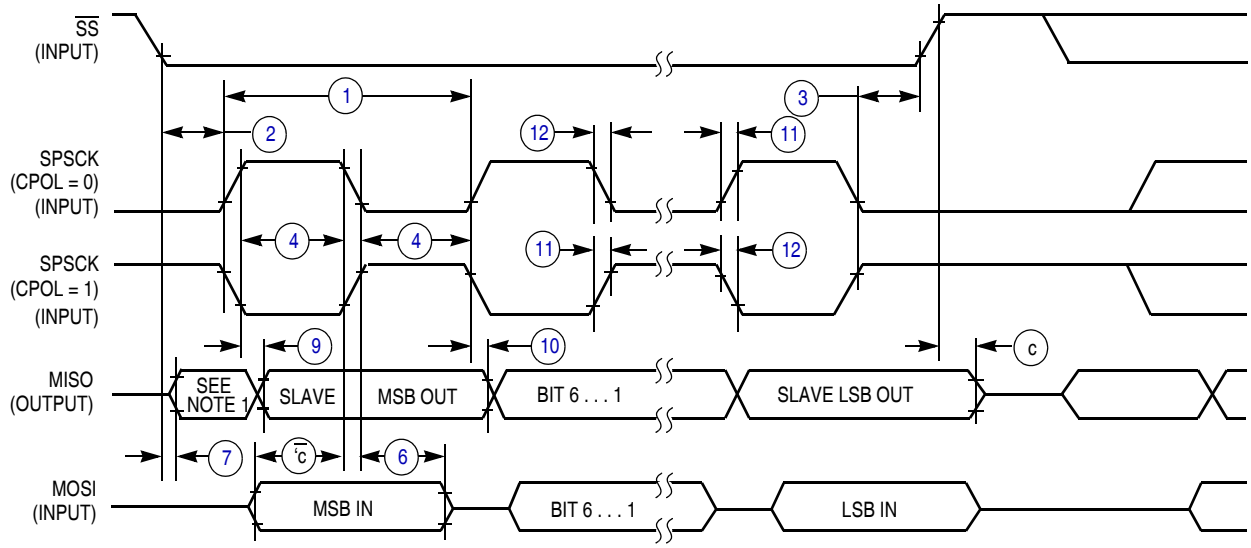
1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 22. SPI Master Timing (CPHA =1)



NOTE:
1. Not defined but normally MSB of character just received.

Figure 23. SPI Slave Timing (CPHA = 0)



NOTE:
1. Not defined but normally LSB of character just received

Figure 24. SPI Slave Timing (CPHA = 1)

Table 17. 16-bit ADC Operating Conditions

Num	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
9	Analog Source Resistance	16 bit modes $f_{ADCK} > 8MHz$ $4MHz < f_{ADCK} < 8MHz$ $f_{ADCK} < 4MHz$	R_{AS}	— — —	— — —	0.5 1 2	kΩ	External to MCU Assumes ADLSMP=0
10		13/12 bit modes $f_{ADCK} > 8MHz$ $4MHz < f_{ADCK} < 8MHz$ $f_{ADCK} < 4MHz$		— — —	— — —	1 2 5		
11		11/10 bit modes $f_{ADCK} > 8MHz$ $4MHz < f_{ADCK} < 8MHz$ $f_{ADCK} < 4MHz$		— — —	— — —	2 5 10		
12		9/8 bit modes $f_{ADCK} > 8MHz$ $f_{ADCK} < 8MHz$		— —	— —	5 10		
13	ADC Conversion Clock Freq.	ADLPC = 0, ADHSC = 1	f_{ADCK}	1.0	—	8	MHz	
14		ADLPC = 0, ADHSC = 0		1.0	—	5		
15		ADLPC = 1, ADHSC = 0		1.0	—	2.5		

1 Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

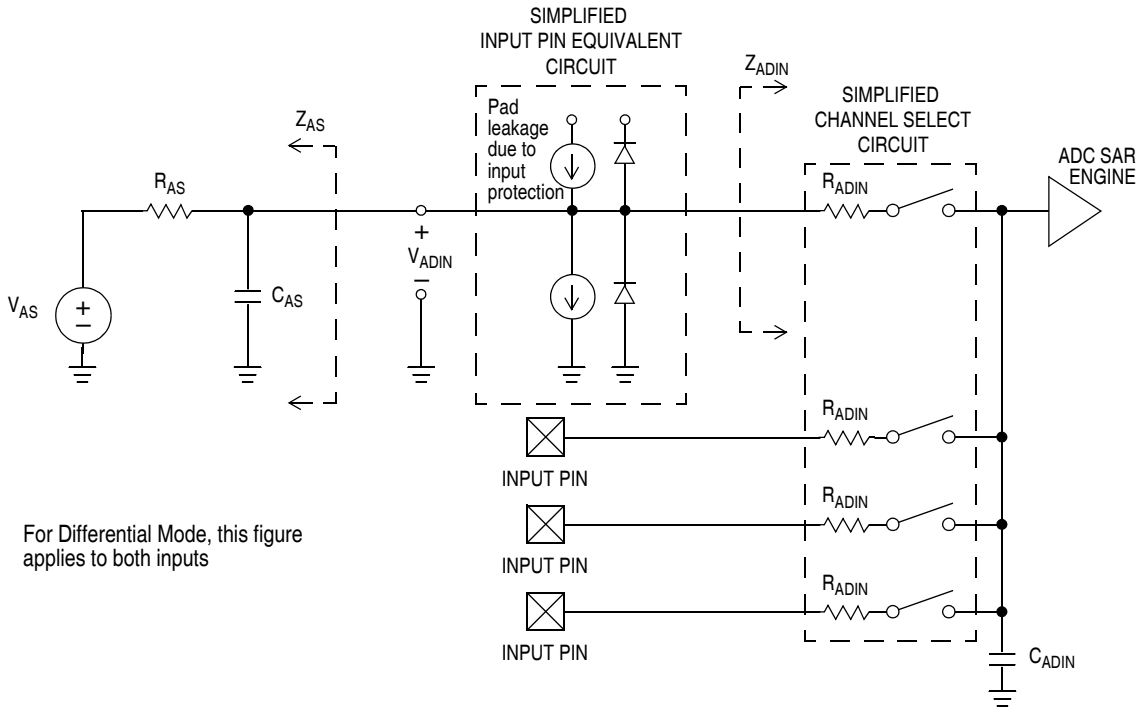


Figure 25. ADC Input Impedance Equivalency Diagram

Table 18. 16-bit ADC Characteristics full operating range($V_{REFH} = V_{DDA} > 1.8$, $V_{REFL} = V_{SSA}$, $F_{ADCK} \leq 8MHz$)

Characteristic	Conditions[1]	C	Symb	Min	Typ[2]	Max	Unit	Comment
Supply Current	ADLPC = 1, ADHSC = 0	T	I_{DDA}	—	215	—	μA	ADLSMP = 0 ADCO = 1
	ADLPC = 0, ADHSC = 0			—	470	—		
	ADLPC=0, ADHSC=1			—	610	—		
Supply Current	Stop, Reset, Module Off	C	I_{DDA}	—	0.01	—	μA	
ADC Asynchronous Clock Source	ADLPC = 1, ADHSC = 0	P	f_{ADACK}	—	2.4	—	MHz	$t_{ADACK} = 1/f_{ADACK}$
	ADLPC = 0, ADHSC = 0			—	5.2	—		
	ADLPC = 0, ADHSC = 1			—	6.2	—		
Sample Time	See reference manual for sample times							
Conversion Time	See reference manual for conversion times							

Table 18. 16-bit ADC Characteristics full operating range(V_{REFH} = V_{DDA} > 1.8, V_{REFL} = V_{SSA}, F_{ADCK} ≤ 8MHz)

Characteristic	Conditions[1]	C	Symb	Min	Typ[2]	Max	Unit	Comment
Full-Scale Error	16-bit differential mode 16-bit single-ended mode	T	E_{FS}	— —	+10/0 +14/0	+42/-2 +46/-2	LSB[2]	V_{ADIN} = V_{DDA}
	13-bit differential mode 12-bit single-ended mode	T		— —	±1.0 ±1.0	±3.5 ±3.5		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.4 ±0.4	±1.5 ±1.5		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.2 ±0.2	±0.5 ±0.5		
Quantization Error	16-bit modes	D	E_Q	—	-1 to 0	—	LSB[2]	
	≤13-bit modes			—	—	±0.5		
Effective Number of Bits	16-bit differential mode Avg = 32 Avg = 16 Avg = 8 Avg = 4 Avg = 1	C	ENOB	 12.8 12.7 12.6 12.5 11.9	 14.2 13.8 13.6 13.3 12.5	 — — — — —	Bits	F_{in} = F_{sample}/100
	16-bit single-ended mode Avg = 32 Avg = 16 Avg = 8 Avg = 4 Avg = 1	D		 — — — — —	 13.2 12.8 12.6 12.3 11.5	 — — — — —		
Signal to Noise plus Distortion	See ENOB		SINAD	$SINAD = 6.02 \cdot ENOB + 1.76$			dB	
Total Harmonic Distortion	16-bit differential mode Avg = 32	C	THD	—	-91.5	-74.3	dB	F_{in} = F_{sample}/100
	16-bit single-ended mode Avg = 32	D		—	-85.5	—		
Spurious Free Dynamic Range	16-bit differential mode Avg = 32	C	SFDR	75.0	92.2	—	dB	F_{in} = F_{sample}/100
	16-bit single-ended mode Avg = 32	D		—	86.2	—		
Input Leakage Error	all modes	D	E_{IL}	I_{In} * R_{AS}			mV	I_{In} = leakage current (refer to DC characteristics)
Temp Sensor Slope	-40 °C– 25 °C	C	m	—	1.646	—	mV/°C	
	25 °C– 125 °C			—	1.769	—		
Temp Sensor Voltage	25 °C	C	V_{TEMP25}	—	701.2	—	mV	

1 All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDA}

2 Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK}=2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

3 1 LSB = (V_{REFH} - V_{REFL})/2^N

Table 19. 16-bit ADC Characteristics(V_{REFH} = V_{DDA} ≥ 2.7V, V_{REFL} = V_{SSA}, F_{ADCK} ≤ 4MHz, ADHSC=1)

Characteristic	Conditions[1]	C	Symb	Min	Typ[2]	Max	Unit	Comment
Total Unadjusted Error	16-bit differential mode 16-bit single-ended mode	T	TUE	— —	±16 ±20	+24/-24 +32/-20	LSB[3]	32x Hardware Averaging (AVGE = %1 AVGS = %11)
	13-bit differential mode 12-bit single-ended mode	T		— —	±1.5 ±1.75	±2.0 ±2.5		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.7 ±0.8	±1.0 ±1.25		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.5 ±0.5	±1.0 ±1.0		
Differential Non-Linearity	16-bit differential mode 16-bit single-ended mode	T	DNL	— —	±2.5 ±2.5	±3 ±3	LSB[2]	
	13-bit differential mode 12-bit single-ended mode	T		— —	±0.7 ±0.7	±1 ±1		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.5 ±0.5	±0.75 ±0.75		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.2 ±0.2	±0.5 ±0.5		
Integral Non-Linearity	16-bit differential mode 16-bit single-ended mode	T	INL	— —	±6.0 ±10.0	±12.0 ±16.0	LSB[2]	
	13-bit differential mode 12-bit single-ended mode	T		— —	±1.0 ±1.0	±2.0 ±2.0		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.5 ±0.5	±1.0 ±1.0		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.3 ±0.3	±0.5 ±0.5		
Zero-Scale Error	16-bit differential mode 16-bit single-ended mode	T	E_{ZS}	— —	±4.0 ±4.0	+16/0 +16/-8	LSB[2]	V_{ADIN} = V_{SSA}
	13-bit differential mode 12-bit single-ended mode	T		— —	±0.7 ±0.7	±2.0 ±2.0		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.4 ±0.4	±1.0 ±1.0		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.2 ±0.2	±0.5 ±0.5		

2 Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

3 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

3.13 VREF Specifications

Table 20. VREF Electrical Specifications

Num	Characteristic	Symbol	Min	Max	Unit
1	Supply voltage	V_{DD}	1.80	3.60	V
2	Operating temperature range	T_{op}	–40	105	C
3	Maximum Load	—	—	10	mA
Operation across Temperature					
4	V Room Temp	V Room Temp	1.135	1.165	V
5	Untrimmed –40 °C	Untrimmed –40 °C	–2 to –6 from Room Temp Voltage		mV
6	Trimmed –40 °C	Trimmed –40 °C	± 1 from Room Temp Voltage		mV
7	Untrimmed 0 °C	Untrimmed 0 °C	+1 to –2 from Room Temp Voltage		mV
	Trimmed 0 °C	Trimmed 0 °C	± 0.5 from Room Temp Voltage		mV
8	Untrimmed 50 °C	Untrimmed 50 °C	+1 to –2 from Room Temp Voltage		mV
9	Trimmed 50 °C	Trimmed 50 °C	± 0.5 from Room Temp Voltage		mV
10	Untrimmed 85 °C	Untrimmed 85 °C	0 to –4 from Room Temp Voltage		mV
11	Trimmed 85 °C	Trimmed 85 °C	± 0.5 from Room Temp Voltage		mV
12	Untrimmed 125 °C	Untrimmed 125 °C	–2 to –6 from Room Temp Voltage		mV
13	Trimmed 125 °C	Trimmed 125 °C	± 1 from Room Temp Voltage		mV
14	Load Bandwidth	—	—	—	—
15	Load Regulation Mode = 10 at 1mA load	Mode = 10	20	100	µV/mA
16	Line Regulation (Power Supply Rejection)	DC	± 0.1 from Room Temp Voltage		mV
		AC	–60		dB
Power Consumption					
17	Powered down Current (Stop Mode, VREFEN = 0, VRSTEN = 0)	I	—	.100	µA
18	Bandgap only (Mode[1:0] 00)	I	—	75	µA
19	Low-Power buffer (Mode[1:0] 01)	I	—	125	µA
20	Tight-Regulation buffer (Mode[1:0] 10)	I	—	1.1	mA
21	Reserved (Mode[1:0] 11)	—	—	—	—