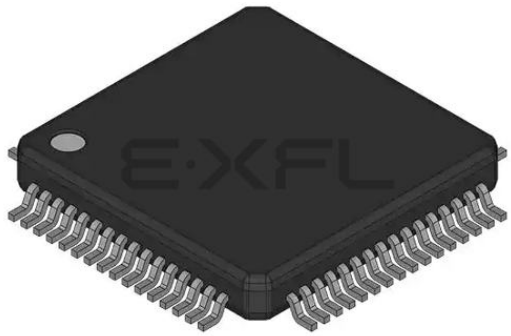

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	LCD, LVD, PWM, WDT
Number of I/O	37
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s08lh64clh

Freescale Semiconductor
Data Sheet Addendum

MC9S08LH64AD
Rev. 1, 08/2012

MC9S08LH64 Data Sheet Addendum

by: Automotive and Industrial Solutions Group

This document describes corrections to the *MC9S08LH64 Series Data Sheet*, order number MC9S08LH64. For convenience, the addenda items are grouped by revision. Please check our website at http://www.freescale.com for the latest updates.

The current available version of the *MC9S08LH64 Series Data Sheet* is Revision 6.

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MC9S08LH64AD
Rev. 1
08/2012

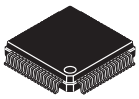
Freescale Semiconductor
Data Sheet: Advanced Information

Document Number: MC9S08LH64
Rev. 6, 4/2012

An Energy Efficient Solution by Freescale

MC9S08LH64 Series

Covers: MC9S08LH64 and MC9S08LH36



64-LQFP
Case 840F

80-LQFP
Case 917A

- 8-bit HCS08 Central Processor Unit (CPU)
  - Up to 40 MHz CPU at 3.6 V to 2.1 V across temperature range of –40 °C to 85 °C
  - Up to 20 MHz at 2.1 V to 1.8 V across temperature range of –40 °C to 85 °C
  - HC08 instruction set with added BGND instruction
  - Support for up to 32 interrupt/reset sources
- On-Chip Memory
  - Dual array flash read/program/erase over full operating voltage and temperature
  - Random-access memory (RAM)
  - Security circuitry to prevent unauthorized access to RAM and flash contents
- Power-Saving Modes
  - Two low-power stop modes
  - Reduced-power wait mode
  - Low-power run and wait modes allow peripherals to run while voltage regulator is in standby
  - Peripheral clock gating register can disable clocks to unused modules, thereby reducing currents
  - Very low-power external oscillator that can be used in stop2 or stop3 modes to provide accurate clock source to time-of-day (TOD) module
  - 6 µs typical wakeup time from stop3 mode
- Clock Source Options
  - Oscillator (XOSC) — Loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
  - Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked-loop (FLL) controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supporting bus frequencies from 1 MHz to 20 MHz
- System Protection
  - Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal clock source or bus clock
  - Low-voltage warning with interrupt
  - Low-voltage detection with reset or interrupt
  - Illegal opcode detection with reset; illegal address detection with reset
  - Flash block protection
- Development Support
  - Single-wire background debug interface
  - Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints in on-chip debug module)
  - On-chip in-circuit emulator (ICE) debug module containing three comparators and nine trigger modes
- Peripherals
  - LCD — Up to 8×36 or 4×40 LCD driver with internal charge pump and option to provide an internally-regulated LCD reference that can be trimmed for contrast control
  - ADC —16-bit resolution; with a dedicated differential ADC input, and 8 single-ended ADC inputs; up to 2.5 µs conversion time; hardware averaging; calibration registers, automatic compare function; temperature sensor; operation in stop3; fully functional from 3.6 V to 1.8 V
  - IIC — Inter-integrated circuit bus module to operate at up to 100 kbps with maximum bus loading; multi-master operation; programmable slave address; interrupt-driven byte-by-byte data transfer; broadcast mode; 10-bit addressing
  - ACMP — Analog comparator with selectable interrupt on rising, falling, or either edge of comparator output; compare option to fixed internal reference voltage; outputs can be optionally routed to TPM module; operation in stop3
  - SCIx — Two full-duplex non-return to zero (NRZ) modules (SCI1 and SCI2); LIN master extended break generation; LIN slave extended break detection; wakeup on active edge
  - SPI — Full-duplex or single-wire bidirectional; double-buffered transmit and receive; master or slave mode; MSB-first or LSB-first shifting
  - TPMx — Two 2-channel (TPM1 and TPM2); selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel
  - TOD — (Time-of-day) 8-bit, quarter second counter with match register; external clock source for precise time base, time-of-day, calendar, or task scheduling functions
  - VREFx — Trimmable via an 8-bit register in 0.5 mV steps; automatically loaded with room temperature value upon reset; can be enabled to operate in stop3 mode; trim register is not available in stop modes
- Input/Output
  - Dedicated accurate voltage reference output pin, 1.15 V output (VREFOx); trimmable with 0.5 mV resolution
  - Up to 39 GPIOs, two output-only pins
  - Hysteresis and configurable pullup device on all input pins; configurable slew rate and drive strength on all output pins
- Package Options
  - 14mm × 14mm 80-pin LQFP, 10 mm × 10 mm 64-pin LQFP

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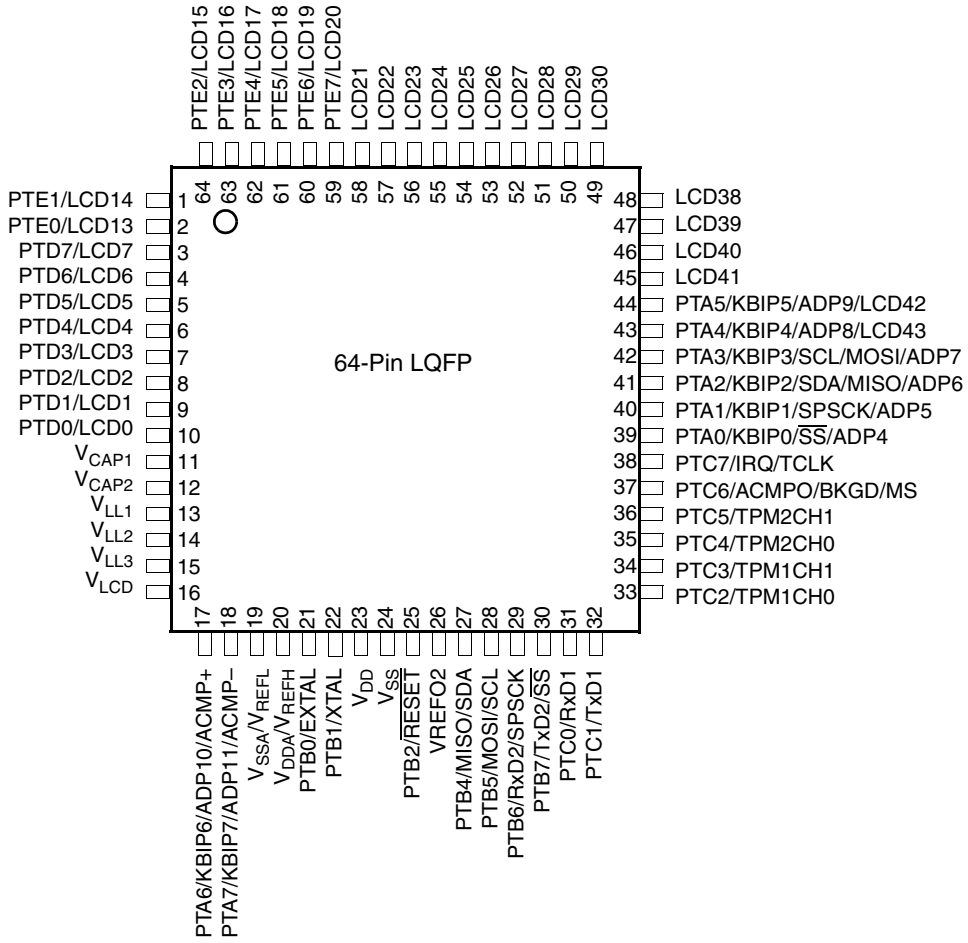

Figure 2. 64-Pin LQFP

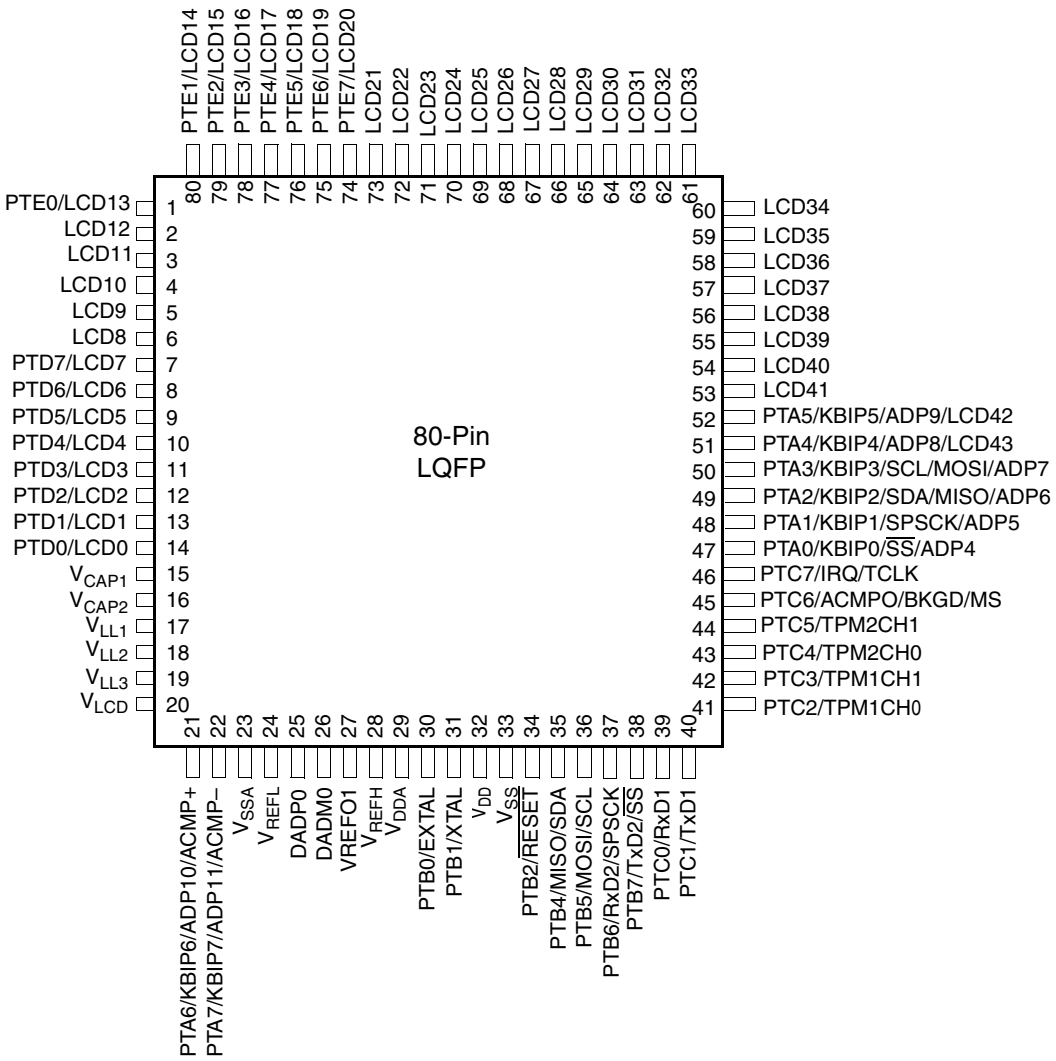

Figure 3. 80-Pin LQFP

Table 2. Pin Availability by Package Pin-Count

		<-- Lowest **Priority** --> Highest				
80	**64**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt3**	**Alt4**
1	2	PTE0	LCD13			
2		LCD12				
3		LCD11				
4		LCD10				
5		LCD9				
6		LCD8				
7	3	PTD7	LCD7			
8	4	PTD6	LCD6			

3 Electrical Characteristics

3.1 Introduction

This section contains electrical and timing specifications for the MC9S08LH64 Series of microcontrollers available at the time of publication.

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 3. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 4 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pullup resistor associated with the pin is enabled.

Table 4. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +3.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	± 25	mA
Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins, except for PTB2 are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 5. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H –40 to 85	°C
Maximum junction temperature	T_J	95	°C
Thermal resistance Single-layer board			
80-pin LQFP	θ_{JA}	55	°C/W
64-pin LQFP		73	
Thermal resistance Four-layer board			
80-pin LQFP	θ_{JA}	42	°C/W
64-pin LQFP		54	

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273\ °C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273\ °C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be taken to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification, ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless instructed otherwise in the device specification.

Table 6. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body Model	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	3	
Charge Device Model	Series resistance	R1	0	Ω
	Storage capacitance	C	200	pF
	Number of pulses per pin	—	3	

Table 6. ESD and Latch-up Test Conditions (continued)

Latch-up	Minimum input voltage limit		–2.5	V
	Maximum input voltage limit		7.5	V

Table 7. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	±2000	—	V
2	Charge device model (CDM)	V_{CDM}	±500	—	V
3	Latch-up current at T_A = 85 °C	I_{LAT}	±100	—	mA

1 Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

3.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 8. DC Characteristics

Num	C	Characteristic	Symbol	Condition	Min	Typ[1]	Max	Unit
1		Operating Voltage			1.8		3.6	V
2	C	Output high voltage — PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7][2], low-drive strength	V_{OH}	V_{DD} >1.8 V, I_{Load} = –0.6 mA	V_{DD} – 0.5	—	—	V
	P	Output high voltage — PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7][2], high-drive strength		V_{DD} > 2.7 V, I_{Load} = –10 mA	V_{DD} – 0.5	—	—	
	C			V_{DD} > 1.8 V, I_{Load} = –3 mA	V_{DD} – 0.5	—	—	
3	C	Output high voltage — PTA[4:5], PTD[0:7], PTE[0:7], low-drive strength	V_{OH}	V_{DD} > 1.8 V, I_{Load} = –0.5 mA	V_{DD} – 0.5	—	—	V
	P	Output high voltage — PTA[4:5], PTD[0:7], PTE[0:7], high-drive strength		V_{DD} > 2.7 V, I_{Load} = –2.5 mA	V_{DD} – 0.5	—	—	
	C			V_{DD} > 1.8 V, I_{Load} = –1 mA	V_{DD} – 0.5	—	—	
4	D	Output high current — Max total I_{OH} for all ports	I_{OHT}		—	—	100	mA
5	C	Output low voltage — PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7], low-drive strength	V_{OL}	V_{DD} >1.8 V, I_{Load} = 0.6 mA	—	—	0.5	V
	P	Output low voltage — PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7], high-drive strength		V_{DD} > 2.7 V, I_{Load} = 10 mA	—	—	0.5	
	C			V_{DD} > 1.8 V, I_{Load} = 3 mA	—	—	0.5	

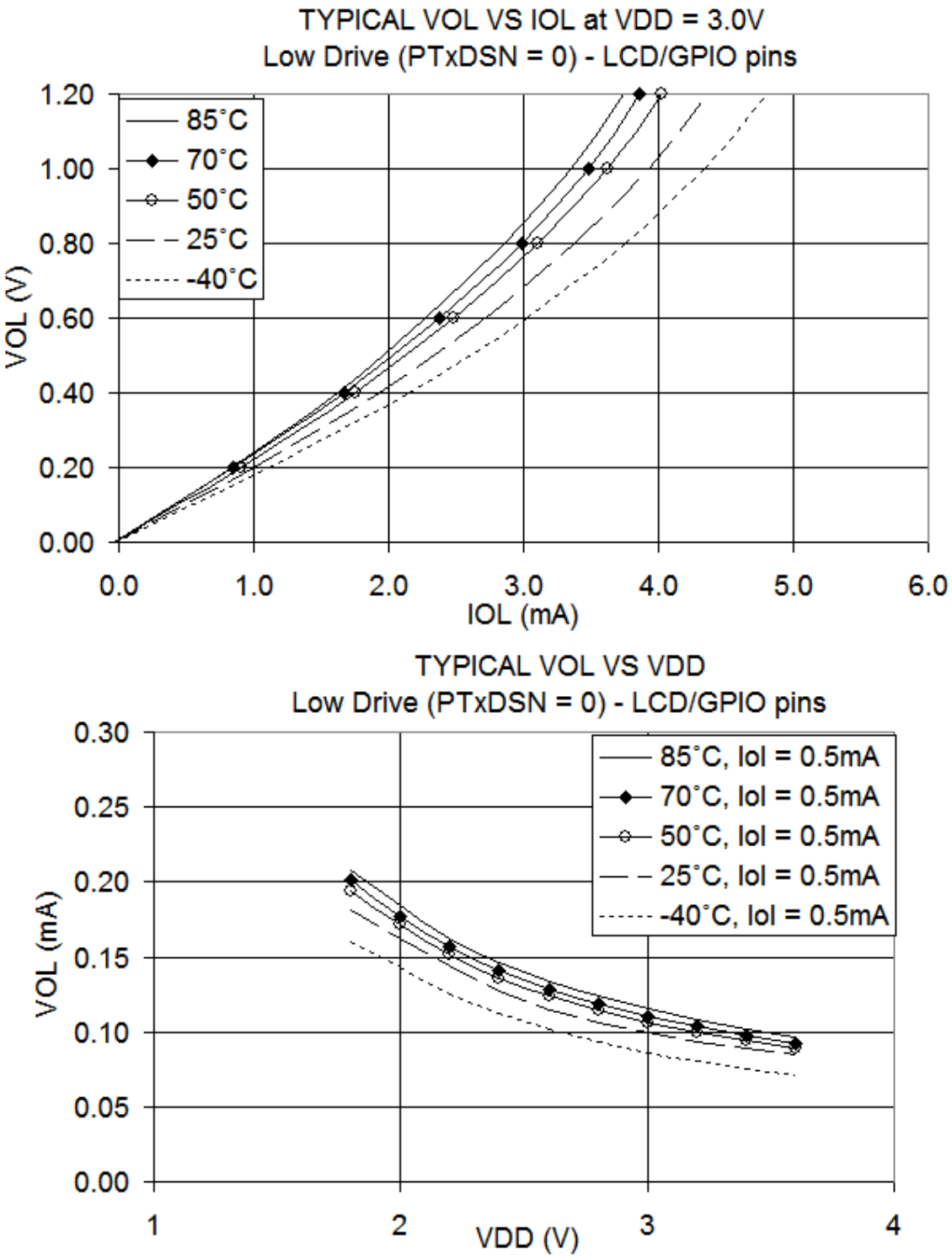

Figure 9. Typical Low-Side Driver (Sink) Characteristics (LCD/GPIO Pins)— Low Drive (PTxDSn = 0)

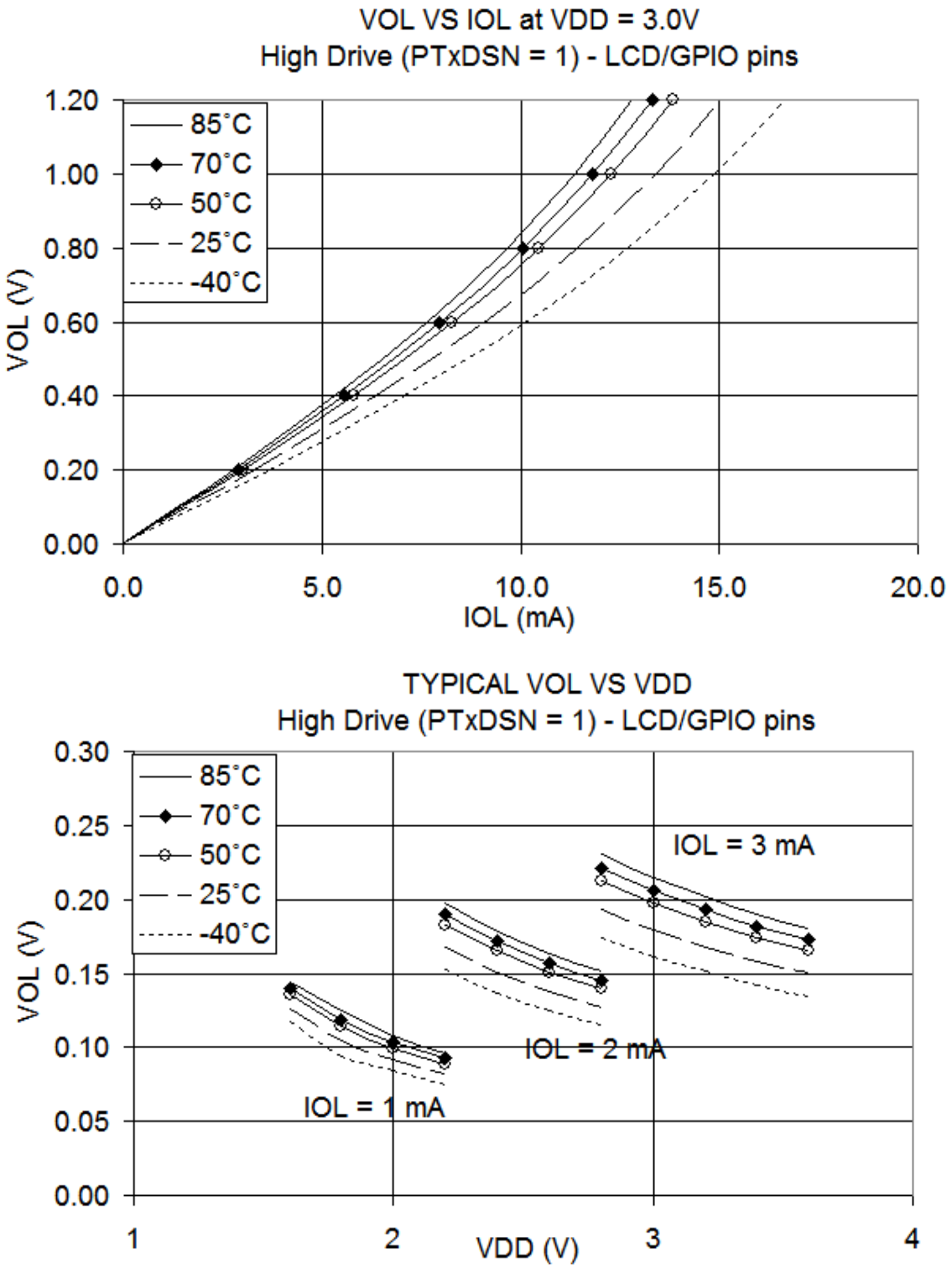

Figure 10. Typical Low-Side Driver (Sink) Characteristics (LCD/GPIO Pins) — High Drive (PTxDSn = 1)

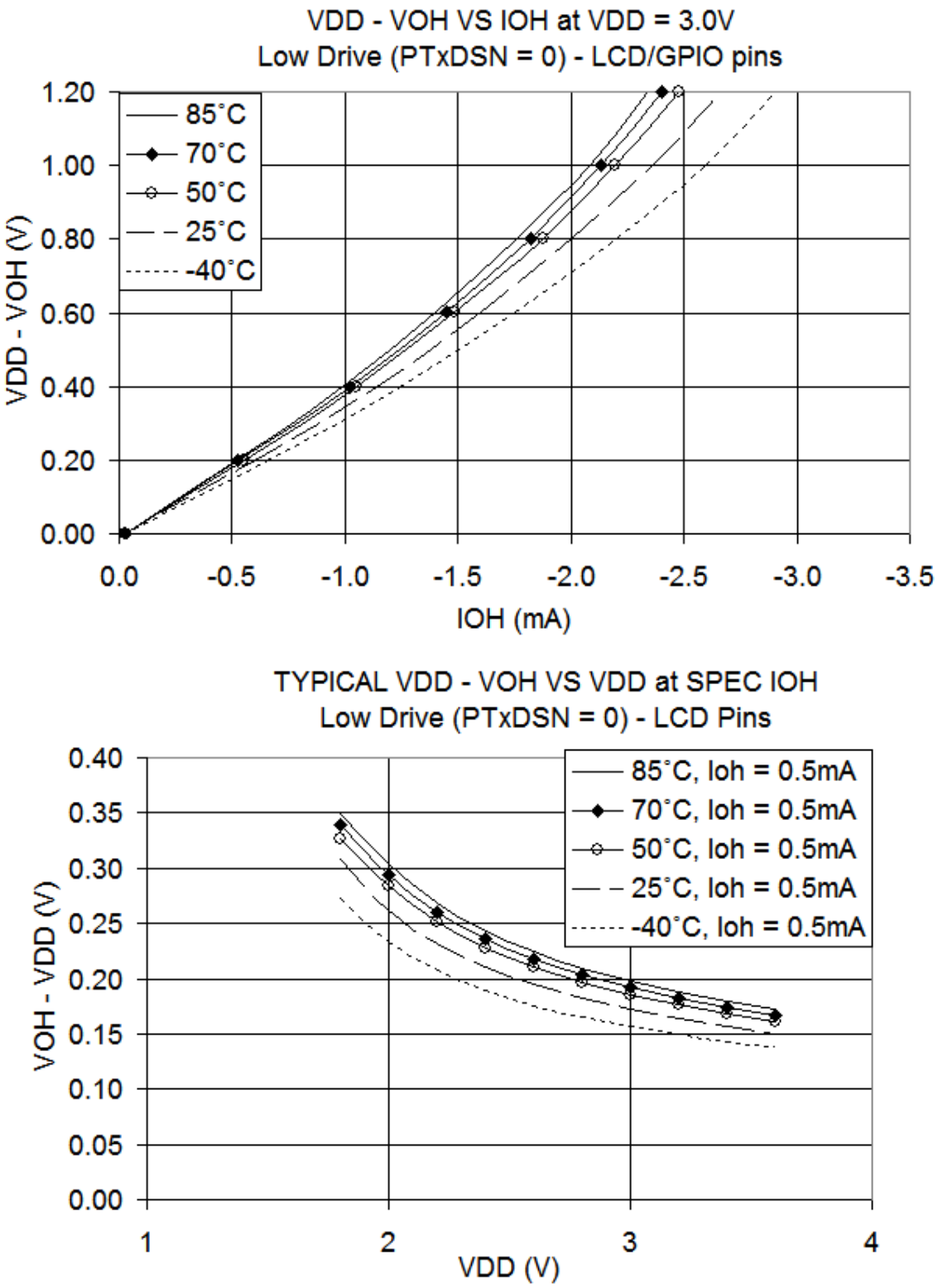

Figure 11. Typical High-Side (Source) Characteristics (LCD/GPIO Pins)— Low Drive (PTxDSn = 0)

3.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 9. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
1	T	Run supply current FEI mode, all modules on	RI_{DD}	20 MHz	3	13.75	17.9	mA	–40 to 85
	T			8 MHz		7	—		
	T			1 MHz		2	—		
2	T	Run supply current FEI mode, all modules off	RI_{DD}	20 MHz	3	8.9	—	mA	–40 to 85
	T			8 MHz		5.5	—		
	T			1 MHz		0.9	—		
3	T	Run supply current LPS=0, all modules off	RI_{DD}	32 kHz FBILP	3	185	—	µA	–-40 to 85
	T			16 kHz FBELP		115	—		
4	T	Run supply current LPS=1, all modules off, running from Flash	RI_{DD}	16 kHz FBELP	3	21.9	—	µA	0 to 70
							—		–40 to 85
	T	Run supply current LPS=1, all modules off, running from RAM				7.3	—		0 to 70
							—		–40 to 85
5	T	Wait mode supply current FEI mode, all modules off	WI_{DD}	20 MHz	3	4.57	6	mA	–40 to 85
	T			8 MHz		2	—		
	T			1 MHz		0.73	—		
6	P	Stop2 mode supply current	$S2I_{DD}$	n/a	3	0.4	1.3	µA	–40 to 25
	C					4	6		70
	P					8.5	13		85
	C				2	0.35	1.0		–40 to 25
	C					3.9	5		70
	C					7.7	10		85
7	P	Stop3 mode supply current No clocks active	$S3I_{DD}$	n/a	3	0.65	1.8	µA	–40 to 25
	C					5.7	8.0		70
	P					12.2	20		85
	C				2	0.6	1.5		–40 to 25
	C					5	6.8		70
	C					11.5	14		85

[1] Typical values are measured at 25 °C. Characterized, not tested

Table 10. Stop Mode Adders

Num	C	Parameter	Condition	Temperature (°C)				Units
				–40	25	70	85	
1	T	LPO		100	100	150	175	nA
2	T	EREFSTEN	RANGE = HGO = 0	750	750	800	850	nA
3	T	IREFSTEN[1]		63	70	77	81	µA
4	T	TOD	Does not include clock source current	50	50	75	100	nA
5	T	LVD[1]	LVDSE = 1	110	110	112	115	µA
6	T	ACMP[1]	Not using the bandgap (BGBE = 0)	12	12	20	23	µA
7	T	ADC[1]	ADLPC = ADLSMP = 1 Not using the bandgap (BGBE = 0)	95	95	101	120	µA
8	T	LCD	VIREG enabled for Contrast control, 1/8 Duty cycle, 8x24 configuration for driving 192 segments, 32 Hz frame rate, No LCD glass connected.	1	1	6	13	µA
9	T	LCD	LCD configured for 1/8 duty cycle, 8x24 configuration for driving 192 segments, 32 Hz frame rate, no LCD glass connected.	0.2	0.24	0.5	0.65	µA

1 Not available in stop2 mode.

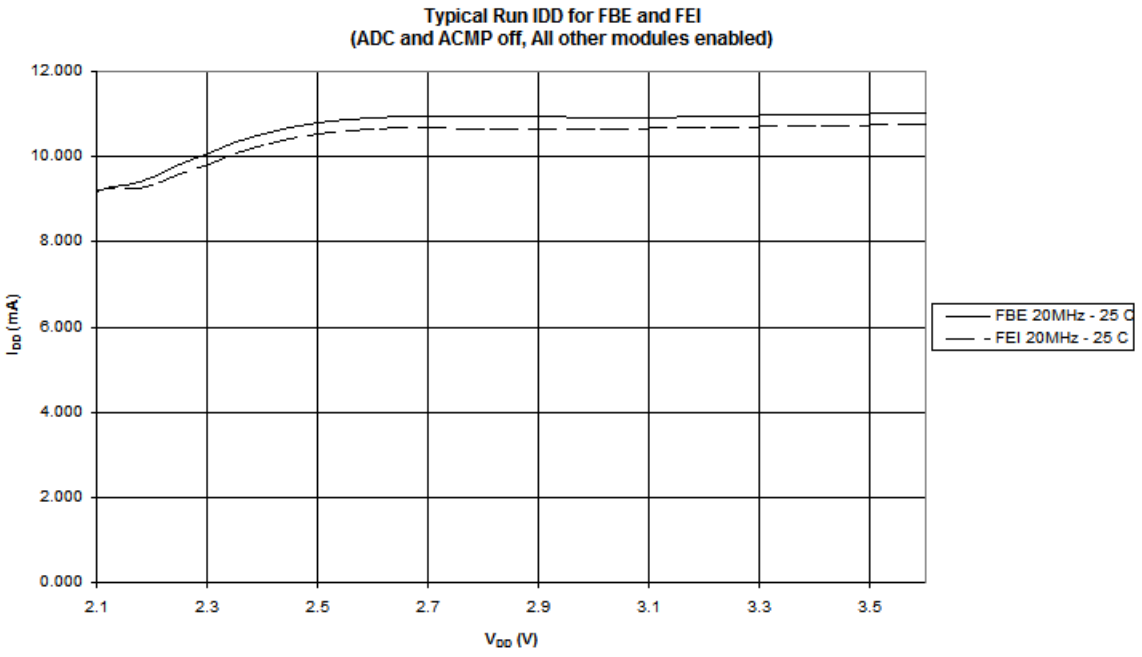

Figure 13. Typical Run I_{DD} for FBE and FEI, I_{DD} vs. V_{DD} (ACMP and ADC off, All Other Modules Enabled)

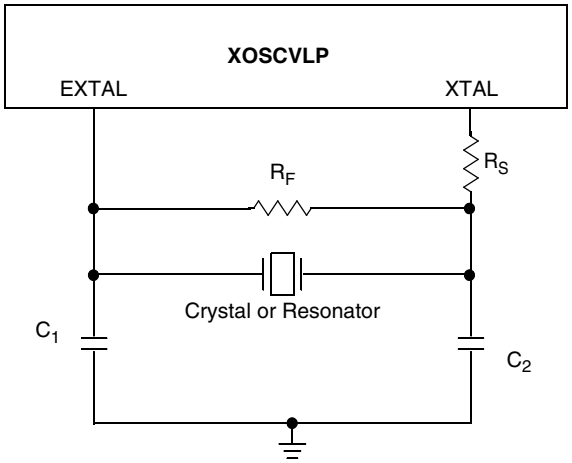

Figure 14. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

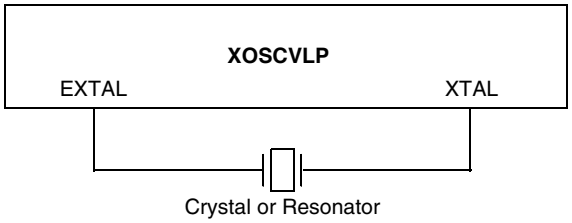

Figure 15. Typical Crystal or Resonator Circuit: Low Range/Low Power

3.9 Internal Clock Source (ICS) Characteristics

Table 12. ICS Frequency Specifications (Temperature Range = –40 to 85 °C Ambient)

Num	C	Characteristic		Symbol	Min	Typ[1]	Max	Unit
1	C	Average internal reference frequency — untrimmed		f_{int_ut}	25	32.7	41.66	kHz
2	P	Average internal reference frequency — user-trimmed		f_{int_t}	31.25	—	39.06	kHz
3	P	Average internal reference frequency — factory-trimmed		f_{int_t}	—	32.7	—	kHz
4	T	Internal reference start-up time		t_{IRST}	—	60	100	µs
5	P	DCO output frequency range — untrimmed	Low range (DFR = 00)	f_{dco_ut}	12.8	16.8	21.33	MHz
	C		Mid range (DFR = 01)		25.6	33.6	42.67	
6	P	DCO output frequency range — trimmed	Low range (DFR = 00)	f_{dco_t}	16	—	20	MHz
	P		Mid range (DFR = 01)		32	—	40	
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$
8	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.2	±0.4	$\%f_{dco}$

Table 17. 16-bit ADC Operating Conditions

Num	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
9	Analog Source Resistance	16 bit modes $f_{ADCK} > 8MHz$ $4MHz < f_{ADCK} < 8MHz$ $f_{ADCK} < 4MHz$	R_{AS}	— — —	— — —	0.5 1 2	kΩ	External to MCU Assumes ADLSMP=0
10		13/12 bit modes $f_{ADCK} > 8MHz$ $4MHz < f_{ADCK} < 8MHz$ $f_{ADCK} < 4MHz$		— — —	— — —	1 2 5		
11		11/10 bit modes $f_{ADCK} > 8MHz$ $4MHz < f_{ADCK} < 8MHz$ $f_{ADCK} < 4MHz$		— — —	— — —	2 5 10		
12		9/8 bit modes $f_{ADCK} > 8MHz$ $f_{ADCK} < 8MHz$		— —	— —	5 10		
13	ADC Conversion Clock Freq.	ADLPC = 0, ADHSC = 1	f_{ADCK}	1.0	—	8	MHz	
14		ADLPC = 0, ADHSC = 0		1.0	—	5		
15		ADLPC = 1, ADHSC = 0		1.0	—	2.5		

1 Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

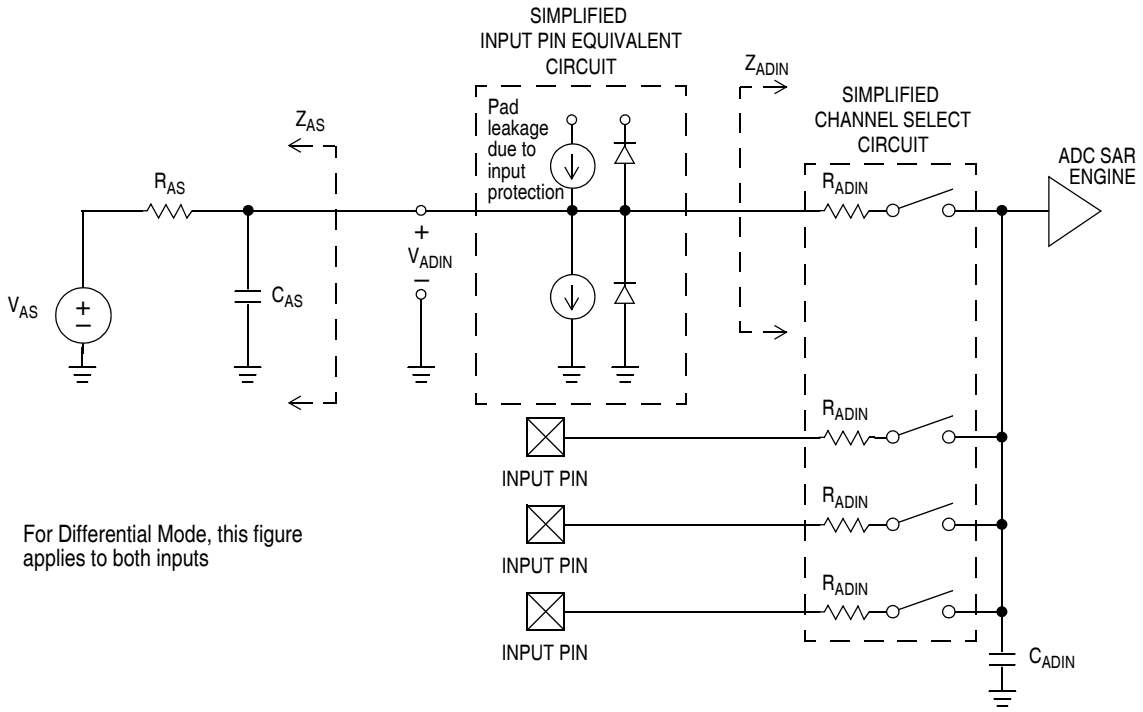

Figure 25. ADC Input Impedance Equivalency Diagram

Table 18. 16-bit ADC Characteristics full operating range($V_{REFH} = V_{DDA} > 1.8$, $V_{REFL} = V_{SSA}$, $F_{ADCK} \leq 8MHz$)

Characteristic	Conditions[1]	C	Symb	Min	Typ[2]	Max	Unit	Comment
Supply Current	ADLPC = 1, ADHSC = 0	T	I_{DDA}	—	215	—	μA	ADLSMP = 0 ADCO = 1
	ADLPC = 0, ADHSC = 0			—	470	—		
	ADLPC=0, ADHSC=1			—	610	—		
Supply Current	Stop, Reset, Module Off	C	I_{DDA}	—	0.01	—	μA	
ADC Asynchronous Clock Source	ADLPC = 1, ADHSC = 0	P	f_{ADACK}	—	2.4	—	MHz	$t_{ADACK} = 1/f_{ADACK}$
	ADLPC = 0, ADHSC = 0			—	5.2	—		
	ADLPC = 0, ADHSC = 1			—	6.2	—		
Sample Time	See reference manual for sample times							
Conversion Time	See reference manual for conversion times							

Table 18. 16-bit ADC Characteristics full operating range($V_{REFH} = V_{DDA} > 1.8$, $V_{REFL} = V_{SSA}$, $F_{ADCK} \leq 8MHz$)

Characteristic	Conditions[1]	C	Symb	Min	Typ[2]	Max	Unit	Comment
Total Unadjusted Error	16-bit differential mode 16-bit single-ended mode	T	TUE	— —	±16 ±20	+48/-40 +56/-28	LSB[3]	32x Hardware Averaging (AVGE = %1 AVGS = %11)
	13-bit differential mode 12-bit single-ended mode	T		— —	±1.5 ±1.75	±3.0 ±3.5		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.7 ±0.8	±1.5 ±1.5		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.5 ±0.5	±1.0 ±1.0		
Differential Non-Linearity	16-bit differential mode 16-bit single-ended mode	T	DNL	— —	±2.5 ±2.5	+5/-3 +5/-3	LSB[2]	
	13-bit differential mode 12-bit single-ended mode	T		— —	±0.7 ±0.7	±1 ±1		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.5 ±0.5	±0.75 ±0.75		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.2 ±0.2	±0.5 ±0.5		
Integral Non-Linearity	16-bit differential mode 16-bit single-ended mode	T	INL	— —	±6.0 ±10.0	±16.0 ±20.0	LSB[2]	
	13-bit differential mode 12-bit single-ended mode	T		— —	±1.0 ±1.0	±2.5 ±2.5		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.5 ±0.5	±1.0 ±1.0		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.3 ±0.3	±0.5 ±0.5		
Zero-Scale Error	16-bit differential mode 16-bit single-ended mode	T	E_{ZS}	— —	±4.0 ±4.0	+32/-24 +24/-16	LSB[2]	$V_{ADIN} = V_{SSA}$
	13-bit differential mode 12-bit single-ended mode	T		— —	±0.7 ±0.7	±2.5 ±2.0		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.4 ±0.4	±1.0 ±1.0		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.2 ±0.2	±0.5 ±0.5		

Table 19. 16-bit ADC Characteristics(V_{REFH} = V_{DDA} ≥ 2.7V, V_{REFL} = V_{SSA}, F_{ADCK} ≤ 4MHz, ADHSC=1)

Characteristic	Conditions[1]	C	Symb	Min	Typ[2]	Max	Unit	Comment
Full-Scale Error	16-bit differential mode 16-bit single-ended mode	T	E_{FS}	— —	+8/0 +12/0	+24/0 +24/0	LSB[2]	V_{ADIN} = V_{DDA}
	13-bit differential mode 12-bit single-ended mode	T		— —	±0.7 ±0.7	±2.0 ±2.5		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.4 ±0.4	±1.0 ±1.0		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.2 ±0.2	±0.5 ±0.5		
Quantization Error	16 bit modes	D	E_Q	—	-1 to 0	—	LSB[2]	
	≤13 bit modes			—	—	±0.5		
Effective Number of Bits	16 bit differential mode Avg=32 Avg=16 Avg=8 Avg=4 Avg=1	C	ENOB	 14.3 13.8 13.4 13.1 12.4	 14.5 14.0 13.7 13.4 12.6	 — — — — —	Bits	F_{in} = F_{sample}/100
	16 bit single-ended mode Avg=32 Avg=16 Avg=8 Avg=4 Avg=1			 TBD TBD TBD TBD TBD	 13.5 13.0 12.7 12.4 11.6	 — — — — —		
Signal to Noise plus Distortion	See ENOB		SINAD	SINAD = 6.02 *ENOB +1.76			dB	
Total Harmonic Distortion	16 bit differential mode Avg=32	C	THD	—	-95.8	-90.4	dB	F_{in} = F_{sample}/100
	16 bit single-ended mode Avg=32	D		—	—	—		
Spurious Free Dynamic Range	16 bit differential mode Avg=32	C	SFDR	91.0	96.5	—	dB	F_{in} = F_{sample}/100
	16 bit single-ended mode Avg=32	D		—	—	—		
Input Leakage Error	all modes	D	E_{IL}	I_{In} * R_{AS}			mV	I_{In} = leakage current (refer to DC characteristics)
Temp Sensor Slope	-40 °C– 25 °C	D	m	—	1.646	—	mV/°C	
	25 °C– 125 °C			—	1.769	—		
Temp Sensor Voltage	25 °C	D	V_{TEMP25}	—	701.2	—	mV	

[1] All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDA}

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

3 The program and erase currents are additional to the standard run I_{DD}. These values are measured at room temperatures with V_{DD} = 3.0 V, bus frequency = 4.0 MHz.

3.16 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 available on www.freescale.com for advice and guidance specifically targeted at optimizing EMC performance.

3.16.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East).

4 Ordering Information

This appendix contains ordering information for the device numbering system.

Table 23. Device Numbering System

Device Number[1]	Memory		Available Packages[2]
	Flash	RAM	
MC9S08LH64	64 KB	4000	80-pin LQFP
	64 KB	4000	64-pin LQFP
MC9S08LH36	36 KB	4000	80-pin LQFP
	36 KB	4000	64-pin LQFP

1 See Table 1 for a complete description of modules included on each device.

2 See Table 24 for package information.

4.1 Device Numbering System

Example of the device numbering system: