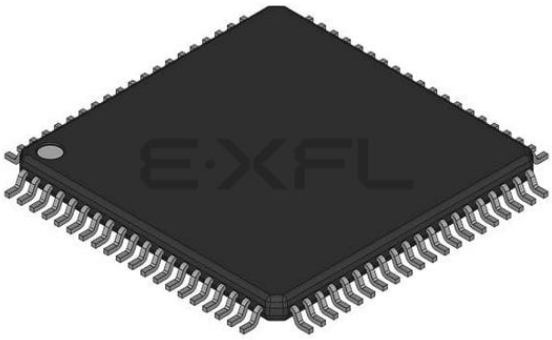

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Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	LCD, LVD, PWM, WDT
Number of I/O	39
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s08lh64clk

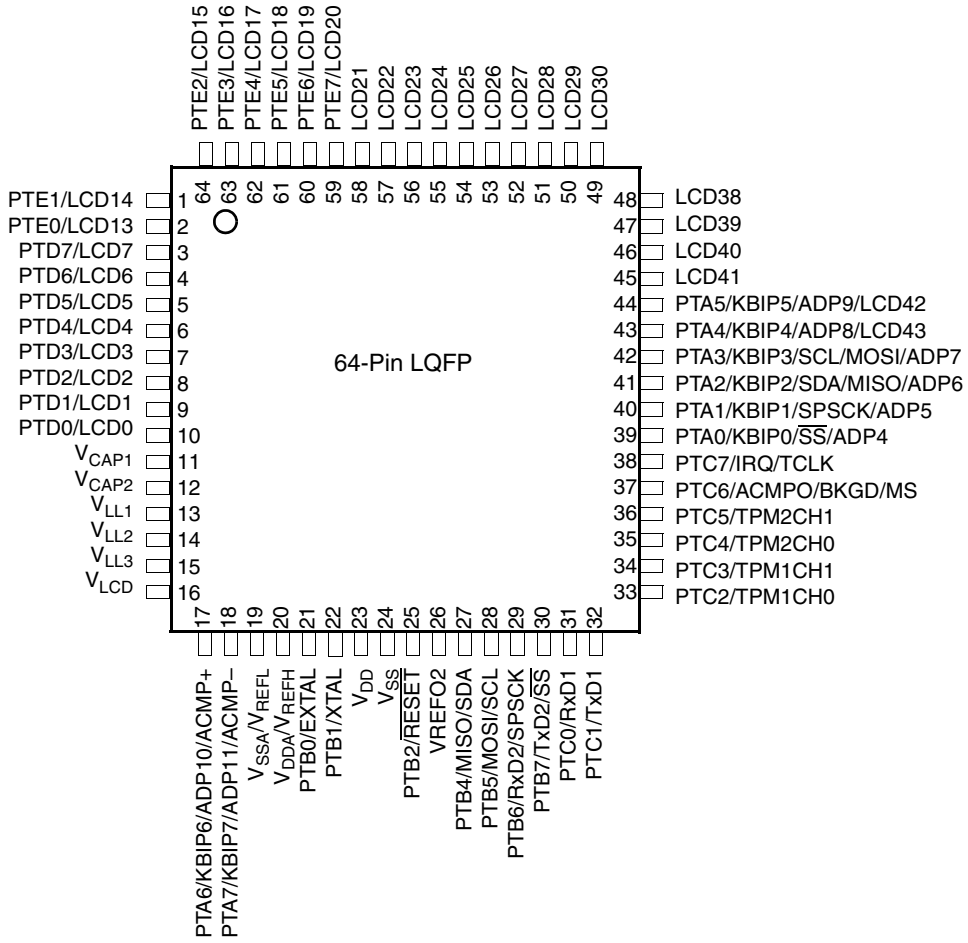


Figure 2. 64-Pin LQFP

Table 2. Pin Availability by Package Pin-Count (continued)

		<-- Lowest **Priority** --> Highest				
80	**64**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt3**	**Alt4**
9	5	PTD5	LCD5			
10	6	PTD4	LCD4			
11	7	PTD3	LCD3			
12	8	PTD2	LCD2			
13	9	PTD1	LCD1			
14	10	PTD0	LCD0			
15	11	V_{CAP1}				
16	12	V_{CAP2}				
17	13	V_{LL1}				
18	14	V_{LL2}				
19	15	V_{LL3}				
20	16	V_{LCD}				
21	17	PTA6	KBIP6	ADP10	ACMP+	
22	18	PTA7	KBIP7	ADP11	ACMP–	
23	19	V_{SSA}				
24		V_{REFL}				
25		DADP0				
26		DADM0				
27		VREFO1				
28	20	V_{REFH}				
29		V_{DDA}				
30	21	PTB0		EXTAL		
31	22	PTB1		XTAL		
32	23	V_{DD}				
33	24	V_{SS}				
34	25	PTB2	$\overline{\text{RESET}}$			
	26	VREFO2				
35	27	PTB4	MISO	SDA		
36	28	PTB5	MOSI	SCL		
37	29	PTB6	RxD2	SPSCK		
38	30	PTB7	TxD2	$\overline{\text{SS}}$		
39	31	PTC0	RxD1			
40	32	PTC1	TxD1			
41	33	PTC2	TPM1CH0			
42	34	PTC3	TPM1CH1			
43	35	PTC4	TPM2CH0			
44	36	PTC5	TPM2CH1			
45	37	PTC6	ACMPO	BKGD	MS	

3 Electrical Characteristics

3.1 Introduction

This section contains electrical and timing specifications for the MC9S08LH64 Series of microcontrollers available at the time of publication.

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 3. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 4 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pullup resistor associated with the pin is enabled.

Table 4. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +3.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	± 25	mA
Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins, except for PTB2 are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 5. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H –40 to 85	°C
Maximum junction temperature	T_J	95	°C
Thermal resistance Single-layer board			
80-pin LQFP	θ_{JA}	55	°C/W
64-pin LQFP		73	
Thermal resistance Four-layer board			
80-pin LQFP	θ_{JA}	42	°C/W
64-pin LQFP		54	

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273\ °C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273\ °C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be taken to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification, ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless instructed otherwise in the device specification.

Table 6. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body Model	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	3	
Charge Device Model	Series resistance	R1	0	Ω
	Storage capacitance	C	200	pF
	Number of pulses per pin	—	3	

Table 6. ESD and Latch-up Test Conditions (continued)

Latch-up	Minimum input voltage limit		–2.5	V
	Maximum input voltage limit		7.5	V

Table 7. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	±2000	—	V
2	Charge device model (CDM)	V_{CDM}	±500	—	V
3	Latch-up current at T_A = 85 °C	I_{LAT}	±100	—	mA

1 Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

3.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 8. DC Characteristics

Num	C	Characteristic	Symbol	Condition	Min	Typ[1]	Max	Unit
1		Operating Voltage			1.8		3.6	V
2	C	Output high voltage — PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7][2], low-drive strength	V_{OH}	V_{DD} >1.8 V, I_{Load} = –0.6 mA	V_{DD} – 0.5	—	—	V
	P	Output high voltage — PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7][2], high-drive strength		V_{DD} > 2.7 V, I_{Load} = –10 mA	V_{DD} – 0.5	—	—	
	C			V_{DD} > 1.8 V, I_{Load} = –3 mA	V_{DD} – 0.5	—	—	
3	C	Output high voltage — PTA[4:5], PTD[0:7], PTE[0:7], low-drive strength	V_{OH}	V_{DD} > 1.8 V, I_{Load} = –0.5 mA	V_{DD} – 0.5	—	—	V
	P	Output high voltage — PTA[4:5], PTD[0:7], PTE[0:7], high-drive strength		V_{DD} > 2.7 V, I_{Load} = –2.5 mA	V_{DD} – 0.5	—	—	
	C			V_{DD} > 1.8 V, I_{Load} = –1 mA	V_{DD} – 0.5	—	—	
4	D	Output high current — Max total I_{OH} for all ports	I_{OHT}		—	—	100	mA
5	C	Output low voltage — PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7], low-drive strength	V_{OL}	V_{DD} >1.8 V, I_{Load} = 0.6 mA	—	—	0.5	V
	P	Output low voltage — PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7], high-drive strength		V_{DD} > 2.7 V, I_{Load} = 10 mA	—	—	0.5	
	C			V_{DD} > 1.8 V, I_{Load} = 3 mA	—	—	0.5	

Table 8. DC Characteristics (continued)

Num	C	Characteristic	Symbol	Condition	Min	Typ[1]	Max	Unit
6	C	Output low voltage — PTA[4:5], PTD[0:7], PTE[0:7], low-drive strength	V_{OL}	V_{DD} > 1.8 V, I_{Load} = 0.5 mA	—	—	0.5	V
	P	Output low voltage — PTA[4:5], PTD[0:7], PTE[0:7], high-drive strength		V_{DD} > 2.7 V, I_{Load} = 3 mA	—	—	0.5	
	C			V_{DD} > 1.8 V, I_{Load} = 1 mA	—	—	0.5	
7	D	Output low current — Max total I_{OL} for all ports	I_{OLT}		—	—	100	mA
8	P	Input high voltage — all digital inputs	V_{IH}	V_{DD} > 2.7 V	0.70 x V_{DD}	—	—	V
	C			V_{DD} > 1.8 V	0.85 x V_{DD}	—	—	
9	P	Input low voltage — all digital inputs	V_{IL}	V_{DD} > 2.7 V	—	—	0.35 x V_{DD}	
	C			V_{DD} > 1.8 V	—	—	0.30 x V_{DD}	
10	C	Input hysteresis — all digital inputs	V_{hys}		0.06 x V_{DD}	—	—	mV
11	P	Input leakage current — all input only pins except for LCD only pins (LCD 8-12, 21-41)	$\lvert I_{In} \rvert$	V_{In} = V_{DD}	—	0.025	1	µA
				V_{In} = V_{SS}	—	0.025	1	µA
		Input leakage current — LCD only pins (LCD 8-12, 21-41)		V_{In} = V_{DD}	—	100	150	µA
				V_{In} = V_{SS}	—	0.025	1	µA
12	P	Hi-Z (off-state) leakage current — all input/output (per pin)	$\lvert I_{OZ} \rvert$	V_{In} = V_{DD} or V_{SS}	—	0.025	1	µA
13	P	Total leakage current[3] — Total leakage current for all pins	$\lvert I_{InT} \rvert$	V_{In} = V_{DD} or V_{SS}	—	—	3	µA
14	P	Pullup, Pulldown resistors — all non-LCD pins when enabled	R_{PU}, R_{PD}		17.5	—	52.5	kΩ
15	P	Pullup, Pulldown resistors — LCD/GPIO pins when enabled	R_{PU}, R_{PD}		35	—	77	kΩ
16	D	DC injection current[4, 5, 6] — Single pin limit	I_{IC}	V_{IN} < V_{SS}, V_{IN} > V_{DD}	–0.2	—	0.2	mA
		DC injection current[4, 5, 6] — Total MCU limit, includes sum of all stressed pins			–5	—	5	mA
17	C	Input Capacitance, all pins	C_{In}		—	—	8	pF
18	C	RAM retention voltage	V_{RAM}		—	0.6	1.0	V
19	C	POR re-arm voltage[7]	V_{POR}		0.9	1.4	2.0	V
20	D	POR re-arm time	t_{POR}		10	—	—	µs
21	P	Low-voltage detection threshold	V_{LVD}	V_{DD} falling V_{DD} rising	1.80 1.88	1.84 1.92	1.88 1.96	V

Table 8. DC Characteristics (continued)

Num	C	Characteristic	Symbol	Condition	Min	Typ[1]	Max	Unit
22	P	Low-voltage warning threshold	V_{LVW}	V_{DD} falling V_{DD} rising	2.08	2.14	2.2	V
23	P	Low-voltage inhibit reset/recover hysteresis	V_{hys}		—	80	—	mV
24	P	Bandgap Voltage Reference[8]	V_{BG}		1.15	1.17	1.18	V

1 Typical values are measured at 25 °C. Characterized, not tested

2 All I/O pins except for LCD pins in Open Drain mode.

3 Total leakage current is the sum value for all GPIO pins. This leakage current is not distributed evenly across all pins but characterization data shows that individual pin leakage current maximums are less than 250 nA.

4 All functional non-supply pins, except for PTB2 are internally clamped to V_{SS} and V_{DD}.

5 Input current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

6 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

7 POR will occur below the minimum voltage.

8 Factory trimmed at V_{DD} = 3.0 V, Temp = 25 °C

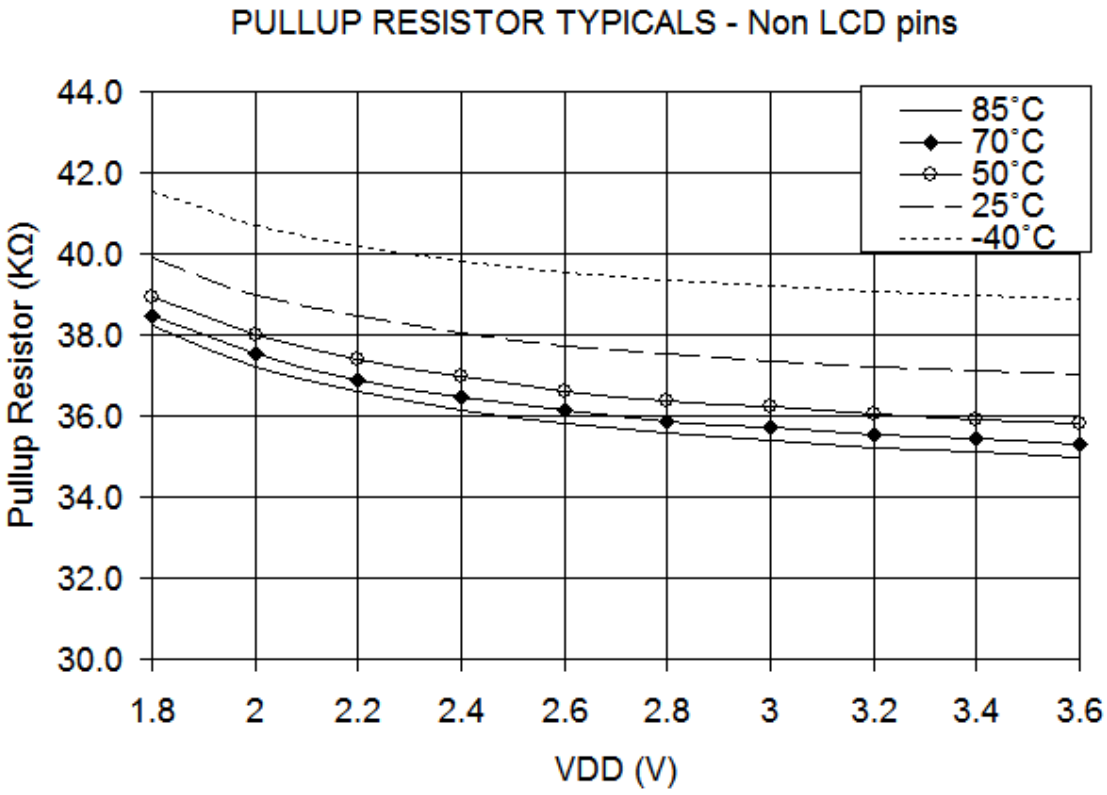


Figure 4. Non LCD pins I/O Pullup Typical Resistor Values

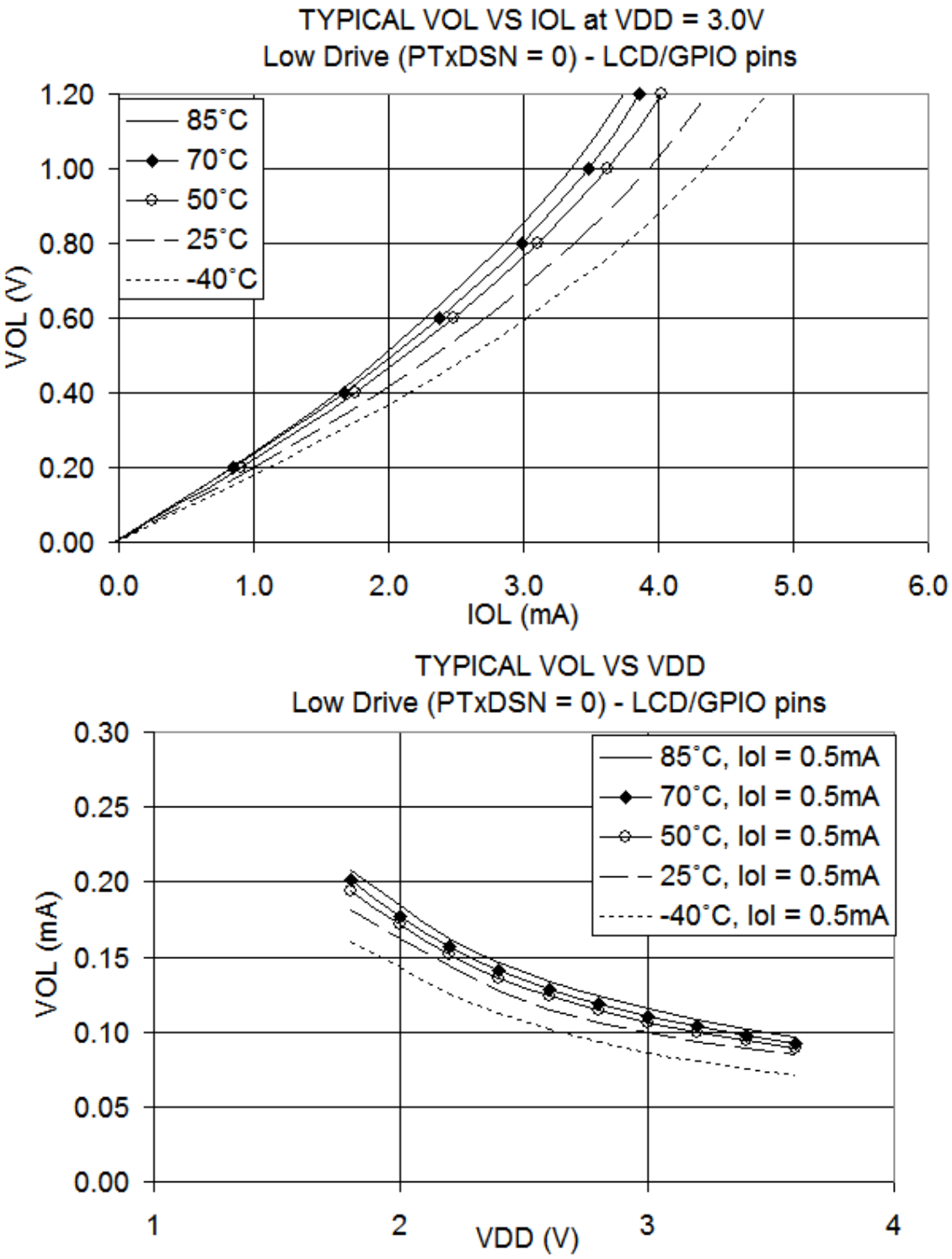


Figure 9. Typical Low-Side Driver (Sink) Characteristics (LCD/GPIO Pins)— Low Drive (PTxDSn = 0)

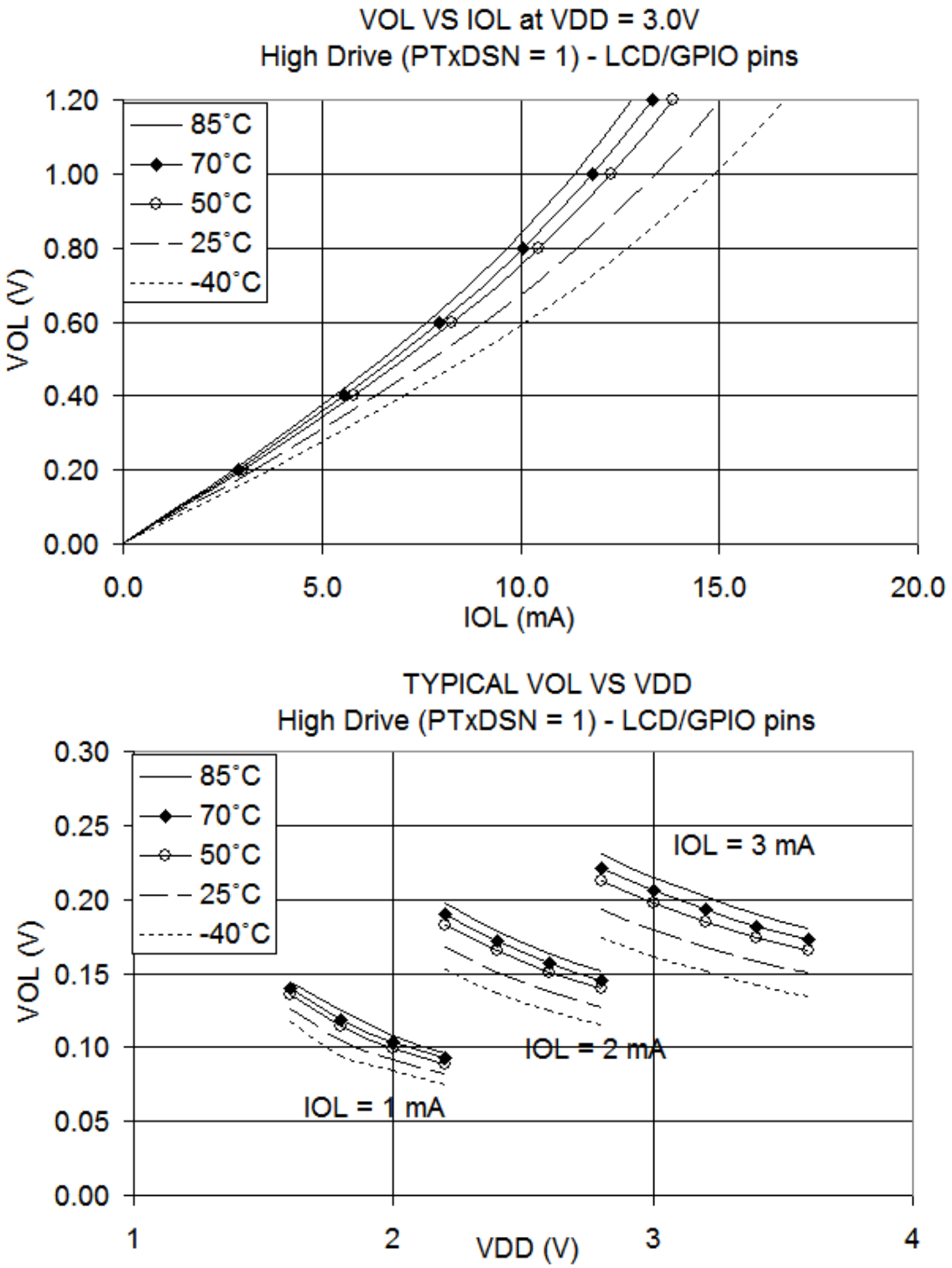


Figure 10. Typical Low-Side Driver (Sink) Characteristics (LCD/GPIO Pins) — High Drive (PTxDSn = 1)

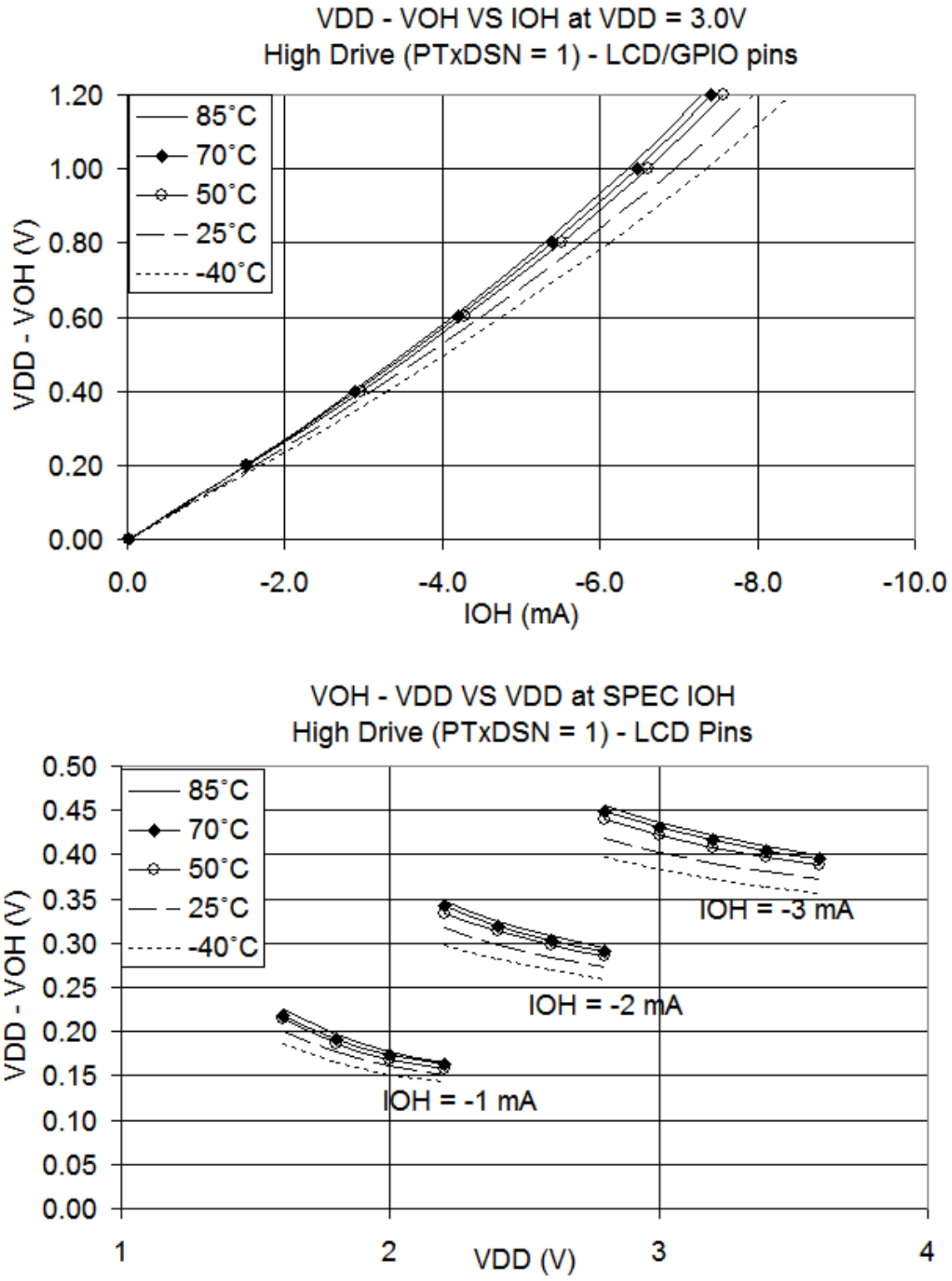


Figure 12. Typical High-Side (Source) Characteristics (LCD/GPIO Pins) — High Drive (PTxDSn = 1)

3.8 External Oscillator (XOSCVLP) Characteristics

See Figure 14 and Figure 15 for crystal or resonator circuits.

Table 11. XOSCVLP and ICS Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1), high gain (HGO = 1) High range (RANGE = 1), low power (HGO = 0)	 f_{lo} f_{hi} f_{hi}	 32 1 1	 — — —	 38.4 16 8	 kHz MHz MHz
2	D	Load capacitors Low range (RANGE=0), low power (HGO=0) Other oscillator settings	C_1, C_2	See Note [2] See Note [3]			
3	D	Feedback resistor Low range, low power (RANGE=0, HGO=0)[2] Low range, high gain (RANGE=0, HGO=1) High range (RANGE=1, HGO=X)	R_F	 — — —	 — 10 1	 — — —	MΩ
4	D	Series resistor — Low range, low power (RANGE = 0, HGO = 0)[2] Low range, high gain (RANGE = 0, HGO = 1) High range, low power (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 — 100 0 0 0 0	 — — — 0 10 20	kΩ
5	C	Crystal start-up time [4] Low range, low power Low range, high gain High range, low power High range, high gain	 t_{CSTL} t_{CSTH}	 — — — —	 600 400 5 15	 — — — —	ms
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE mode FBE or FBELP mode	f_{extal}	 0.03125 0	 — —	 20 20	 MHz MHz

1 Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

2 Load capacitors (C_1, C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE=HGO=0.

3 See crystal or resonator manufacturer's recommendation.

4 Proper PC board layout procedures must be followed to achieve specifications.

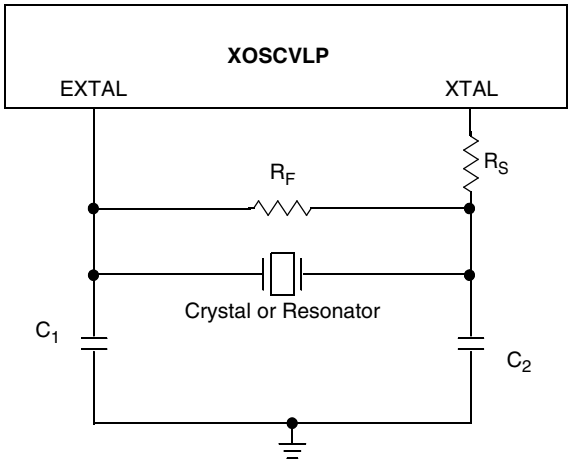


Figure 14. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

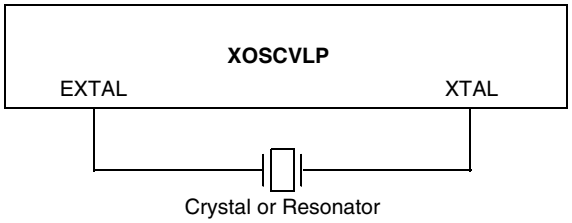


Figure 15. Typical Crystal or Resonator Circuit: Low Range/Low Power

3.9 Internal Clock Source (ICS) Characteristics

Table 12. ICS Frequency Specifications (Temperature Range = –40 to 85 °C Ambient)

Num	C	Characteristic		Symbol	Min	Typ[1]	Max	Unit
1	C	Average internal reference frequency — untrimmed		f_{int_ut}	25	32.7	41.66	kHz
2	P	Average internal reference frequency — user-trimmed		f_{int_t}	31.25	—	39.06	kHz
3	P	Average internal reference frequency — factory-trimmed		f_{int_t}	—	32.7	—	kHz
4	T	Internal reference start-up time		t_{IRST}	—	60	100	µs
5	P	DCO output frequency range — untrimmed	Low range (DFR = 00)	f_{dco_ut}	12.8	16.8	21.33	MHz
	C		Mid range (DFR = 01)		25.6	33.6	42.67	
6	P	DCO output frequency range — trimmed	Low range (DFR = 00)	f_{dco_t}	16	—	20	MHz
	P		Mid range (DFR = 01)		32	—	40	
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$
8	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.2	±0.4	$\%f_{dco}$

Table 12. ICS Frequency Specifications (Temperature Range = –40 to 85 °C Ambient) (continued)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
9	C	Total deviation of trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	+0.5 –1.0	±2	$\%f_{dco}$
10	C	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0 °C to 70 °C	Δf_{dco_t}	—	±0.5	±1	$\%f_{dco}$
11	C	FLL acquisition time[2]	$t_{Acquire}$	—	—	1	ms
12	C	Long term jitter of DCO output clock (averaged over 2-ms interval)[3]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1 Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

2 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

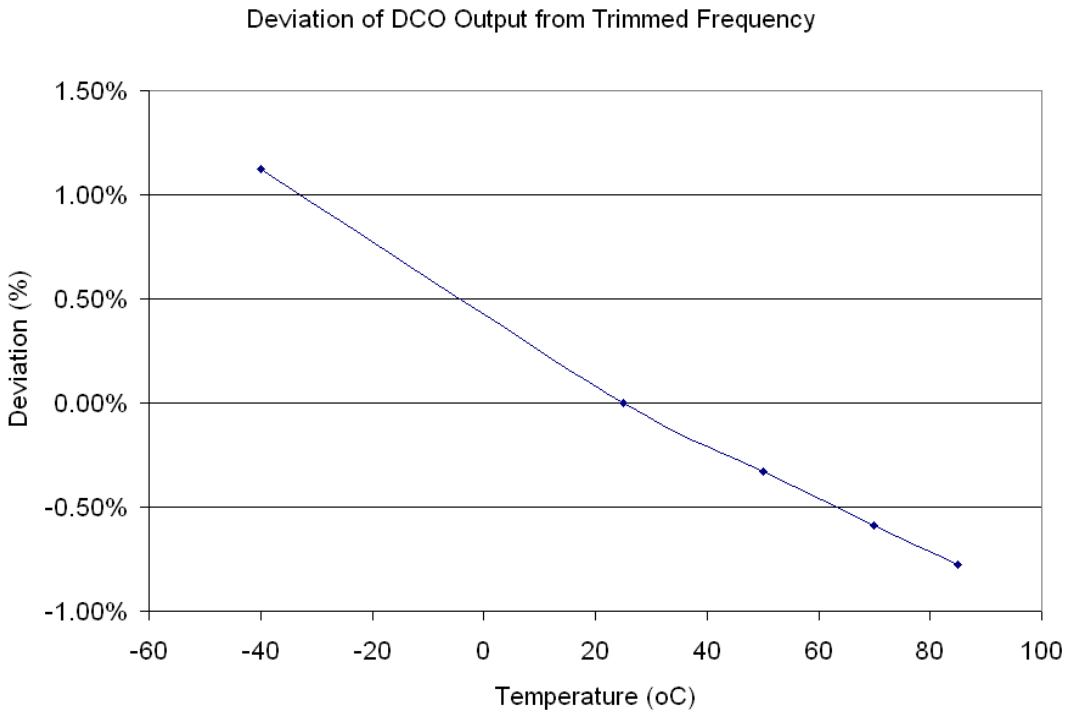
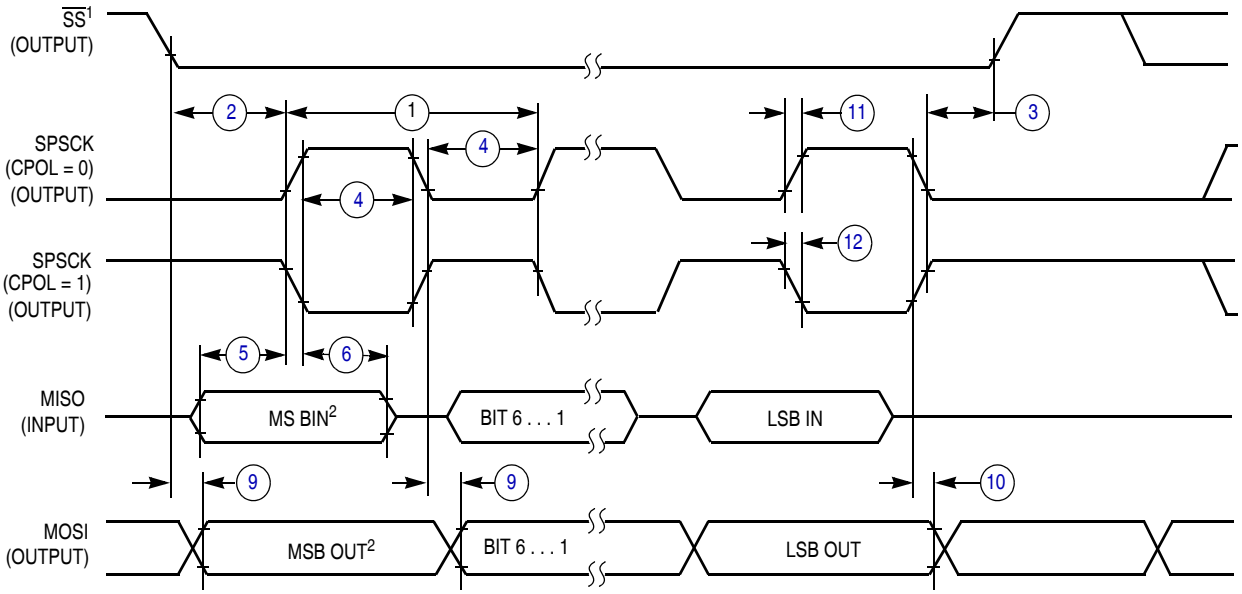


Figure 16. Deviation of DCO Output from Trimmed Frequency (20 MHz, 3.0 V)

3.10 AC Characteristics

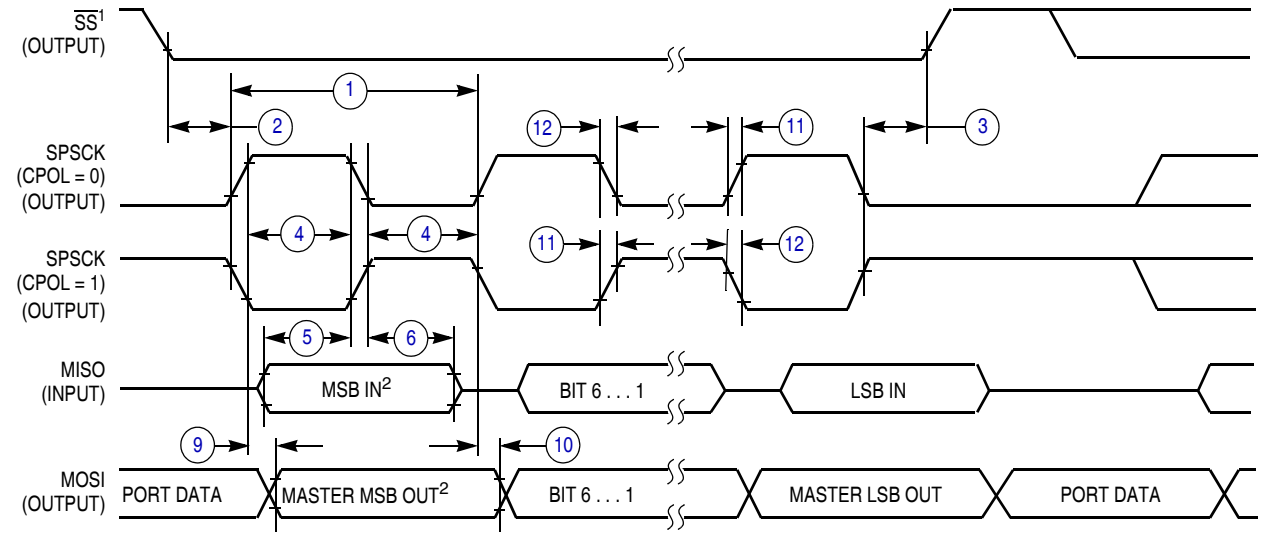
This section describes timing characteristics for each peripheral system.



NOTES:

1. SS output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 21. SPI Master Timing (CPHA = 0)



NOTES:

1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 22. SPI Master Timing (CPHA =1)

3.11 Analog Comparator (ACMP) Electricals

Table 16. Analog Comparator Electrical Specifications

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	V_{DD}	1.8	—	3.6	V
P	Supply current (active)	I_{DDAC}	—	20	35	μA
D	Analog input voltage	V_{AIN}	V_{SS} – 0.3	—	V_{DD}	V
P	Analog input offset voltage	V_{AIO}		20	40	mV
C	Analog comparator hysteresis	V_H	3.0	9.0	15.0	mV
P	Analog input leakage current	I_{ALKG}	—	—	1.0	μA
C	Analog comparator initialization delay	t_{AINIT}	—	—	1.0	μs

3.12 ADC Characteristics

Table 17. 16-bit ADC Operating Conditions

Num	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
1	Supply voltage	Absolute	V_{DDA}	1.8	—	3.6	V	
2		Delta to V_{DD} (V_{DD}–V_{DDA})[2]	ΔV_{DDA}	–100	0	100	mV	
3	Ground voltage	Delta to V_{SS} (V_{SS}–V_{SSA})[2]	ΔV_{SSA}	–100	0	100	mV	
4	Ref Voltage High		V_{REFH}	1.15	V_{DDA}	V_{DDA}	V	
5	Ref Voltage Low		V_{REFL}	V_{SSA}	V_{SSA}	V_{SSA}	V	
6	Input Voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
7	Input Capacitance	16-bit modes 8/10/12-bit modes	C_{ADIN}	—	8 4	10 5	pF	
8	Input Resistance		R_{ADIN}	—	2	5	kΩ	

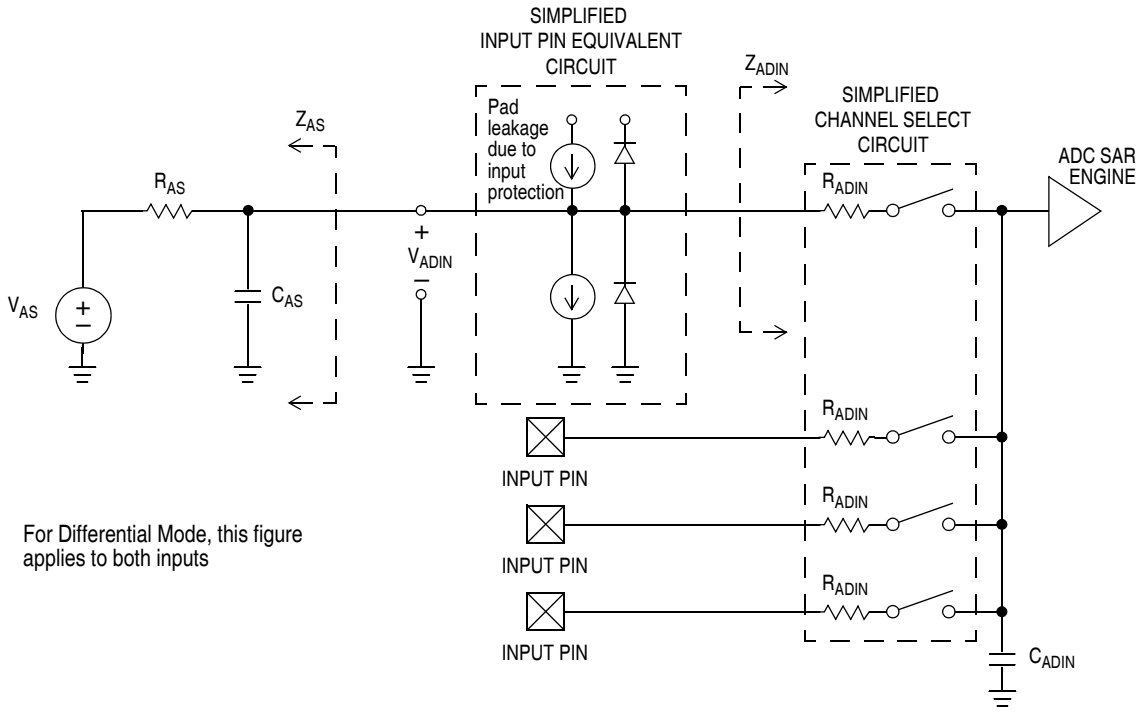


Figure 25. ADC Input Impedance Equivalency Diagram

Table 18. 16-bit ADC Characteristics full operating range($V_{REFH} = V_{DDA} > 1.8$, $V_{REFL} = V_{SSA}$, $F_{ADCK} \leq 8MHz$)

Characteristic	Conditions[1]	C	Symb	Min	Typ[2]	Max	Unit	Comment
Supply Current	ADLPC = 1, ADHSC = 0	T	I_{DDA}	—	215	—	μA	ADLSMP = 0 ADCO = 1
	ADLPC = 0, ADHSC = 0			—	470	—		
	ADLPC=0, ADHSC=1			—	610	—		
Supply Current	Stop, Reset, Module Off	C	I_{DDA}	—	0.01	—	μA	
ADC Asynchronous Clock Source	ADLPC = 1, ADHSC = 0	P	f_{ADACK}	—	2.4	—	MHz	$t_{ADACK} = 1/f_{ADACK}$
	ADLPC = 0, ADHSC = 0			—	5.2	—		
	ADLPC = 0, ADHSC = 1			—	6.2	—		
Sample Time	See reference manual for sample times							
Conversion Time	See reference manual for conversion times							

Table 18. 16-bit ADC Characteristics full operating range($V_{REFH} = V_{DDA} > 1.8$, $V_{REFL} = V_{SSA}$, $F_{ADCK} \leq 8MHz$)

Characteristic	Conditions[1]	C	Symb	Min	Typ[2]	Max	Unit	Comment
Total Unadjusted Error	16-bit differential mode 16-bit single-ended mode	T	TUE	— —	±16 ±20	+48/-40 +56/-28	LSB[3]	32x Hardware Averaging (AVGE = %1 AVGS = %11)
	13-bit differential mode 12-bit single-ended mode	T		— —	±1.5 ±1.75	±3.0 ±3.5		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.7 ±0.8	±1.5 ±1.5		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.5 ±0.5	±1.0 ±1.0		
Differential Non-Linearity	16-bit differential mode 16-bit single-ended mode	T	DNL	— —	±2.5 ±2.5	+5/-3 +5/-3	LSB[2]	
	13-bit differential mode 12-bit single-ended mode	T		— —	±0.7 ±0.7	±1 ±1		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.5 ±0.5	±0.75 ±0.75		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.2 ±0.2	±0.5 ±0.5		
Integral Non-Linearity	16-bit differential mode 16-bit single-ended mode	T	INL	— —	±6.0 ±10.0	±16.0 ±20.0	LSB[2]	
	13-bit differential mode 12-bit single-ended mode	T		— —	±1.0 ±1.0	±2.5 ±2.5		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.5 ±0.5	±1.0 ±1.0		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.3 ±0.3	±0.5 ±0.5		
Zero-Scale Error	16-bit differential mode 16-bit single-ended mode	T	E_{ZS}	— —	±4.0 ±4.0	+32/-24 +24/-16	LSB[2]	$V_{ADIN} = V_{SSA}$
	13-bit differential mode 12-bit single-ended mode	T		— —	±0.7 ±0.7	±2.5 ±2.0		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.4 ±0.4	±1.0 ±1.0		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.2 ±0.2	±0.5 ±0.5		

Table 18. 16-bit ADC Characteristics full operating range(V_{REFH} = V_{DDA} > 1.8, V_{REFL} = V_{SSA}, F_{ADCK} ≤ 8MHz)

Characteristic	Conditions[1]	C	Symb	Min	Typ[2]	Max	Unit	Comment
Full-Scale Error	16-bit differential mode 16-bit single-ended mode	T	E_{FS}	— —	+10/0 +14/0	+42/-2 +46/-2	LSB[2]	V_{ADIN} = V_{DDA}
	13-bit differential mode 12-bit single-ended mode	T		— —	±1.0 ±1.0	±3.5 ±3.5		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.4 ±0.4	±1.5 ±1.5		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.2 ±0.2	±0.5 ±0.5		
Quantization Error	16-bit modes	D	E_Q	—	-1 to 0	—	LSB[2]	
	≤13-bit modes			—	—	±0.5		
Effective Number of Bits	16-bit differential mode Avg = 32 Avg = 16 Avg = 8 Avg = 4 Avg = 1	C	ENOB	 12.8 12.7 12.6 12.5 11.9	 14.2 13.8 13.6 13.3 12.5	 — — — — —	Bits	F_{in} = F_{sample}/100
	16-bit single-ended mode Avg = 32 Avg = 16 Avg = 8 Avg = 4 Avg = 1	D		 — — — — —	 13.2 12.8 12.6 12.3 11.5	 — — — — —		
Signal to Noise plus Distortion	See ENOB		SINAD	$SINAD = 6.02 \cdot ENOB + 1.76$			dB	
Total Harmonic Distortion	16-bit differential mode Avg = 32	C	THD	—	-91.5	-74.3	dB	F_{in} = F_{sample}/100
	16-bit single-ended mode Avg = 32	D		—	-85.5	—		
Spurious Free Dynamic Range	16-bit differential mode Avg = 32	C	SFDR	75.0	92.2	—	dB	F_{in} = F_{sample}/100
	16-bit single-ended mode Avg = 32	D		—	86.2	—		
Input Leakage Error	all modes	D	E_{IL}	I_{In} * R_{AS}			mV	I_{In} = leakage current (refer to DC characteristics)
Temp Sensor Slope	-40 °C– 25 °C	C	m	—	1.646	—	mV/°C	
	25 °C– 125 °C			—	1.769	—		
Temp Sensor Voltage	25 °C	C	V_{TEMP25}	—	701.2	—	mV	

3.14 LCD Specifications

Table 21. LCD Electricals, 3-V Glass

#	C	Characteristic	Symbol	Min	Typ	Max	Unit
1	D	LCD Supply Voltage	V_{LCD}	0.9	1.5	1.8	V
2	D	LCD Frame Frequency	f_{Frame}	28	30	58	Hz
3	D	LCD Charge Pump Capacitance	C_{LCD}	—	100	100	nF
4	D	LCD Bypass Capacitance	C_{BYLCD}	—	100	100	nF
5	D	LCD Glass Capacitance	C_{glass}	—	2000	8000	pF
6	D	V_{IREG} HRefSel = 0	V_{IREG}	0.89	1.00	1.15	V
7		V_{IREG} HRefSel = 1		1.49	1.67	1.85[1]	
8	D	V_{IREG} TRIM Resolution	Δ_{RTRIM}	1.5	—	—	% V_{IREG}
9	D	V_{IREG} Ripple HRefSel = 0	—	—	—	0.1	V
10		HRefSel = 1	—	—	—	0.15	
11	D	V_{LCD} Buffered Adder[2]	I_{Buff}	—	1		µA

1 V_{IREG} Max can not exceed V_{DD} – 0.15 V

2 VSUPPLY = 10, BYPASS = 0

3.15 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section of the reference manual.

Table 22. Flash Characteristics

#	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	D	Supply voltage for program/erase –40 °C to 85 °C	$V_{prog/erase}$	1.8	—	3.6	V
2	D	Supply voltage for read operation	V_{Read}	1.8	—	3.6	V
3	D	Internal FCLK frequency[1]	f_{FCLK}	150	—	200	kHz
4	D	Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	µs
5	P	Byte program time (random location)[2]	t_{prog}	9			t_{Fcyc}
6	P	Byte program time (burst mode)[2]	t_{Burst}	4			t_{Fcyc}
7	P	Page erase time[2]	t_{Page}	4000			t_{Fcyc}
8	P	Mass erase time[2]	t_{Mass}	20,000			t_{Fcyc}
9	D	Byte program current[3]	R_{IDDBP}	—	4	—	mA

1 The frequency of this clock is controlled by a software setting.