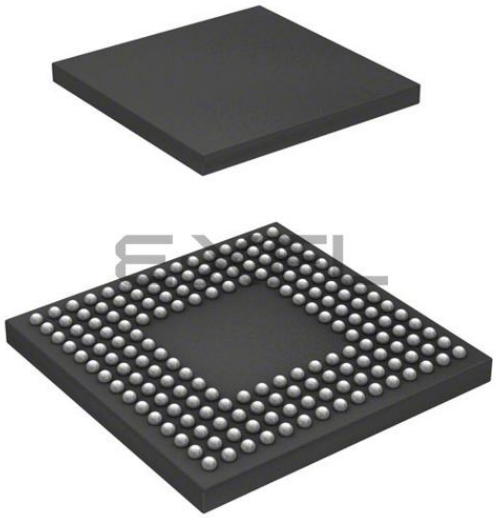
Renesas Electronics America Inc - R5F56216BDBG#U0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	126
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10/12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LFBGA
Supplier Device Package	176-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f56216bdbg-u0

1.4 Pin Assignments

Figure 1.3 to Figure 1.9 show the pins assignments. Table 1.4 to Table 1.8 show the list of pins and pin functions.

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
15	PE1	P70	PE6	P65	P67	PG5	PA1	PA3	PA6	PB0	VCC	PB2	PB5	PB7	P75	15
14	P63	PE2	PE5	PE7	P66	PA0	PG6	PA4	PA7	P72	PB3	PB6	P73	PC1	P77	14
13	P61	P64	PE3	PE4	VCC	PG3	VCC	PA2	PA5	P71	PB4	VCC	P74	P76	P80	13
12	PD7	P62	PE0	VSS	PG2	PG4	VSS	PG7	VSS	PB1	VSS	PC0	PC2	PC4	PC7	12
11	PG0	P60	VCC	VSS								P81	PC3	P82	P83	11
10	PD4	PD6	PD5	PG1								PC6	PC5	P50	P53	10
9	PD3	P97	VCC	VSS								VSS	VCC	P84	P85	9
8	PD2	P96	P94	P95								P51	P52	VCC_ USB	USB1_ DP	8
7	PD0	PD1	P92	P93								P54	P10	P56	USB1_ DM	7
6	P90	P91	VCC	VSS								P55	P57	VCC_ USB	VSS_ USB	6
5	P46	P47	P40	P43								P11	P15	P13	USB0_ DP	5
4	P45	P44	P07	P41	VSS	VSS	MDE	RES#	P34	PF4	P30	VSS	P17	P14	USB0_ DM	4
3	P42	VREFL	P05	VCC	BSCANP	VCL	MD0	VCC	PF3	PF0	VCC	P22	P20	P16	P12	3
2	AVCC	VREFH	P03	P01	CNVSS	WDTOVF#	MD1	P35	P32	P31	P27	P25	P23	PLLVCC	PLLVSS	2
1	AVSS	P02	P00	EMLE	XCIN	XCOUT	VSS	XTAL	EXTAL	P33	PF2	PF1	P26	P24	P21	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

RX62N Group
RX621 Group
PLBG0176GA-A
(176-pin LFBGA)
(Upper perspective view)

: NC pin

Figure 1.3 Pin Assignment of the 176-Pin LFBGA

Table 1.4 List of Pins and Pin Functions (176-Pin LFBGA) (5 / 6)

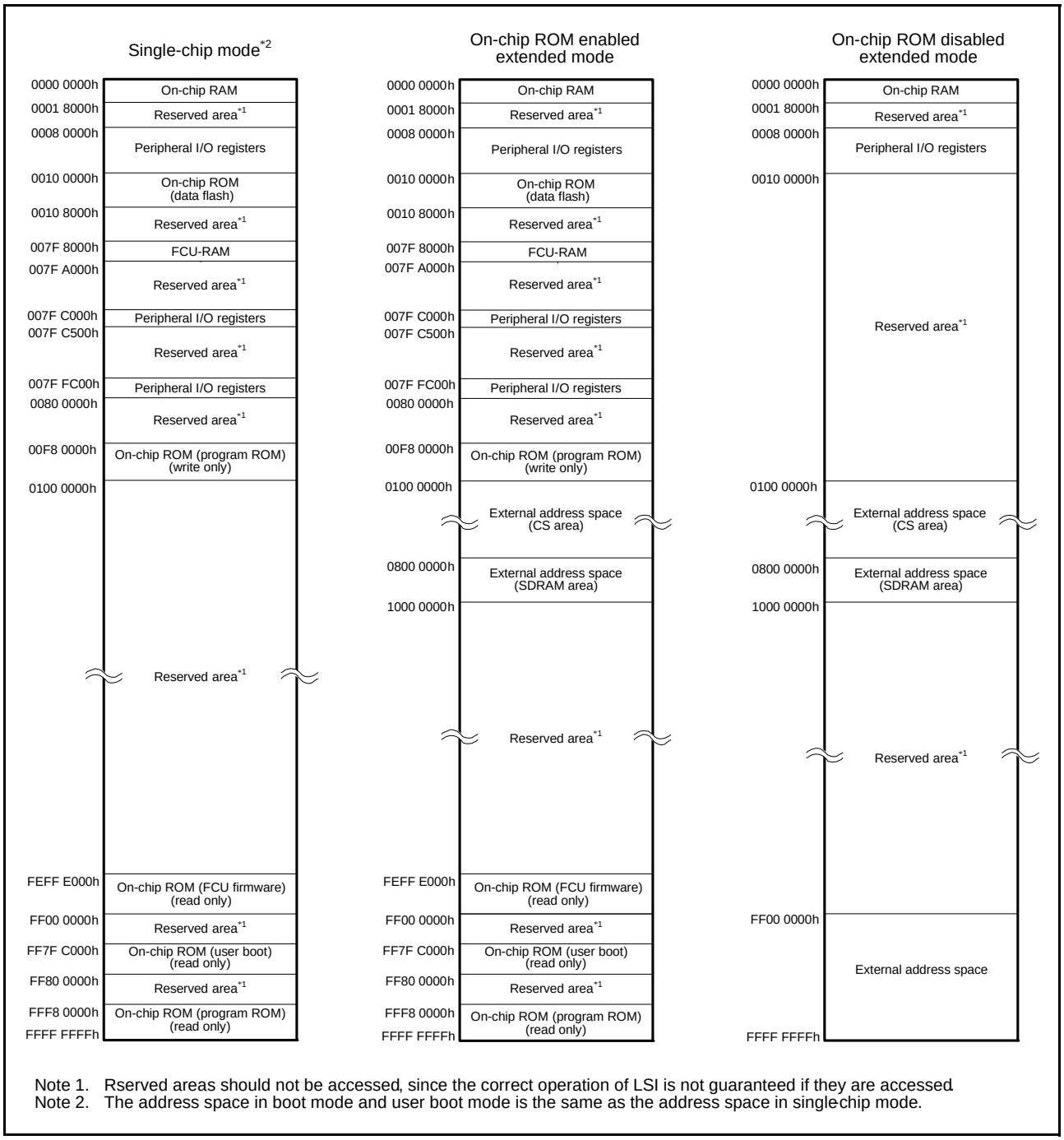
Pin No. 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	External Bus EXDMAC	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE, WDT)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
N2		P23	EDACK0-B		USB0_DPUPE-A	MTIOC3D-A/ MTCLKD-A/ PO3	TxD3-B	
N3		P20			USB0_ID	MTIOC1A/ TMRI0-B/ PO0	SDA1/ TxD0	
N4		P17			USB1_VBUS/ USB1_OVRCURB/ USB1_VBUSEN-B	MTIOC3A/ PO15	TxD3-A	IRQ7-B
N5		P15			USB1_OVRCURA/ USB1_DPUPE-B	MTIOC0B/ TMCI2-A/ PO13	SCK3-A	IRQ5-B
N6		P57	WAIT#-A/ WR3#/ BC3#/ EDREQ1-C					
N7		P10			USB1_DPUPE-A	MTIC5W-A/ TMRI3-A		IRQ0-B
N8		P52	RD#				SSLB3-A/ RxD2-B	
N9	VCC							
N10		PC5	A21-A/ CS2#-C/ WAIT#-C	ET_ETXD2		MTIC11W-A/ MTCLKD-B	RSPCKA-A	
N11		PC3	A19-A	ET_TX_ER		MTCLKF-A	TxD5	
N12		PC2	A18-A	ET_RX_DV		MTCLKE-A	SSLA3-A/ RxD5	
N13		P74	CS4#-B	ET_ERXD1/ RMII_RXD1				
N14		P73	CS3#-B	ET_WOL				
N15		PB5	A13			MTIOC10C/ MTCLKF-B/ PO29		
P1		P24	CS4#-C/ EDREQ1-B		USB0_VBUSEN-A	MTIOC4A-A/ MTCLKA-A/ TMRI1/ PO4	SCK3-B	
P2	PLLVCC							
P3		P16			USB0_VBUS/ USB0_OVRCURB/ USB0_VBUSEN-B	MTIOC3C-A/ TMO2/ PO14	RxD3-A	IRQ6-B
P4		P14			USB0_OVRCURA/ USB0_DPUPE-B	TMRI2		IRQ4-B
P5		P13				TMO3	SDA0/ TxD2-A	IRQ3-B/ ADTRG1#
P6	VCC_USB							

3. Address Space

3.1 Address Space

This LSI has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.

Figure 3.1 shows the memory maps in the respective operating modes. Accessible areas will differ according to the operating mode and states of control bits.



Note 1. Rserved areas should not be accessed, since the correct operation of LSI is not guaranteed if they are accessed.
Note 2. The address space in boot mode and user boot mode is the same as the address space in single-chip mode.

Figure 3.1 Memory Map in Each Operating Mode

Table 4.1 List of I/O Registers (Address Order) (10 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 718Dh	ICU	DTC activation enable register 141	DTCER141	8	8	2 ICLK
0008 718Eh	ICU	DTC activation enable register 142	DTCER142	8	8	2 ICLK
0008 718Fh	ICU	DTC activation enable register 143	DTCER143	8	8	2 ICLK
0008 7190h	ICU	DTC activation enable register 144	DTCER144	8	8	2 ICLK
0008 7191h	ICU	DTC activation enable register 145	DTCER145	8	8	2 ICLK
0008 7195h	ICU	DTC activation enable register 149	DTCER149	8	8	2 ICLK
0008 7196h	ICU	DTC activation enable register 150	DTCER150	8	8	2 ICLK
0008 7199h	ICU	DTC activation enable register 153	DTCER153	8	8	2 ICLK
0008 719Ah	ICU	DTC activation enable register 154	DTCER154	8	8	2 ICLK
0008 719Dh	ICU	DTC activation enable register 157	DTCER157	8	8	2 ICLK
0008 719Eh	ICU	DTC activation enable register 158	DTCER158	8	8	2 ICLK
0008 719Fh	ICU	DTC activation enable register 159	DTCER159	8	8	2 ICLK
0008 71A0h	ICU	DTC activation enable register 160	DTCER160	8	8	2 ICLK
0008 71A2h	ICU	DTC activation enable register 162	DTCER162	8	8	2 ICLK
0008 71A3h	ICU	DTC activation enable register 163	DTCER163	8	8	2 ICLK
0008 71A4h	ICU	DTC activation enable register 164	DTCER164	8	8	2 ICLK
0008 71A5h	ICU	DTC activation enable register 165	DTCER165	8	8	2 ICLK
0008 71A6h	ICU	DTC activation enable register 166	DTCER166	8	8	2 ICLK
0008 71A7h	ICU	DTC activation enable register 167	DTCER167	8	8	2 ICLK
0008 71A8h	ICU	DTC activation enable register 168	DTCER168	8	8	2 ICLK
0008 71A9h	ICU	DTC activation enable register 169	DTCER169	8	8	2 ICLK
0008 71AEh	ICU	DTC activation enable register 174	DTCER174	8	8	2 ICLK
0008 71AFh	ICU	DTC activation enable register 175	DTCER175	8	8	2 ICLK
0008 71B1h	ICU	DTC activation enable register 177	DTCER177	8	8	2 ICLK
0008 71B2h	ICU	DTC activation enable register 178	DTCER178	8	8	2 ICLK
0008 71B4h	ICU	DTC activation enable register 180	DTCER180	8	8	2 ICLK
0008 71B5h	ICU	DTC activation enable register 181	DTCER181	8	8	2 ICLK
0008 71B7h	ICU	DTC activation enable register 183	DTCER183	8	8	2 ICLK
0008 71B8h	ICU	DTC activation enable register 184	DTCER184	8	8	2 ICLK
0008 71C6h	ICU	DTC activation enable register 198	DTCER198	8	8	2 ICLK
0008 71C7h	ICU	DTC activation enable register 199	DTCER199	8	8	2 ICLK
0008 71C8h	ICU	DTC activation enable register 200	DTCER200	8	8	2 ICLK
0008 71C9h	ICU	DTC activation enable register 201	DTCER201	8	8	2 ICLK
0008 71CAh	ICU	DTC activation enable register 202	DTCER202	8	8	2 ICLK
0008 71CBh	ICU	DTC activation enable register 203	DTCER203	8	8	2 ICLK
0008 71D7h	ICU	DTC activation enable register 215	DTCER215	8	8	2 ICLK
0008 71D8h	ICU	DTC activation enable register 216	DTCER216	8	8	2 ICLK
0008 71DBh	ICU	DTC activation enable register 219	DTCER219	8	8	2 ICLK
0008 71DCh	ICU	DTC activation enable register 220	DTCER220	8	8	2 ICLK
0008 71DFh	ICU	DTC activation enable register 223	DTCER223	8	8	2 ICLK
0008 71E0h	ICU	DTC activation enable register 224	DTCER224	8	8	2 ICLK
0008 71E3h	ICU	DTC activation enable register 227	DTCER227	8	8	2 ICLK
0008 71E4h	ICU	DTC activation enable register 228	DTCER228	8	8	2 ICLK
0008 71EBh	ICU	DTC activation enable register 235	DTCER235	8	8	2 ICLK
0008 71ECh	ICU	DTC activation enable register 236	DTCER236	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (17 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 824Fh	SCI1	Serial extended mode register	SEMR	8	8	2 to 3 PCLK*8
0008 8248h	SMCI1	Serial mode register	SMR	8	8	2 to 3 PCLK*8
0008 8249h	SMCI1	Bit rate register	BRR	8	8	2 to 3 PCLK*8
0008 824Ah	SMCI1	Serial control register	SCR	8	8	2 to 3 PCLK*8
0008 824Bh	SMCI1	Transmit data register	TDR	8	8	2 to 3 PCLK*8
0008 824Ch	SMCI1	Serial status register	SSR	8	8	2 to 3 PCLK*8
0008 824Dh	SMCI1	Receive data register	RDR	8	8	2 to 3 PCLK*8
0008 824Eh	SMCI1	Smart card mode register	SCMR	8	8	2 to 3 PCLK*8
0008 8250h	SCI2	Serial mode register	SMR	8	8	2 to 3 PCLK*8
0008 8251h	SCI2	Bit rate register	BRR	8	8	2 to 3 PCLK*8
0008 8252h	SCI2	Serial control register	SCR	8	8	2 to 3 PCLK*8
0008 8253h	SCI2	Transmit data register	TDR	8	8	2 to 3 PCLK*8
0008 8254h	SCI2	Serial status register	SSR	8	8	2 to 3 PCLK*8
0008 8255h	SCI2	Receive data register	RDR	8	8	2 to 3 PCLK*8
0008 8256h	SCI2	Smart card mode register	SCMR	8	8	2 to 3 PCLK*8
0008 8257h	SCI2	Serial extended mode register	SEMR	8	8	2 to 3 PCLK*8
0008 8250h	SMCI2	Serial mode register	SMR	8	8	2 to 3 PCLK*8
0008 8251h	SMCI2	Bit rate register	BRR	8	8	2 to 3 PCLK*8
0008 8252h	SMCI2	Serial control register	SCR	8	8	2 to 3 PCLK*8
0008 8253h	SMCI2	Transmit data register	TDR	8	8	2 to 3 PCLK*8
0008 8254h	SMCI2	Serial status register	SSR	8	8	2 to 3 PCLK*8
0008 8255h	SMCI2	Receive data register	RDR	8	8	2 to 3 PCLK*8
0008 8256h	SMCI2	Smart card mode register	SCMR	8	8	2 to 3 PCLK*8
0008 8258h	SCI3	Serial mode register	SMR	8	8	2 to 3 PCLK*8
0008 8259h	SCI3	Bit rate register	BRR	8	8	2 to 3 PCLK*8
0008 825Ah	SCI3	Serial control register	SCR	8	8	2 to 3 PCLK*8
0008 825Bh	SCI3	Transmit data register	TDR	8	8	2 to 3 PCLK*8
0008 825Ch	SCI3	Serial status register	SSR	8	8	2 to 3 PCLK*8
0008 825Dh	SCI3	Receive data register	RDR	8	8	2 to 3 PCLK*8
0008 825Eh	SCI3	Smart card mode register	SCMR	8	8	2 to 3 PCLK*8
0008 825Fh	SCI3	Serial extended mode register	SEMR	8	8	2 to 3 PCLK*8
0008 8258h	SMCI3	Serial mode register	SMR	8	8	2 to 3 PCLK*8
0008 8259h	SMCI3	Bit rate register	BRR	8	8	2 to 3 PCLK*8
0008 825Ah	SMCI3	Serial control register	SCR	8	8	2 to 3 PCLK*8
0008 825Bh	SMCI3	Transmit data register	TDR	8	8	2 to 3 PCLK*8
0008 825Ch	SMCI3	Serial status register	SSR	8	8	2 to 3 PCLK*8
0008 825Dh	SMCI3	SMCI3 Receive data register	RDR	8	8	2 to 3 PCLK*8
0008 825Eh	SMCI3	SMCI3 Smart card mode register	SCMR	8	8	2 to 3 PCLK*8
0008 8268h	SCI5	Serial mode register	SMR	8	8	2 to 3 PCLK*8
0008 8269h	SCI5	Bit rate register	BRR	8	8	2 to 3 PCLK*8
0008 826Ah	SCI5	Serial control register	SCR	8	8	2 to 3 PCLK*8
0008 826Bh	SCI5	Transmit data register	TDR	8	8	2 to 3 PCLK*8
0008 826Ch	SCI5	Serial status register	SSR	8	8	2 to 3 PCLK*8
0008 826Dh	SCI5	Receive data register	RDR	8	8	2 to 3 PCLK*8
0008 826Eh	SCI5	Smart card mode register	SCMR	8	8	2 to 3 PCLK*8

Table 4.1 List of I/O Registers (Address Order) (21 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 861Eh	MTU4	Timer general register B	TGRB	16	16	2 to 3 PCLK*8
0008 8620h	MTUA	Timer subcounter	TCNTS	16	16	2 to 3 PCLK*8
0008 8622h	MTUA	Timer cycle buffer register	TCBR	16	16	2 to 3 PCLK*8
0008 8624h	MTU3	Timer general register C	TGRC	16	16	2 to 3 PCLK*8
0008 8626h	MTU3	Timer general register D	TGRD	16	16	2 to 3 PCLK*8
0008 8628h	MTU4	Timer general register C	TGRC	16	16	2 to 3 PCLK*8
0008 862Ah	MTU4	Timer general register D	TGRD	16	16	2 to 3 PCLK*8
0008 862Ch	MTU3	Timer status register	TSR	8	8	2 to 3 PCLK*8
0008 862Dh	MTU4	Timer status register	TSR	8	8	2 to 3 PCLK*8
0008 8630h	MTUA	Timer interrupt skipping set register	TITCR	8	8	2 to 3 PCLK*8
0008 8631h	MTUA	Timer interrupt skipping counter	TITCNT	8	8	2 to 3 PCLK*8
0008 8632h	MTUA	Timer buffer transfer set register	TBTER	8	8	2 to 3 PCLK*8
0008 8634h	MTUA	Timer dead time enable register	TDER	8	8	2 to 3 PCLK*8
0008 8636h	MTUA	Timer output level buffer register	TOLBR	8	8	2 to 3 PCLK*8
0008 8638h	MTU3	Timer buffer operation transfer mode register	TBTM	8	8	2 to 3 PCLK*8
0008 8639h	MTU4	Timer buffer operation transfer mode register	TBTM	8	8	2 to 3 PCLK*8
0008 8640h	MTU4	Timer A/D converter start request control register	TADCR	16	16	2 to 3 PCLK*8
0008 8644h	MTU4	Timer A/D converter start request cycle set register A	TADCORA	16	16	2 to 3 PCLK*8
0008 8646h	MTU4	Timer A/D converter start request cycle set register B	TADCORB	16	16	2 to 3 PCLK*8
0008 8648h	MTU4	Timer A/D converter start request cycle set buffer register A	TADCOBRA	16	16	2 to 3 PCLK*8
0008 864Ah	MTU4	Timer A/D converter start request cycle set buffer register B	TADCOBRB	16	16	2 to 3 PCLK*8
0008 8660h	MTUA	Timer waveform control register	TWCR	8	8	2 to 3 PCLK*8
0008 8680h	MTUA	Timer start register	TSTR	8	8	2 to 3 PCLK*8
0008 8681h	MTUA	Timer synchronous register	TSYR	8	8	2 to 3 PCLK*8
0008 8684h	MTUA	Timer read/write enable register	TRWER	8	8	2 to 3 PCLK*8
0008 8700h	MTU0	Timer control register	TCR	8	8	2 to 3 PCLK*8
0008 8701h	MTU0	Timer mode register	TMDR	8	8	2 to 3 PCLK*8
0008 8702h	MTU0	Timer I/O control register H	TIORH	8	8	2 to 3 PCLK*8
0008 8703h	MTU0	Timer I/O control register L	TIORL	8	8	2 to 3 PCLK*8
0008 8704h	MTU0	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK*8
0008 8705h	MTU0	Timer status register	TSR	8	8	2 to 3 PCLK*8
0008 8706h	MTU0	Timer counter	TCNT	16	16	2 to 3 PCLK*8
0008 8708h	MTU0	Timer general register A	TGRA	16	16	2 to 3 PCLK*8
0008 870Ah	MTU0	Timer general register B	TGRB	16	16	2 to 3 PCLK*8
0008 870Ch	MTU0	Timer general register C	TGRC	16	16	2 to 3 PCLK*8
0008 870Eh	MTU0	Timer general register D	TGRD	16	16	2 to 3 PCLK*8
0008 8720h	MTU0	Timer general register E	TGRE	16	16	2 to 3 PCLK*8
0008 8722h	MTU0	Timer general register F	TGRF	16	16	2 to 3 PCLK*8
0008 8724h	MTU0	Timer interrupt enable register 2	TIER2	8	8	2 to 3 PCLK*8

Table 4.1 List of I/O Registers (Address Order) (26 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 C023h	PORT3	Data register	DR	8	8	2 to 3 PCLK*8
0008 C024h	PORT4	Data register	DR	8	8	2 to 3 PCLK*8
0008 C025h	PORT5	Data register	DR	8	8	2 to 3 PCLK*8
0008 C026h	PORT6	Data register	DR*6*7	8	8	2 to 3 PCLK*8
0008 C027h	PORT7	Data register	DR*6*7	8	8	2 to 3 PCLK*8
0008 C028h	PORT8	Data register	DR*6*7	8	8	2 to 3 PCLK*8
0008 C029h	PORT9	Data register	DR*6*7	8	8	2 to 3 PCLK*8
0008 C02Ah	PORTA	Data register	DR	8	8	2 to 3 PCLK*8
0008 C02Bh	PORTB	Data register	DR	8	8	2 to 3 PCLK*8
0008 C02Ch	PORTC	Data register	DR	8	8	2 to 3 PCLK*8
0008 C02Dh	PORTD	Data register	DR	8	8	2 to 3 PCLK*8
0008 C02Eh	PORTE	Data register	DR*7	8	8	2 to 3 PCLK*8
0008 C02Fh	PORTF	Data register	DR*5*6*7	8	8	2 to 3 PCLK*8
0008 C030h	PORTG	Data register	DR**5*6*7	8	8	2 to 3 PCLK*8
0008 C040h	PORT0	Port register	PORT	8	8	2 to 3 PCLK*8
0008 C041h	PORT1	Port register	PORT	8	8	2 to 3 PCLK*8
0008 C042h	PORT2	Port register	PORT	8	8	2 to 3 PCLK*8
0008 C043h	PORT3	Port register	PORT	8	8	2 to 3 PCLK*8
0008 C044h	PORT4	Port register	PORT	8	8	2 to 3 PCLK*8
0008 C045h	PORT5	Port register	PORT	8	8	2 to 3 PCLK*8
0008 C046h	PORT6	Port register	PORT*6*7	8	8	2 to 3 PCLK*8
0008 C047h	PORT7	Port register	PORT*6*7	8	8	2 to 3 PCLK*8
0008 C048h	PORT8	Port register	PORT*6*7	8	8	2 to 3 PCLK*8
0008 C049h	PORT9	Port register	PORT*6*7	8	8	2 to 3 PCLK*8
0008 C04Ah	PORTA	Port register	PORT	8	8	2 to 3 PCLK*8
0008 C04Bh	PORTB	Port register	PORT	8	8	2 to 3 PCLK*8
0008 C04Ch	PORTC	Port register	PORT	8	8	2 to 3 PCLK*8
0008 C04Dh	PORTD	Port register	PORT	8	8	2 to 3 PCLK*8
0008 C04Eh	PORTE	Port register	PORT*7	8	8	2 to 3 PCLK*8
0008 C04Fh	PORTF	Port register	PORT*5*6*7	8	8	2 to 3 PCLK*8
0008 C050h	PORTG	Port register	PORT*5*6*7	8	8	2 to 3 PCLK*8
0008 C060h	PORT0	Input buffer control register	ICR	8	8	2 to 3 PCLK*8
0008 C061h	PORT1	Input buffer control register	ICR	8	8	2 to 3 PCLK*8
0008 C062h	PORT2	Input buffer control register	ICR	8	8	2 to 3 PCLK*8
0008 C063h	PORT3	Input buffer control register	ICR	8	8	2 to 3 PCLK*8
0008 C064h	PORT4	Input buffer control register	ICR	8	8	2 to 3 PCLK*8
0008 C065h	PORT5	Input buffer control register	ICR	8	8	2 to 3 PCLK*8
0008 C066h	PORT6	Input buffer control register	ICR*6*7	8	8	2 to 3 PCLK*8
0008 C067h	PORT7	Input buffer control register	ICR*6*7	8	8	2 to 3 PCLK*8
0008 C068h	PORT8	Input buffer control register	ICR*6*7	8	8	2 to 3 PCLK*8
0008 C069h	PORT9	Input buffer control register	ICR*6*7	8	8	2 to 3 PCLK*8
0008 C06Ah	PORTA	Input buffer control register	ICR	8	8	2 to 3 PCLK*8
0008 C06Bh	PORTB	Input buffer control register	ICR	8	8	2 to 3 PCLK*8
0008 C06Ch	PORTC	Input buffer control register	ICR	8	8	2 to 3 PCLK*8
0008 C06Dh	PORTD	Input buffer control register	ICR	8	8	2 to 3 PCLK*8

Table 4.1 List of I/O Registers (Address Order) (29 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 C412h	RTC	Minute alarm register	RMINAR	8	8	2 to 3 PCLK*8
0008 C414h	RTC	Hour alarm register	RHRAR	8	8	2 to 3 PCLK*8
0008 C416h	RTC	Day-of-week alarm register	RWKAR	8	8	2 to 3 PCLK*8
0008 C418h	RTC	Date alarm register	RDAYAR	8	8	2 to 3 PCLK*8
0008 C41Ah	RTC	Month alarm register	RMONAR	8	8	2 to 3 PCLK*8
0008 C41Ch	RTC	Year alarm register	RYRAR	16	16	2 to 3 PCLK*8
0008 C41Eh	RTC	Year alarm enable register	RYRAREN	8	8	2 to 3 PCLK*8
0008 C422h	RTC	RTC control register 1	RCR1	8	8	2 to 3 PCLK*8
0008 C424h	RTC	RTC control register 2	RCR2	8	8	2 to 3 PCLK*8
0009 0200h to 0009 03FFh	CAN0	Mailbox registers 0 to 31	MB0 to MB31	128	8, 16, 32	2 to 3 PCLK*8
0009 0400h	CAN0	Mask register 0	MKR0	32	8, 16, 32	2 to 3 PCLK*8
0009 0404h	CAN0	Mask register 1	MKR1	32	8, 16, 32	2 to 3 PCLK*8
0009 0408h	CAN0	Mask register 2	MKR2	32	8, 16, 32	2 to 3 PCLK*8
0009 040Ch	CAN0	Mask register 3	MKR3	32	8, 16, 32	2 to 3 PCLK*8
0009 0410h	CAN0	Mask register 4	MKR4	32	8, 16, 32	2 to 3 PCLK*8
0009 0414h	CAN0	Mask register 5	MKR5	32	8, 16, 32	2 to 3 PCLK*8
0009 0418h	CAN0	Mask register 6	MKR6	32	8, 16, 32	2 to 3 PCLK*8
0009 041Ch	CAN0	Mask register 7	MKR7	32	8, 16, 32	2 to 3 PCLK*8
0009 0420h	CAN0	FIFO received ID compare register 0	FIDCR0	32	8, 16, 32	2 to 3 PCLK*8
0009 0424h	CAN0	FIFO received ID compare register 1	FIDCR1	32	8, 16, 32	2 to 3 PCLK*8
0009 0428h	CAN0	Mask invalid register	MKIVLR	32	8, 16, 32	2 to 3 PCLK*8
0009 042Ch	CAN0	Mailbox interrupt enable register	MIER	32	8, 16, 32	2 to 3 PCLK*8
0009 0820h to 0009 083Fh	CAN0	Message control registers 0 to 31	MCTL0 to MCTL31	8	8	2 to 3 PCLK*8
0009 0840h	CAN0	Control register	CTLR	16	8, 16	2 to 3 PCLK*8
0009 0842h	CAN0	Status register	STR	16	8, 16	2 to 3 PCLK*8
0009 0844h	CAN0	Bit configuration register	BCR	32	8, 16, 32	2 to 3 PCLK*8
0009 0848h	CAN0	Receive FIFO control register	RFCR	8	8	2 to 3 PCLK*8
0009 0849h	CAN0	Receive FIFO pointer control register	RFPCR	8	8	2 to 3 PCLK*8
0009 084Ah	CAN0	Transmit FIFO control register	TFCR	8	8	2 to 3 PCLK*8
0009 084Bh	CAN0	Transmit FIFO pointer control register	TFPCR	8	8	2 to 3 PCLK*8
0009 084Ch	CAN0	Error interrupt enable register	EIER	8	8	2 to 3 PCLK*8
0009 084Dh	CAN0	Error interrupt factor judge register	EIFR	8	8	2 to 3 PCLK*8
0009 084Eh	CAN0	Receive error count register	RECR	8	8	2 to 3 PCLK*8
0009 084Fh	CAN0	Transmit error count register	TECR	8	8	2 to 3 PCLK*8
0009 0850h	CAN0	Error code store register	ECSR	8	8	2 to 3 PCLK*8
0009 0851h	CAN0	Channel search support register	CSSR	8	8	2 to 3 PCLK*8
0009 0852h	CAN0	Mailbox search status register	MSSR	8	8	2 to 3 PCLK*8
0009 0853h	CAN0	Mailbox search mode register	MSMR	8	8	2 to 3 PCLK*8
0009 0854h	CAN0	Time stamp register	TSR	16	8, 16	2 to 3 PCLK*8
0009 0856h	CAN0	Acceptance filter support register	AFSR	16	8, 16	2 to 3 PCLK*8
0009 0858h	CAN0	Test control register	TCR	8	8	2 to 3 PCLK*8
000A 0000h	USB0	System configuration control register	SYSCFG	16	16	3 to 4 PCLK*8
000A 0004h	USB0	System configuration status register 0	SYSSTS0	16	16	at least 9 PCLK*9

Table 4.1 List of I/O Registers (Address Order) (32 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000A 00D4h	USB0	Device address 2 configuration register	DEVADD2	16	16	at least 9 PCLK*9
000A 00D6h	USB0	Device address 3 configuration register	DEVADD3	16	16	at least 9 PCLK*9
000A 00D8h	USB0	Device address 4 configuration register	DEVADD4	16	16	at least 9 PCLK*9
000A 00DAh	USB0	Device address 5 configuration register	DEVADD5	16	16	at least 9 PCLK*9
000A 0200h	USB1	System configuration control register	SYSCFG	16	16	3 to 4 PCLK*8
000A 0204h	USB1	System configuration status register 0	SYSSTS0	16	16	at least 9 PCLK*9
000A 0208h	USB1	Device state control register 0	DVSTCTR0	16	16	at least 9 PCLK*9
000A 0214h	USB1	CFIFO port register	CFIFO	16	8, 16	3 to 4 PCLK*8
000A 0218h	USB1	D0FIFO port register	D0FIFO	16	8, 16	3 to 4 PCLK*8
000A 021Ch	USB1	D1FIFO port register	D1FIFO	16	8, 16	3 to 4 PCLK*8
000A 0220h	USB1	CFIFO port select register	CFIFOSEL	16	16	3 to 4 PCLK*8
000A 0222h	USB1	CFIFO port control register	CFIFOCTR	16	16	3 to 4 PCLK*8
000A 0228h	USB1	D0FIFO port select register	D0FIFOSEL	16	16	3 to 4 PCLK*8
000A 022Ah	USB1	D0FIFO port control register	D0FIFOCTR	16	16	3 to 4 PCLK*8
000A 022Ch	USB1	D1FIFO port select register	D1FIFOSEL	16	16	3 to 4 PCLK*8
000A 022Eh	USB1	D1FIFO port control register	D1FIFOCTR	16	16	3 to 4 PCLK*8
000A 0230h	USB1	Interrupt enable register 0	INTENB0	16	16	at least 9 PCLK*9
000A 0232h	USB1	Interrupt enable register 1	INTENB1	16	16	at least 9 PCLK*9
000A 0236h	USB1	BRDY interrupt enable register	BRDYENB	16	16	at least 9 PCLK*9
000A 0238h	USB1	NRDY interrupt enable register	NRDYENB	16	16	at least 9 PCLK*9
000A 023Ah	USB1	BEMP interrupt enable register	BEMPENB	16	16	at least 9 PCLK*9
000A 023Ch	USB1	SOF output configuration register	SOFCFG	16	16	at least 9 PCLK*9
000A 0240h	USB1	Interrupt status register 0	INTSTS0	16	16	at least 9 PCLK*9
000A 0242h	USB1	Interrupt status register 1	INTSTS1	16	16	at least 9 PCLK*9
000A 0246h	USB1	BRDY interrupt status register	BRDYSTS	16	16	at least 9 PCLK*9
000A 0248h	USB1	NRDY interrupt status register	NRDYSTS	16	16	at least 9 PCLK*9
000A 024Ah	USB1	BEMP interrupt status register	BEMPSTS	16	16	at least 9 PCLK*9
000A 024Ch	USB1	Frame number register	FRMNUM	16	16	at least 9 PCLK*9
000A 024Eh	USB1	Device state change register	DVCHGR	16	16	at least 9 PCLK*9
000A 0250h	USB1	USB address register	USBADDR	16	16	at least 9 PCLK*9

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

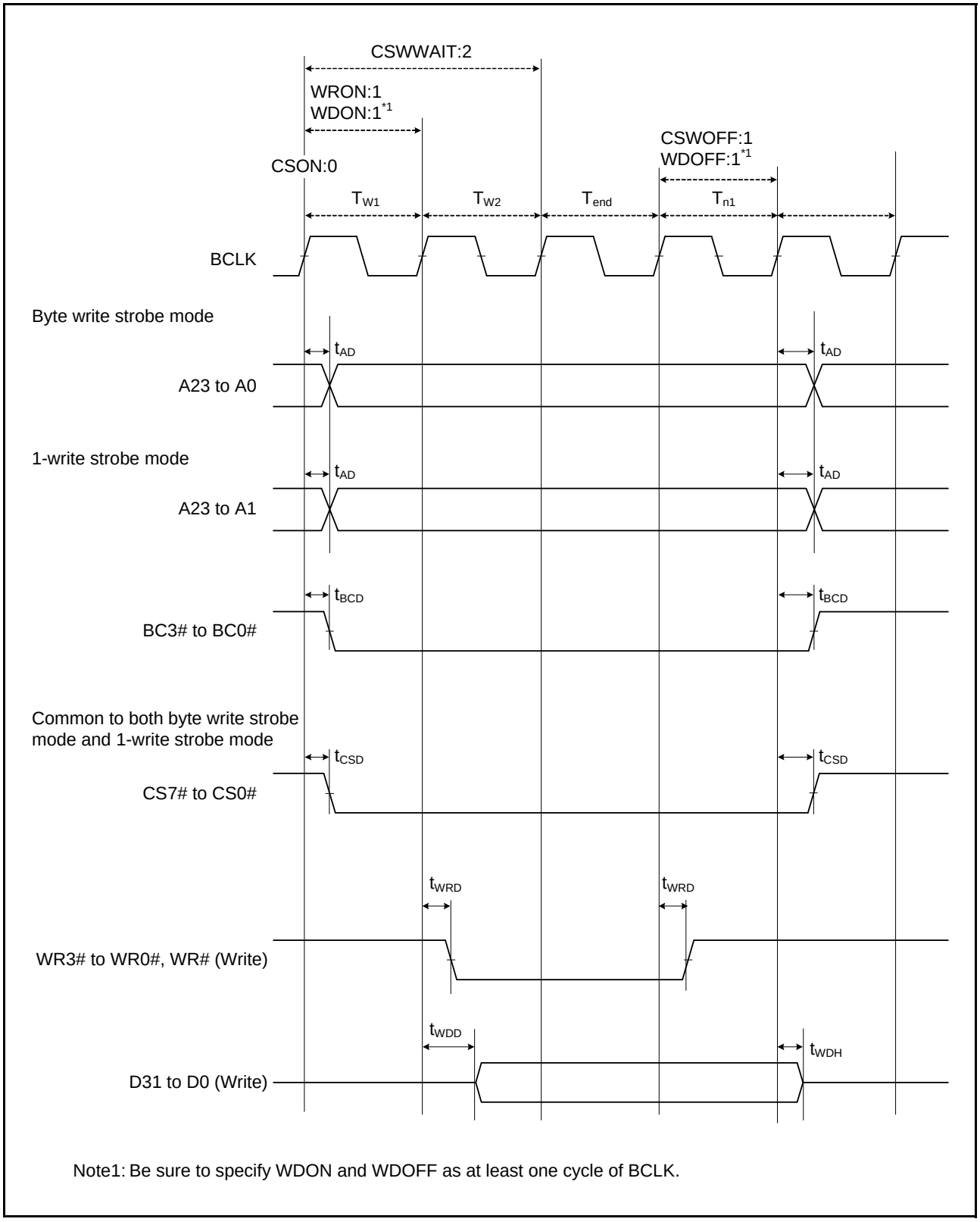
Table 5.1 Absolute Maximum Ratings

Item	Symbol	Value	Unit
Power supply voltage	VCC PLLVCC VCC_USB	-0.3 to +4.6	V
Input voltage (except for ports 00 to 02, 07, ports 12, 13, 16, 17, ports 20, 21, port 33)	V_{IN}	-0.3 to VCC+0.3	V
Input voltage (ports 00 to 02, 07, ports 12, 13, 16, 17, ports 20, 21, port 33*1)	V_{IN}	-0.3 to +5.8	V
Reference power supply voltage	V_{REF}	-0.3 to VCC+0.3	V
Analog power supply voltage	AVCC*2	-0.3 to +4.6	V
Analog input voltage	V_{AN}	-0.3 to VCC+0.3	V
Operating temperature	T_{opr}	-40 to +85	°C
Storage temperature	T_{stg}	-55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. Ports 00 to 02, 07, ports 12, 13, 16, 17, ports 20, 21, and port 33 are 5 V tolerant.

Note 2. Connect AVCC to VCC. When neither the A/D converter nor the D/A converter is in use, do not leave the AVCC, VREFH, AVSS, and VREFL pins open. Connect the AVCC and VREFH pins to VCC, and the AVSS and VREFL pins to VSS, respectively.



Note1: Be sure to specify WDON and WDOFF as at least one cycle of BCLK.

Figure 5.11 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized)

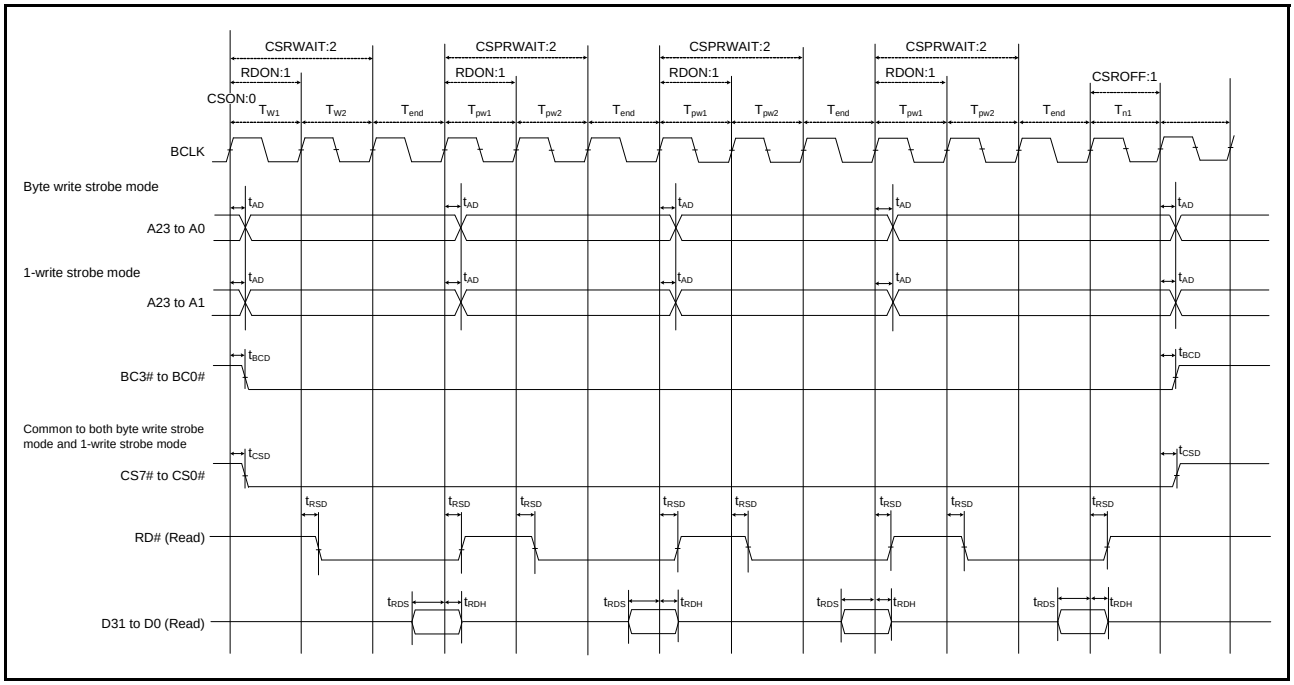


Figure 5.12 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)

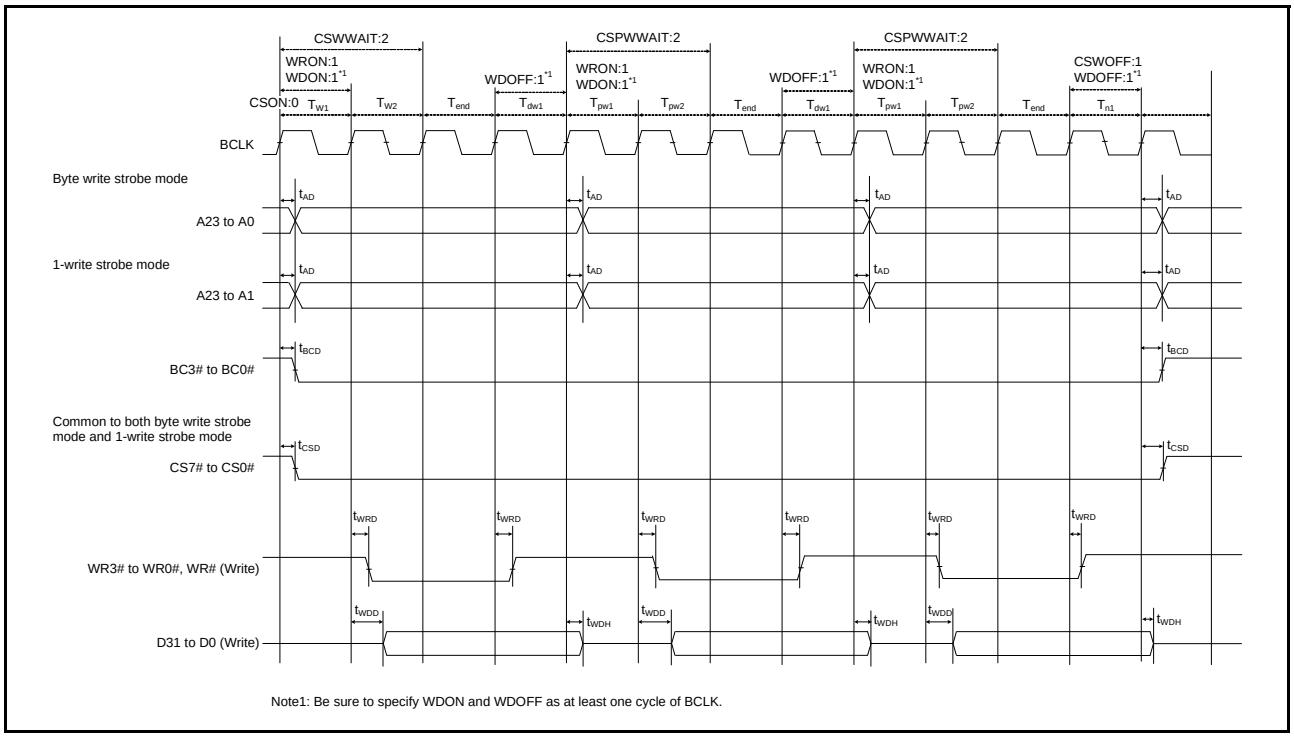


Figure 5.13 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)

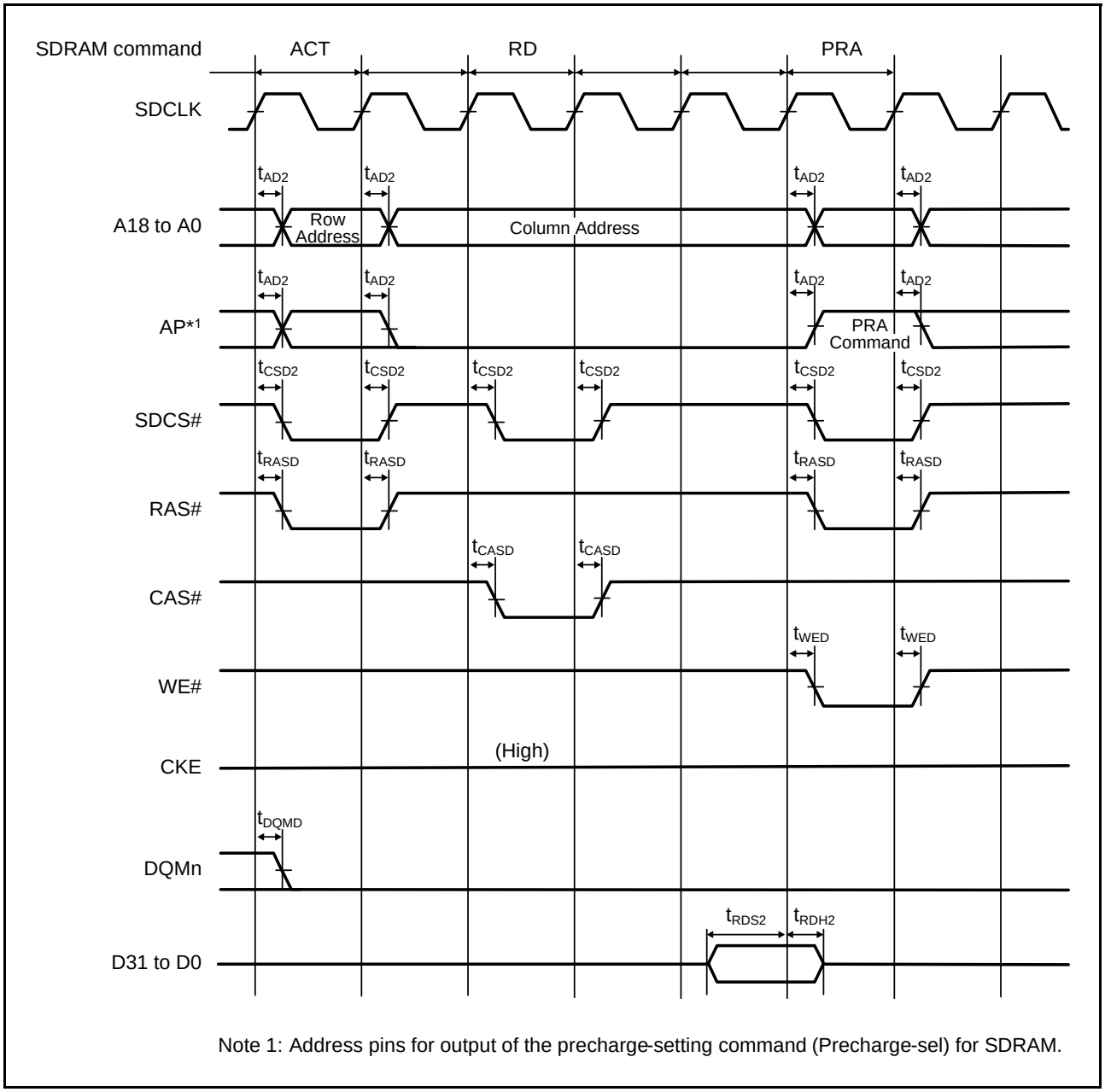


Figure 5.15 SDRAM Space Single Read Bus Timing

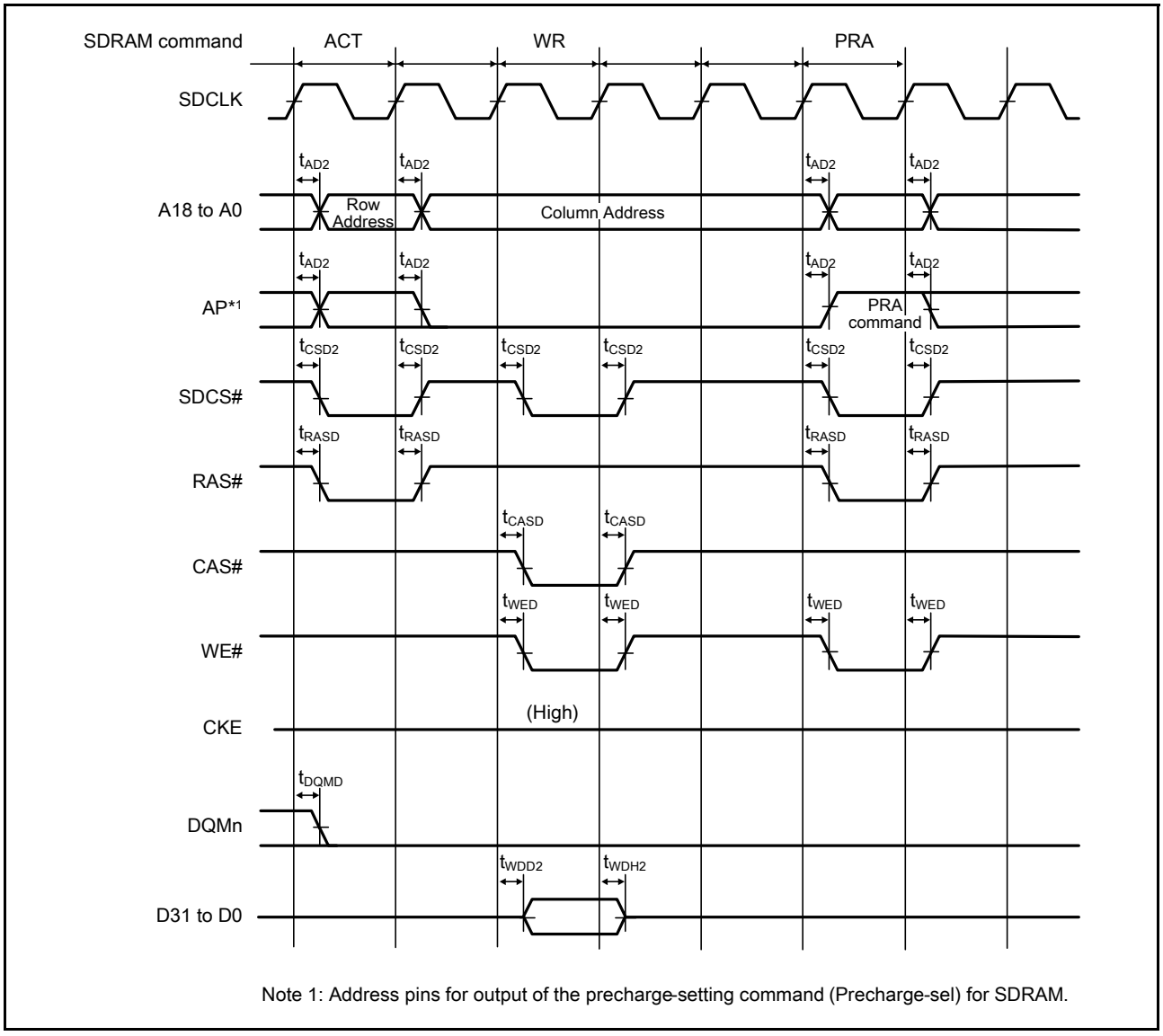
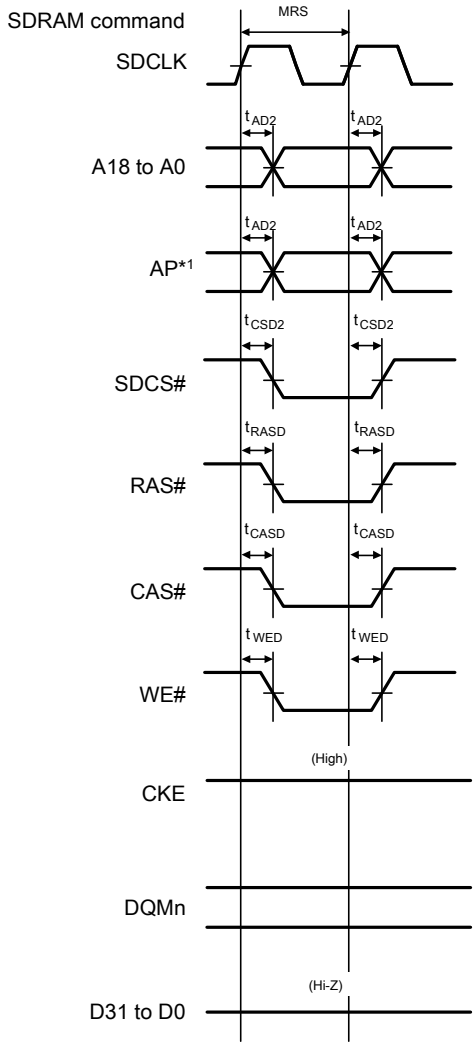


Figure 5.16 SDRAM Space Single Write Bus Timing



Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.20 SDRAM Space Mode Register Set Bus Timing

Table 5.16 Timing of On-Chip Peripheral Modules (7)

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
PCLK = 8 to 50 MHz
T_a = -40 to +85°C

Item		Symbol	Min.*1*2	Max.	Unit	Test Conditions
RIIC (Fast-mode+) ICFER.FMPE = 1	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 240	—	ns	Figure 5.43
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 120	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 120	—	ns	
	SCL, SDA input rising time	t_{Sr}	—	120	ns	
	SCL, SDA input falling time	t_{Sf}	—	120	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 120	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 120		ns	
	Re-start condition input setup time	t_{STAS}	120	—	ns	
	Stop condition input setup time	t_{STOS}	120	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 20	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	550	pF	

Note: t_{IICcyc}: RIIC internal reference clock (IICφ) cycles
Note 1. The value in parentheses is used when ICMR3.NF[1:0] are set to 11b while a digital filter is enabled with ICFER.NFE = 1.
Note 2. C_b indicates the total capacity of the bus line.

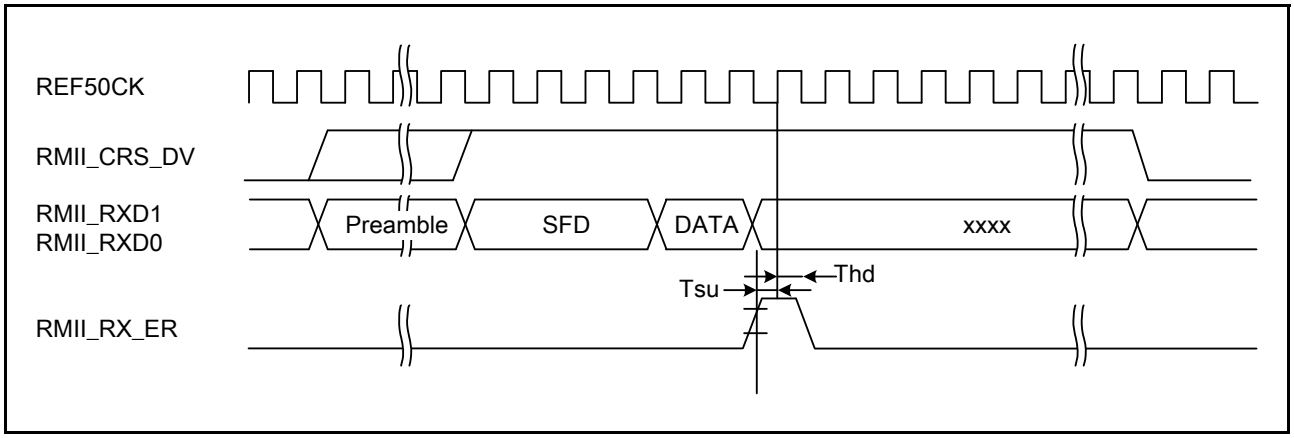


Figure 5.47 RMII Reception Timing (Error Occurrence)

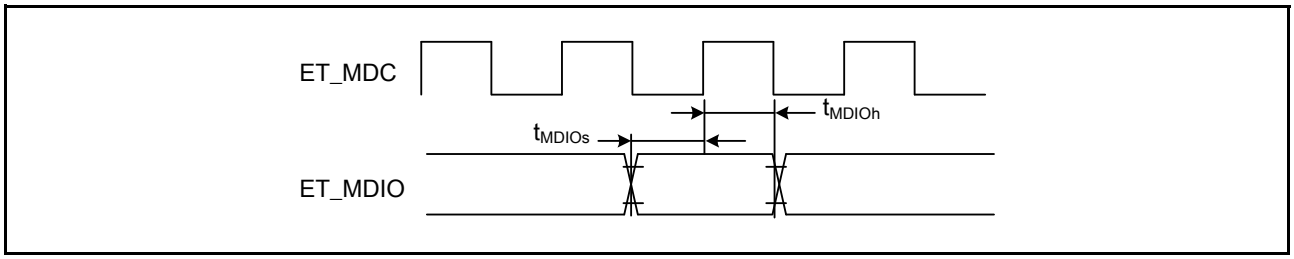


Figure 5.48 MDIO Input Timing (RMII)

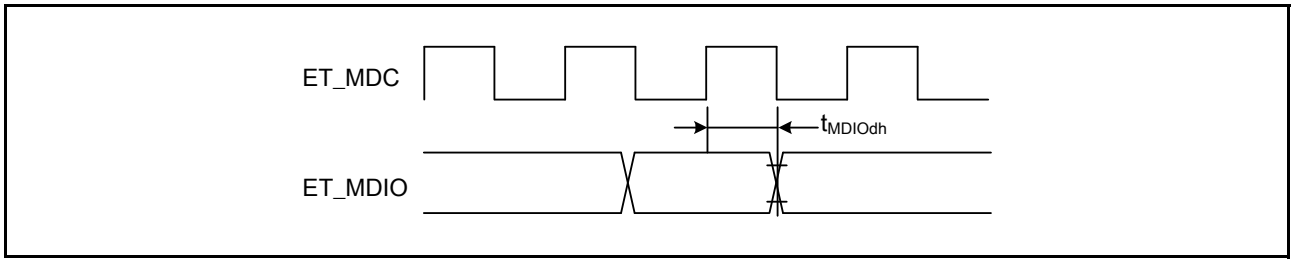


Figure 5.49 MDIO Output Timing (RMII)

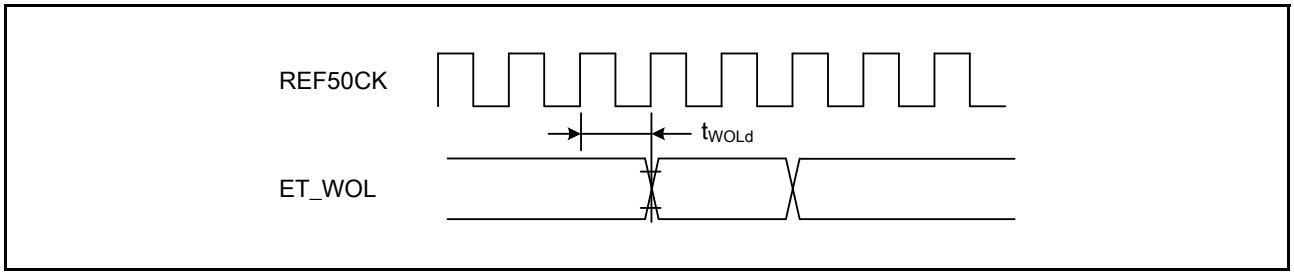


Figure 5.50 WOL Output Timing (RMII)

5.9 ROM (Flash Memory for Code Storage) Characteristics

Table 5.25 ROM (Flash Memory for Code Storage) Characteristics (1)

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
Temperature range for the programming/erasure operation: T_a = -40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Rewrite/erase cycle*1	N_{PEC}	1000	—	—	Times	
Data hold time	t_{DRP}	30*2	—	—	Year	T_a = +85°C

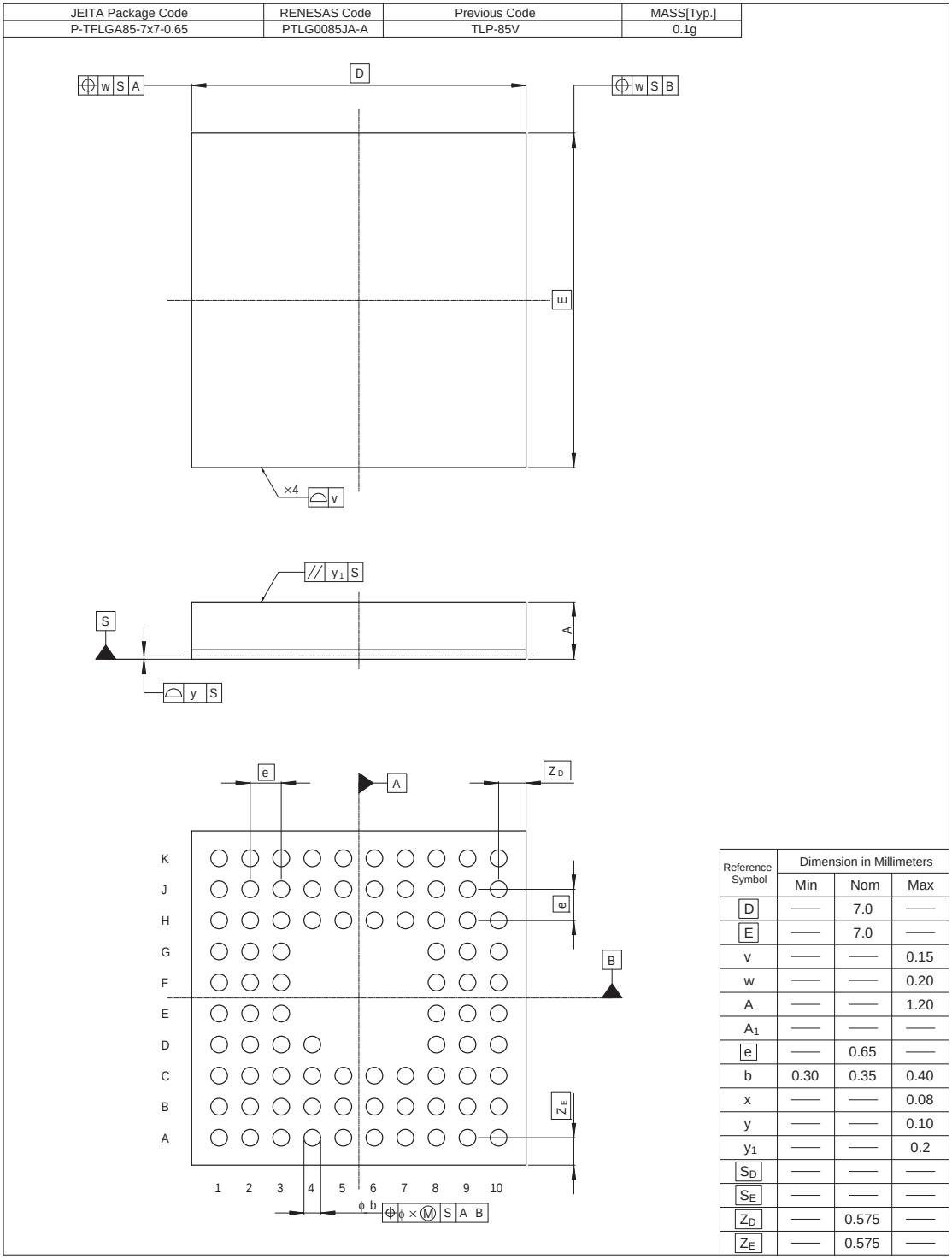
Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 256-byte programming is performed 16 times for different addresses in 4-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. The result obtained from the reliability test.

Table 5.26 ROM (Flash Memory for Code Storage) Characteristics (2)

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
Temperature range for the programming/erasure operation: T_a = -40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Programming time	256 bytes	t_{P256}	—	2	12	ms	PCLK = 50 MHz $N_{PEC} \leq 100$
	4 Kbytes	t_{P4K}	—	23	50	ms	
	16 Kbytes	t_{P16K}	—	90	200	ms	
	256 byte	t_{P256}	—	2.4	14.4	ms	PCLK = 50 MHz $N_{PEC} > 100$
	4 Kbytes	t_{P4K}	—	27.6	60	ms	
	16 Kbytes	t_{P16K}	—	108	240	ms	
Erasure time	4 Kbytes	t_{E4K}	—	25	60	ms	PCLK = 50 MHz $N_{PEC} \leq 100$
	16 Kbytes	t_{E16K}	—	100	240	ms	
	4 Kbytes	t_{E4K}	—	30	72	ms	PCLK = 50 MHz $N_{PEC} > 100$
	16 Kbytes	t_{E16K}	—	120	288	ms	
Suspend delay time during writing		t_{SPD}	—	—	120	µs	Figure 5.67 PCLK = 50-MHz operation
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	120	µs	
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	1.7	ms	
Suspend delay time during erasing (in erasure priority mode)		t_{SEED}	—	—	1.7	ms	

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA85-7x7-0.65	PTLG0085JA-A	TLP-85V	0.1g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	7.0	—
E	—	7.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.20
A_1	—	—	—
e	—	0.65	—
b	0.30	0.35	0.40
x	—	—	0.08
y	—	—	0.10
y_1	—	—	0.2
S_D	—	—	—
S_E	—	—	—
Z_D	—	0.575	—
Z_E	—	0.575	—

Figure E 85-Pin TFLGA (PTLG0085JA-A) Package Dimensions

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.40	Jul 16, 2014	4. I/O Registers		
		69, 70	Table 5.1 List of I/O Registers (Address Order), changed	TN-RX*-A012A/E
		5. Electrical Characteristics		
		91	Table 5.4 DC Characteristics (3), Note 1, changed	
		101 to 104	Figure 5.10 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized) to Figure 5.14 External Bus Timing/External Wait Control, changed	
		114	Table 5.13 Timing of On-Chip Peripheral Modules (2): SCI changed	
		140	Table 5.25 ROM (Flash Memory for Code Storage) Characteristics (1), Note 2, changed, Note 3, deleted, Table 5.26 ROM (Flash Memory for Code Storage) Characteristics (2), added	TN-RX*-A051A/E
		Appendix 2. Package Dimensions		
		145	Figure C 144-Pin LQFP (PLQP0144KA-A) Package Dimensions, Figure D 100-Pin LQFP (PLQP0100KB-A) Package Dimensions, changed	