Renesas Electronics America Inc - R5F56216BDFB#V0 Datasheet

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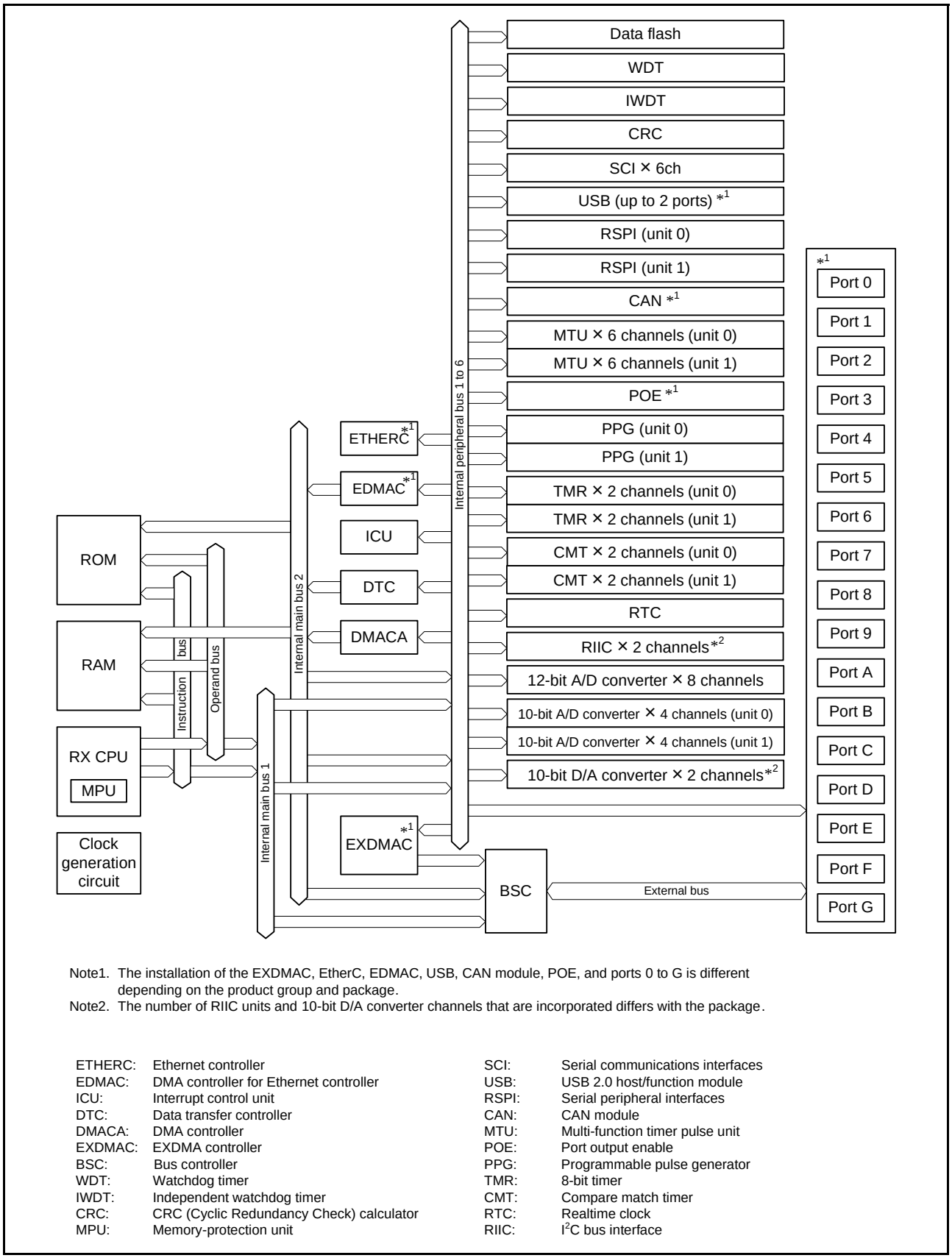
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	103
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10/12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f56216bdfb-v0

1.3 Block Diagram

Figure 1.2 shows a block diagram.



Note1. The installation of the EXDMAC, EtherC, EDMAC, USB, CAN module, POE, and ports 0 to G is different depending on the product group and package.
Note2. The number of RIIC units and 10-bit D/A converter channels that are incorporated differs with the package.

ETHERC:	Ethernet controller	SCI:	Serial communications interfaces
EDMAC:	DMA controller for Ethernet controller	USB:	USB 2.0 host/function module
ICU:	Interrupt control unit	RSPI:	Serial peripheral interfaces
DTC:	Data transfer controller	CAN:	CAN module
DMACA:	DMA controller	MTU:	Multi-function timer pulse unit
EXDMAC:	EXDMA controller	POE:	Port output enable
BSC:	Bus controller	PPG:	Programmable pulse generator
WDT:	Watchdog timer	TMR:	8-bit timer
IWDT:	Independent watchdog timer	CMT:	Compare match timer
CRC:	CRC (Cyclic Redundancy Check) calculator	RTC:	Realtime clock
MPU:	Memory-protection unit	RIIC:	I^2C bus interface

Figure 1.2 Block Diagram

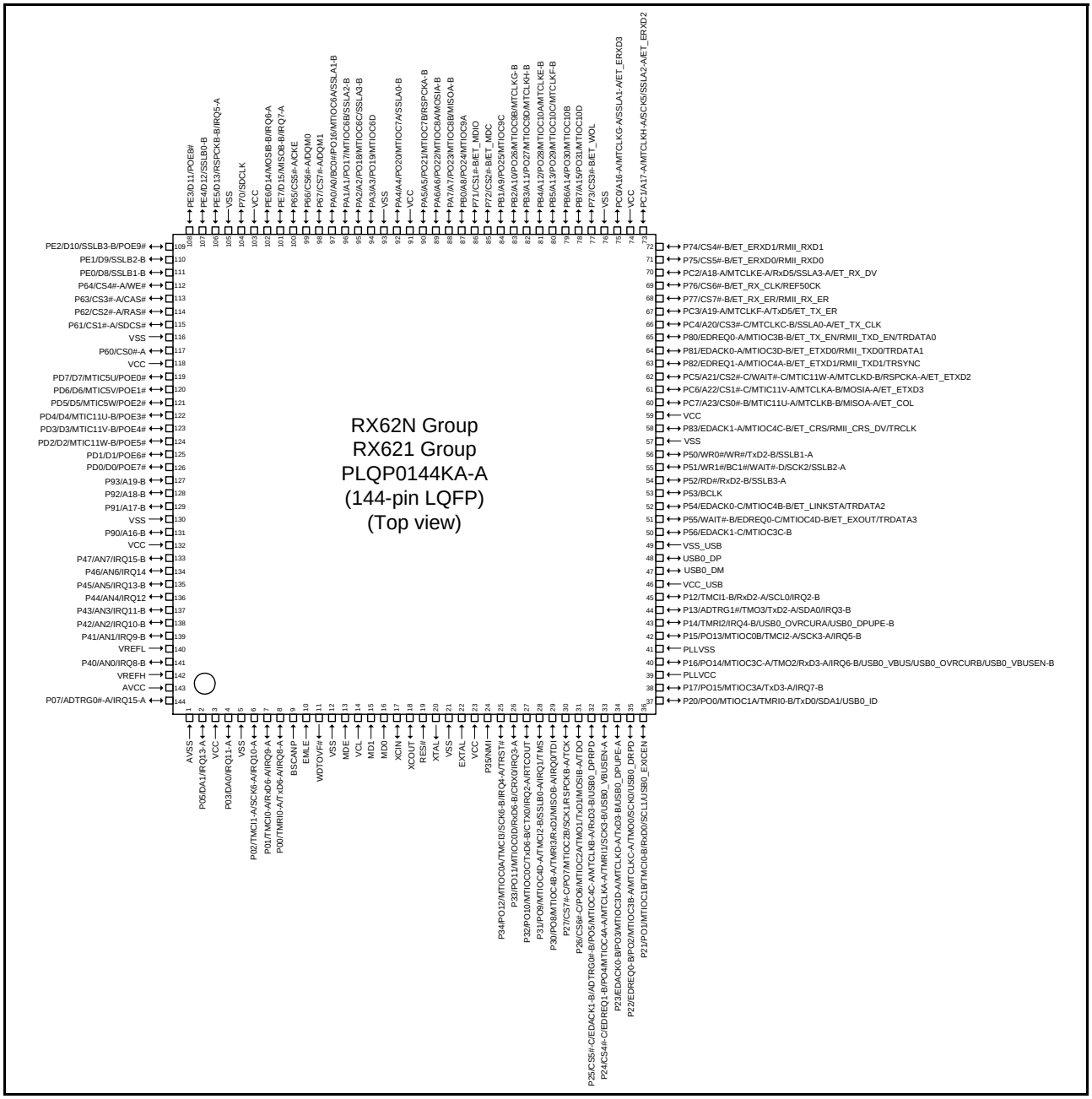


Figure 1.5 Pin Assignment of the 144-Pin LQFP

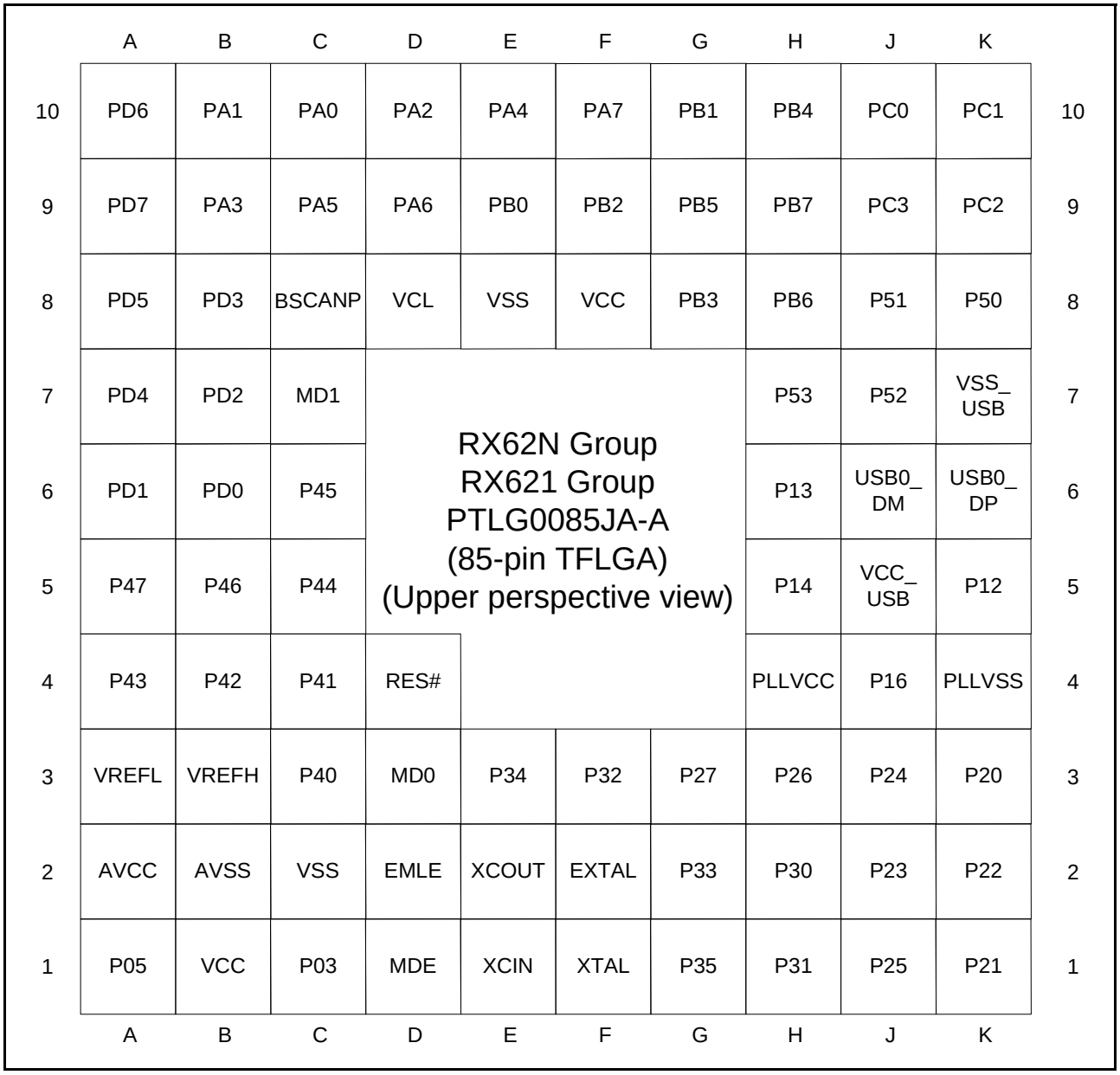


Figure 1.9 Pin Assignment of the 85-Pin TFLGA

Table 1.4 List of Pins and Pin Functions (176-Pin LFBGA) (3 / 6)

Pin No. 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	External Bus EXDMAC	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE, WDT)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
F15		PG5	D29					TRCLK
G1	VSS							
G2	MD1							
G3	MD0							
G4	MDE							
G12	VSS							
G13	VCC							
G14		PG6	D30					TRDATA2
G15		PA1	A1/DQM3			MTIOC6B/ PO17	SSLA2-B	
H1	XTAL							
H2		P35						NMI
H3	VCC							
H4	RES#							
H12		PG7	D31					TRDATA3
H13		PA2	A2			MTIOC6C/ PO18	SSLA3-B	
H14		PA4	A4			MTIOC7A/ PO20	SSLA0-B	
H15		PA3	A3			MTIOC6D/ PO19		
J1	EXTAL							
J2		P32				MTIOC0C/ PO10/ RTCOUT	CTX0/ TxD6-B	IRQ2-A
J3		PF3						TMS
J4		P34				MTIOC0A/ TMCI3-B/ PO12	SCK6-B	IRQ4-A
J12	VSS							
J13		PA5	A5			MTIOC7B/ PO21	RSPCKA-B	
J14		PA7	A7			MTIOC8B/ PO23	MISOA-B	
J15		PA6	A6			MTIOC8A/ PO22	MOSIA-B	
K1		P33				MTIOC0D/ PO11	CRX0/ RxD6-B	IRQ3-A
K2		P31			USB1_DPRPD	MTIOC4D-A/ TMCI2-B/ PO9	SSLB0-A	IRQ1-A
K3		PF0					TxD1-B	TDO
K4		PF4						TRST#
K12		PB1	A9			MTIOC9C/ PO25		
K13		P71	CS1#-B	ET_MDIO				
K14		P72	CS2#-B	ET_MDC				

Table 1.4 List of Pins and Pin Functions (176-Pin LFBGA) (5 / 6)

Pin No. 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	External Bus EXDMAC	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE, WDT)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
N2		P23	EDACK0-B		USB0_DPUPE-A	MTIOC3D-A/ MTCLKD-A/ PO3	TxD3-B	
N3		P20			USB0_ID	MTIOC1A/ TMRI0-B/ PO0	SDA1/ TxD0	
N4		P17			USB1_VBUS/ USB1_OVRCURB/ USB1_VBUSEN-B	MTIOC3A/ PO15	TxD3-A	IRQ7-B
N5		P15			USB1_OVRCURA/ USB1_DPUPE-B	MTIOC0B/ TMCI2-A/ PO13	SCK3-A	IRQ5-B
N6		P57	WAIT#-A/ WR3#/ BC3#/ EDREQ1-C					
N7		P10			USB1_DPUPE-A	MTIC5W-A/ TMRI3-A		IRQ0-B
N8		P52	RD#				SSLB3-A/ RxD2-B	
N9	VCC							
N10		PC5	A21-A/ CS2#-C/ WAIT#-C	ET_ETXD2		MTIC11W-A/ MTCLKD-B	RSPCKA-A	
N11		PC3	A19-A	ET_TX_ER		MTCLKF-A	TxD5	
N12		PC2	A18-A	ET_RX_DV		MTCLKE-A	SSLA3-A/ RxD5	
N13		P74	CS4#-B	ET_ERXD1/ RMII_RXD1				
N14		P73	CS3#-B	ET_WOL				
N15		PB5	A13			MTIOC10C/ MTCLKF-B/ PO29		
P1		P24	CS4#-C/ EDREQ1-B		USB0_VBUSEN-A	MTIOC4A-A/ MTCLKA-A/ TMRI1/ PO4	SCK3-B	
P2	PLLVCC							
P3		P16			USB0_VBUS/ USB0_OVRCURB/ USB0_VBUSEN-B	MTIOC3C-A/ TMO2/ PO14	RxD3-A	IRQ6-B
P4		P14			USB0_OVRCURA/ USB0_DPUPE-B	TMRI2		IRQ4-B
P5		P13				TMO3	SDA0/ TxD2-A	IRQ3-B/ ADTRG1#
P6	VCC_USB							

Table 1.4 List of Pins and Pin Functions (176-Pin LFBGA) (6 / 6)

Pin No. 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	External Bus EXDMAC	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE, WDT)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
P7		P56	WR2#/ BC2#/ EDACK1-C			MTIOC3C-B		
P8	VCC_USB							
P9		P84						
P10		P50	WR0#/ WR#				SSLB1-A/ TxD2-B	
P11		P82	EDREQ1-A	ET_ETXD1/ RMII_TXD1		MTIOC4A-B		
P12		PC4	A20-A/ CS3#-C	ET_TX_CLK		MTCLKC-B	SSLA0-A	
P13		P76	CS6#-B	ET_RX_CLK/ REF50CK				
P14		PC1	A17-A	ET_ERXD2		MTCLKH-A	SSLA2-A/ SCK5	
P15		PB7	A15			MTIOC10D/ PO31		
R1		P21			USB0_EXICEN	MTIOC1B/ TMCI0-B/ PO1	SCL1/ RxD0	
R2	PLLVSS							
R3		P12				MTIC5U-A/ TMCI1-B	SCL0/ RxD2-A	IRQ2-B
R4					USB0_DM			
R5					USB0_DP			
R6	VSS_USB							
R7					USB1_DM			
R8					USB1_DP			
R9		P85						
R10	BCLK	P53						
R11		P83	EDACK1-A	ET_CRS/ RMII_CRS_DV		MTIOC4C-B		
R12		PC7	A23-A/ CS0#-B	ET_COL		MTIC11U-A/ MTCLKB-B	MISOA-A	
R13		P80	EDREQ0-A	ET_TX_EN/ RMII_TXD_EN		MTIOC3B-B		
R14		P77	CS7#-B	ET_RX_ER/ RMII_RX_ER				
R15		P75	CS5#-B	ET_ERXD0/ RMII_RXD0				

Table 1.5 List of Pins and Pin Functions (145-Pin TFLGA) (3 / 5)

Pin No. 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	External Bus EXDMAC	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE, WDT)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
G3	MD1							
G4	MD0							
G10	VSS							
G11		PA5	A5			MTIOC7B/ PO21	RSPCKA-B	
G12		PA6	A6			MTIOC8A/ PO22	MOSIA-B	
G13		PA4	A4			MTIOC7A/ PO20	SSLA0-B	
H1	EXTAL							
H2		P34				MTIOC0A/ TMCI3/ PO12	SCK6-B	IRQ4-A/ TRST#
H3	VCC							
H4	RES#							
H10		PB0	A8			MTIOC9A/ PO24		
H11		P71	CS1#-B	ET_MDIO				
H12		PB1	A9			MTIOC9C/ PO25		
H13		PA7	A7			MTIOC8B/ PO23	MISOA-B	
J1		P33				MTIOC0D/ PO11	CRX0/ RxD6-B	IRQ3-A
J2		P27	CS7#-C			MTIOC2B/ PO7	RSPCKB-A/ SCK1	TCK
J3		P35						NMI
J4		P32				MTIOC0C/ PO10/ RTCOUT	CTX0/ TxD6-B	IRQ2-A
J10		PB2	A10			MTIOC9B/ MTCLKG-B/ PO26		
J11		PB4	A12			MTIOC10A/ MTCLKE-B/ PO28		
J12		PB5	A13			MTIOC10C/ MTCLKF-B/ PO29		
J13		P72	CS2#-B	ET_MDC				
K1		P30				MTIOC4B-A/ TMRI3/ PO8	RxD1/ MISOB-A	IRQ0/ TDI
K2		P24	CS4#-C/ EDREQ1-B		USB0_VBUSEN-A	MTIOC4A-A/ MTCLKA-A/ TMRI1/PO4	SCK3-B	
K3		P31				MTIOC4D-A/ TMCI2-B/ PO9	SSLB0-A	IRQ1/ TMS

Table 1.5 List of Pins and Pin Functions (145-Pin TFLGA) (4 / 5)

Pin No. 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	External Bus EXDMAC	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE, WDT)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
K4		P26	CS6#-C			MTIOC2A/ TMO1/ PO6	MOSIB-A/ TxD1	TDO
K5	BCLK	P53						
K6	VSS							
K7		PC7	A23/ CS0#-B	ET_COL		MTIC11U-A/ MTCLKB-B	MISOA-A	
K8		P82	EDREQ1-A	ET_ETXD1/ RMII_TXD1		MTIOC4A-B		TRSYNC
K9		PC3	A19-A	ET_TX_ER		MTCLKF-A	TxD5	
K10		PB7	A15			MTIOC10D/ PO31		
K11		P73	CS3#-B	ET_WOL				
K12		PC0	A16-A	ET_ERXD3		MTCLKG-A	SSLA1-A	
K13		PB3	A11			MTIOC9D/ MTCLKH-B/ PO27		
L1		P25	CS5#-C/ EDACK1-B		USB0_DPRPD	MTIOC4C-A/ MTCLKB-A/ PO5	RxD3-B	ADTRG0#-B
L2		P22	EDREQ0-B		USB0_DRPD	MTIOC3B-A/ MTCLKC-A/ TMO0/PO2	SCK0	
L3		P17				MTIOC3A/ PO15	TxD3-A	IRQ7-B
L4		P12				TMCI1-B	SCL0/ RxD2-A	IRQ2-B
L5	VCC_USB							
L6		P56	EDACK1-C			MTIOC3C-B		
L7		P52	RD#				SSLB3-A/ RxD2-B	
L8		P83	EDACK1-A	ET_CRS/ RMII_CRS_DV		MTIOC4C-B		TRCLK
L9		P81	EDACK0-A	ET_ETXD0/ RMII_TXD0		MTIOC3D-B		TRDATA1
L10		P77	CS7#-B	ET_RX_ER/ RMII_RX_ER				
L11		P75	CS5#-B	ET_ERXD0/ RMII_RXD0				
L12	VCC							
L13		PB6	A14			MTIOC10B/ PO30		
M1		P23	EDACK0-B		USB0_DPUPE-A	MTIOC3D-A/ MTCLKD-A/ PO3	TxD3-B	
M2		P20			USB0_ID	MTIOC1A/ TMRI0-B/ PO0	SDA1/ TxD0	
M3	PLLVCC							

Table 1.8 List of Pins and Pin Functions (85-Pin TFLGA) (1 / 3)

Pin No. 85-Pin TFLGA	Power Supply Clock System Control	I/O Port	External Bus	USB	Timers (MTU, TMR, PPG)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
A1		P05					DA1/ IRQ13-A
A2	AVCC						
A3	VREFL						
A4		P43					IRQ11-B/AN3
A5		P47					IRQ15/ AN7
A6		PD1	D1				
A7		PD4	D4		MTIC11U		
A8		PD5	D5		MTIC5W		
A9		PD7	D7		MTIC5U		
A10		PD6	D6		MTIC5V		
B1	VCC						
B2	AVSS						
B3	VREFH						
B4		P42					IRQ10/ AN2
B5		P46					IRQ14/ AN6
B6		PD0	D0				
B7		PD2	D2		MTIC11W		
B8		PD3	D3		MTIC11V		
B9		PA3	A3		MTIOC6D/PO19		
B10		PA1	A1		MTIOC6B/PO17	SSLA2	
C1		P03					IRQ11-A/DA0
C2	VSS						
C3		P40					IRQ8/ AN0
C4		P41					IRQ9/ AN1
C5		P44					IRQ12/ AN4
C6		P45					IRQ13-B/AN5
C7	MD1						
C8	BSCANP						
C9		PA5	A5		MTIOC7B/PO21	RSPCKA	
C10		PA0	A0		MTIOC6A/PO16	SSLA1	
D1	MDE						
D2	EMLE						
D3	MD0						
D4	RES#						

Table 4.1 List of I/O Registers (Address Order) (9 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 7125h	ICU	DTC activation enable register 037	DTCER037	8	8	2 ICLK
0008 7128h	ICU	DTC activation enable register 040	DTCER040	8	8	2 ICLK
0008 7129h	ICU	DTC activation enable register 041	DTCER041	8	8	2 ICLK
0008 712Dh	ICU	DTC activation enable register 045	DTCER045	8	8	2 ICLK
0008 712Eh	ICU	DTC activation enable register 046	DTCER046	8	8	2 ICLK
0008 7131h	ICU	DTC activation enable register 049	DTCER049	8	8	2 ICLK
0008 7132h	ICU	DTC activation enable register 050	DTCER050	8	8	2 ICLK
0008 7140h	ICU	DTC activation enable register 064	DTCER064	8	8	2 ICLK
0008 7141h	ICU	DTC activation enable register 065	DTCER065	8	8	2 ICLK
0008 7142h	ICU	DTC activation enable register 066	DTCER066	8	8	2 ICLK
0008 7143h	ICU	DTC activation enable register 067	DTCER067	8	8	2 ICLK
0008 7144h	ICU	DTC activation enable register 068	DTCER068	8	8	2 ICLK
0008 7145h	ICU	DTC activation enable register 069	DTCER069	8	8	2 ICLK
0008 7146h	ICU	DTC activation enable register 070	DTCER070	8	8	2 ICLK
0008 7147h	ICU	DTC activation enable register 071	DTCER071	8	8	2 ICLK
0008 7148h	ICU	DTC activation enable register 072	DTCER072	8	8	2 ICLK
0008 7149h	ICU	DTC activation enable register 073	DTCER073	8	8	2 ICLK
0008 714Ah	ICU	DTC activation enable register 074	DTCER074	8	8	2 ICLK
0008 714Bh	ICU	DTC activation enable register 075	DTCER075	8	8	2 ICLK
0008 714Ch	ICU	DTC activation enable register 076	DTCER076	8	8	2 ICLK
0008 714Dh	ICU	DTC activation enable register 077	DTCER077	8	8	2 ICLK
0008 714Eh	ICU	DTC activation enable register 078	DTCER078	8	8	2 ICLK
0008 714Fh	ICU	DTC activation enable register 079	DTCER079	8	8	2 ICLK
0008 7162h	ICU	DTC activation enable register 098	DTCER098	8	8	2 ICLK
0008 7163h	ICU	DTC activation enable register 099	DTCER099	8	8	2 ICLK
0008 7166h	ICU	DTC activation enable register 102	DTCER102	8	8	2 ICLK
0008 7172h	ICU	DTC activation enable register 114	DTCER114	8	8	2 ICLK
0008 7173h	ICU	DTC activation enable register 115	DTCER115	8	8	2 ICLK
0008 7174h	ICU	DTC activation enable register 116	DTCER116	8	8	2 ICLK
0008 7175h	ICU	DTC activation enable register 117	DTCER117	8	8	2 ICLK
0008 7179h	ICU	DTC activation enable register 121	DTCER121	8	8	2 ICLK
0008 717Ah	ICU	DTC activation enable register 122	DTCER122	8	8	2 ICLK
0008 717Dh	ICU	DTC activation enable register 125	DTCER125	8	8	2 ICLK
0008 717Eh	ICU	DTC activation enable register 126	DTCER126	8	8	2 ICLK
0008 7181h	ICU	DTC activation enable register 129	DTCER129	8	8	2 ICLK
0008 7182h	ICU	DTC activation enable register 130	DTCER130	8	8	2 ICLK
0008 7183h	ICU	DTC activation enable register 131	DTCER131	8	8	2 ICLK
0008 7184h	ICU	DTC activation enable register 132	DTCER132	8	8	2 ICLK
0008 7186h	ICU	DTC activation enable register 134	DTCER134	8	8	2 ICLK
0008 7187h	ICU	DTC activation enable register 135	DTCER135	8	8	2 ICLK
0008 7188h	ICU	DTC activation enable register 136	DTCER136	8	8	2 ICLK
0008 7189h	ICU	DTC activation enable register 137	DTCER137	8	8	2 ICLK
0008 718Ah	ICU	DTC activation enable register 138	DTCER138	8	8	2 ICLK
0008 718Bh	ICU	DTC activation enable register 139	DTCER139	8	8	2 ICLK
0008 718Ch	ICU	DTC activation enable register 140	DTCER140	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (20 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 839Ah	RSPI0	RSPI command register 5	SPCMD5	16	16	2 to 3 PCLK*8
0008 839Ch	RSPI0	RSPI command register 6	SPCMD6	16	16	2 to 3 PCLK*8
0008 839Eh	RSPI0	RSPI command register 7	SPCMD7	16	16	2 to 3 PCLK*8
0008 83A0h	RSPI1	RSPI control register	SPCR	8	8	2 to 3 PCLK*8
0008 83A1h	RSPI1	RSPI slave select polarity register	SSLP	8	8	2 to 3 PCLK*8
0008 83A2h	RSPI1	RSPI pin control register	SPPCR	8	8	2 to 3 PCLK*8
0008 83A3h	RSPI1	RSPI status register	SPSR	8	8	2 to 3 PCLK*8
0008 83A4h	RSPI1	RSPI data register	SPDR	32	16, 32	2 to 3 PCLK*8
0008 83A8h	RSPI1	RSPI sequence control register	SPSCR	8	8	2 to 3 PCLK*8
0008 83A9h	RSPI1	RSPI sequence status register	SPSSR	8	8	2 to 3 PCLK*8
0008 83AAh	RSPI1	RSPI bit rate register	SPBR	8	8	2 to 3 PCLK*8
0008 83ABh	RSPI1	RSPI data control register	SPDCR	8	8	2 to 3 PCLK*8
0008 83ACh	RSPI1	RSPI clock delay register	SPCKD	8	8	2 to 3 PCLK*8
0008 83ADh	RSPI1	RSPI slave select negation delay register	SSLND	8	8	2 to 3 PCLK*8
0008 83AEh	RSPI1	RSPI next-access delay register	SPND	8	8	2 to 3 PCLK*8
0008 83AFh	RSPI1	RSPI control register 2	SPCR2	8	8	2 to 3 PCLK*8
0008 83B0h	RSPI1	RSPI command register 0	SPCMD0	16	16	2 to 3 PCLK*8
0008 83B2h	RSPI1	RSPI command register 1	SPCMD1	16	16	2 to 3 PCLK*8
0008 83B4h	RSPI1	RSPI command register 2	SPCMD2	16	16	2 to 3 PCLK*8
0008 83B6h	RSPI1	RSPI command register 3	SPCMD3	16	16	2 to 3 PCLK*8
0008 83B8h	RSPI1	RSPI command register 4	SPCMD4	16	16	2 to 3 PCLK*8
0008 83BAh	RSPI1	RSPI command register 5	SPCMD5	16	16	2 to 3 PCLK*8
0008 83BCh	RSPI1	RSPI command register 6	SPCMD6	16	16	2 to 3 PCLK*8
0008 83BEh	RSPI1	RSPI command register 7	SPCMD7	16	16	2 to 3 PCLK*8
0008 8600h	MTU3	Timer control register	TCR	8	8	2 to 3 PCLK*8
0008 8601h	MTU4	Timer control register	TCR	8	8	2 to 3 PCLK*8
0008 8602h	MTU3	Timer mode register	TMDR	8	8	2 to 3 PCLK*8
0008 8603h	MTU4	Timer mode register	TMDR	8	8	2 to 3 PCLK*8
0008 8604h	MTU3	Timer I/O control register H	TIORH	8	8	2 to 3 PCLK*8
0008 8605h	MTU3	Timer I/O control register L	TIORL	8	8	2 to 3 PCLK*8
0008 8606h	MTU4	Timer I/O control register H	TIORH	8	8	2 to 3 PCLK*8
0008 8607h	MTU4	Timer I/O control register L	TIORL	8	8	2 to 3 PCLK*8
0008 8608h	MTU3	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK*8
0008 8609h	MTU4	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK*8
0008 860Ah	MTUA	Timer output master enable register	TOER	8	8	2 to 3 PCLK*8
0008 860Dh	MTUA	Timer gate control register	TGCR	8	8	2 to 3 PCLK*8
0008 860Eh	MTUA	Timer output control register 1	TOCR1	8	8	2 to 3 PCLK*8
0008 860Fh	MTUA	Timer output control register 2	TOCR2	8	8	2 to 3 PCLK*8
0008 8610h	MTU3	Timer counter	TCNT	16	16	2 to 3 PCLK*8
0008 8612h	MTU4	Timer counter	TCNT	16	16	2 to 3 PCLK*8
0008 8614h	MTUA	Timer cycle data register	TCDR	16	16	2 to 3 PCLK*8
0008 8616h	MTUA	Timer dead time data register	TDDR	16	16	2 to 3 PCLK*8
0008 8618h	MTU3	Timer general register A	TGRA	16	16	2 to 3 PCLK*8
0008 861Ah	MTU3	Timer general register B	TGRB	16	16	2 to 3 PCLK*8
0008 861Ch	MTU4	Timer general register A	TGRA	16	16	2 to 3 PCLK*8

Table 4.1 List of I/O Registers (Address Order) (25 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 8C94h	MTU11	Timer control register V	TCRV	8	8	2 to 3 PCLK*8
0008 8C96h	MTU11	Timer I/O control register V	TIORV	8	8	2 to 3 PCLK*8
0008 8CA0h	MTU11	Timer counter W	TCNTW	16	16	2 to 3 PCLK*8
0008 8CA2h	MTU11	Timer general register W	TGRW	16	16	2 to 3 PCLK*8
0008 8CA4h	MTU11	Timer control register W	TCRW	8	8	2 to 3 PCLK*8
0008 8CA6h	MTU11	Timer I/O control register W	TIORW	8	8	2 to 3 PCLK*8
0008 8CB2h	MTU11	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK*8
0008 8CB4h	MTU11	Timer start register	TSTR	8	8	2 to 3 PCLK*8
0008 8CB6h	MTU11	Timer compare match clear register	TCNTCMPCLR	8	8	2 to 3 PCLK*8
0008 9000h	S12AD	A/D control register	ADCSR	8	8	2 to 3 PCLK*8
0008 9004h	S12AD	A/D channel select register	ADANS	16	16	2 to 3 PCLK*8
0008 9008h	S12AD	A/D-converted value addition mode select register	ADADS	16	16	2 to 3 PCLK*8
0008 900Ch	S12AD	A/D-converted value addition count select register	ADADC	8	8	2 to 3 PCLK*8
0008 900Eh	S12AD	A/D control extended register	ADCER	16	16	2 to 3 PCLK*8
0008 9010h	S12AD	A/D start trigger select register	ADSTRGR	8	8	2 to 3 PCLK*8
0008 9020h	S12AD	A/D data register 0	ADDR0	16	16	2 to 3 PCLK*8
0008 9022h	S12AD	A/D data register 1	ADDR1	16	16	2 to 3 PCLK*8
0008 9024h	S12AD	A/D data register 2	ADDR2	16	16	2 to 3 PCLK*8
0008 9026h	S12AD	A/D data register 3	ADDR3	16	16	2 to 3 PCLK*8
0008 9028h	S12AD	A/D data register 4	ADDR4	16	16	2 to 3 PCLK*8
0008 902Ah	S12AD	A/D data register 5	ADDR5	16	16	2 to 3 PCLK*8
0008 902Ch	S12AD	A/D data register 6	ADDR6	16	16	2 to 3 PCLK*8
0008 902Eh	S12AD	A/D data register 7	ADDR7	16	16	2 to 3 PCLK*8
0008 C000h	PORT0	Data direction register	DDR	8	8	2 to 3 PCLK*8
0008 C001h	PORT1	Data direction register	DDR	8	8	2 to 3 PCLK*8
0008 C002h	PORT2	Data direction register	DDR	8	8	2 to 3 PCLK*8
0008 C003h	PORT3	Data direction register	DDR	8	8	2 to 3 PCLK*8
0008 C004h	PORT4	Data direction register	DDR	8	8	2 to 3 PCLK*8
0008 C005h	PORT5	Data direction register	DDR	8	8	2 to 3 PCLK*8
0008 C006h	PORT6	Data direction register	DDR*6*7	8	8	2 to 3 PCLK*8
0008 C007h	PORT7	Data direction register	DDR*6*7	8	8	2 to 3 PCLK*8
0008 C008h	PORT8	Data direction register	DDR*6*7	8	8	2 to 3 PCLK*8
0008 C009h	PORT9	Data direction register	DDR*6*7	8	8	2 to 3 PCLK*8
0008 C00Ah	PORTA	Data direction register	DDR	8	8	2 to 3 PCLK*8
0008 C00Bh	PORTB	Data direction register	DDR	8	8	2 to 3 PCLK*8
0008 C00Ch	PORTC	Data direction register	DDR	8	8	2 to 3 PCLK*8
0008 C00Dh	PORTD	Data direction register	DDR	8	8	2 to 3 PCLK*8
0008 C00Eh	PORTE	Data direction register	DDR*7	8	8	2 to 3 PCLK*8
0008 C00Fh	PORTF	Data direction register	DDR*5*6*7	8	8	2 to 3 PCLK*8
0008 C010h	PORTG	Data direction register	DDR*5*6*7	8	8	2 to 3 PCLK*8
0008 C020h	PORT0	Data register	DR	8	8	2 to 3 PCLK*8
0008 C021h	PORT1	Data register	DR	8	8	2 to 3 PCLK*8
0008 C022h	PORT2	Data register	DR	8	8	2 to 3 PCLK*8

Table 4.1 List of I/O Registers (Address Order) (31 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000A 0060h	USB0	DCP control register	DCPCTR	16	16	at least 9 PCLK*9
000A 0064h	USB0	Pipe window select register	PIPESEL	16	16	at least 9 PCLK*9
000A 0068h	USB0	Pipe configuration register	PIPECFG	16	16	at least 9 PCLK*9
000A 006Ch	USB0	Pipe maximum packet size register	PIPEMAXP	16	16	at least 9 PCLK*9
000A 006Eh	USB0	Pipe cycle control register	PIPEPERI	16	16	at least 9 PCLK*9
000A 0070h	USB0	Pipe 1 control register	PIPE1CTR	16	16	at least 9 PCLK*9
000A 0072h	USB0	Pipe 2 control register	PIPE2CTR	16	16	at least 9 PCLK*9
000A 0074h	USB0	Pipe 3 control register	PIPE3CTR	16	16	at least 9 PCLK*9
000A 0076h	USB0	Pipe 4 control register	PIPE4CTR	16	16	at least 9 PCLK*9
000A 0078h	USB0	Pipe 5 control register	PIPE5CTR	16	16	at least 9 PCLK*9
000A 007Ah	USB0	Pipe 6 control register	PIPE6CTR	16	16	at least 9 PCLK*9
000A 007Ch	USB0	Pipe 7 control register	PIPE7CTR	16	16	at least 9 PCLK*9
000A 007Eh	USB0	Pipe 8 control register	PIPE8CTR	16	16	at least 9 PCLK*9
000A 0080h	USB0	Pipe 9 control register	PIPE9CTR	16	16	at least 9 PCLK*9
000A 0090h	USB0	Pipe 1 transaction counter enable register	PIPE1TRE	16	16	at least 9 PCLK*9
000A 0092h	USB0	Pipe 1 transaction counter register	PIPE1TRN	16	16	at least 9 PCLK*9
000A 0094h	USB0	Pipe 2 transaction counter enable register	PIPE2TRE	16	16	at least 9 PCLK*9
000A 0096h	USB0	Pipe 2 transaction counter register	PIPE2TRN	16	16	at least 9 PCLK*9
000A 0098h	USB0	Pipe 3 transaction counter enable register	PIPE3TRE	16	16	at least 9 PCLK*9
000A 009Ah	USB0	Pipe 3 transaction counter register	PIPE3TRN	16	16	at least 9 PCLK*9
000A 009Ch	USB0	Pipe 4 transaction counter enable register	PIPE4TRE	16	16	at least 9 PCLK*9
000A 009Eh	USB0	Pipe 4 transaction counter register	PIPE4TRN	16	16	at least 9 PCLK*9
000A 00A0h	USB0	Pipe 5 transaction counter enable register	PIPE5TRE	16	16	at least 9 PCLK*9
000A 00A2h	USB0	Pipe 5 transaction counter register	PIPE5TRN	16	16	at least 9 PCLK*9
000A 00D0h	USB0	Device address 0 configuration register	DEVADD0	16	16	at least 9 PCLK*9
000A 00D2h	USB0	Device address 1 configuration register	DEVADD1	16	16	at least 9 PCLK*9

5.2 DC Characteristics

Table 5.2 DC Characteristics (1)

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
T_a = -40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	IRQ input pin*1 MTU input pin*1 TMR input pin*1 SCI input pin*1 ADTRG input pin*1 RES#, NMI	V_{IH}	VCC × 0.8	—	VCC+0.3	V	
		V_{IL}	-0.3	—	VCC × 0.2		
		ΔV_T	VCC × 0.06	—	—		
	RIIC input pin (except for SMBus)	V_{IH}	VCC × 0.7	—	5.8		
		V_{IL}	-0.3	—	VCC × 0.3		
		ΔV_T	VCC × 0.05	—	—		
	Ports 00 to 02, 07 ports 12, 13, 16, 17 ports 20, 21 port 33	V_{IH}	VCC × 0.8	—	5.8		
		V_{IL}	-0.3	—	VCC × 0.2		
	Ports 03, 05, 10, 11, 14, 15 ports 22 to 27 ports 30 to 32, 34, 35 ports 4 to G Other input pins	V_{IH}	VCC × 0.8	—	VCC+0.3		
		V_{IL}	-0.3	—	VCC × 0.2		
Input high voltage (except Schmitt trigger input pin)	MD pin, EMLE	V_{IH}	VCC × 0.9	—	VCC+0.3	V	
	EXTAL, RSPI, ETHERC EXDMAC, WAIT#, TCK		VCC × 0.8	—	VCC+0.3		
	XCIN		VCC × 0.8	—	VCC+0.3		
	D0 to D31		VCC × 0.7	—	VCC+0.3		
	RIIC (SMBus)		2.1	—	VCC+0.3		
Input low voltage (except Schmitt trigger input pin)	MD pin, EMLE	V_{IL}	-0.3	—	VCC × 0.1	V	
	EXTAL, RSPI, ETHERC EXDMAC, WAIT#, TCK		-0.3	—	VCC × 0.2		
	XCIN		-0.3	—	VCC×0.2		
	D0 to D31		-0.3	—	VCC×0.3		
	RIIC (SMBus)		-0.3	—	0.8		

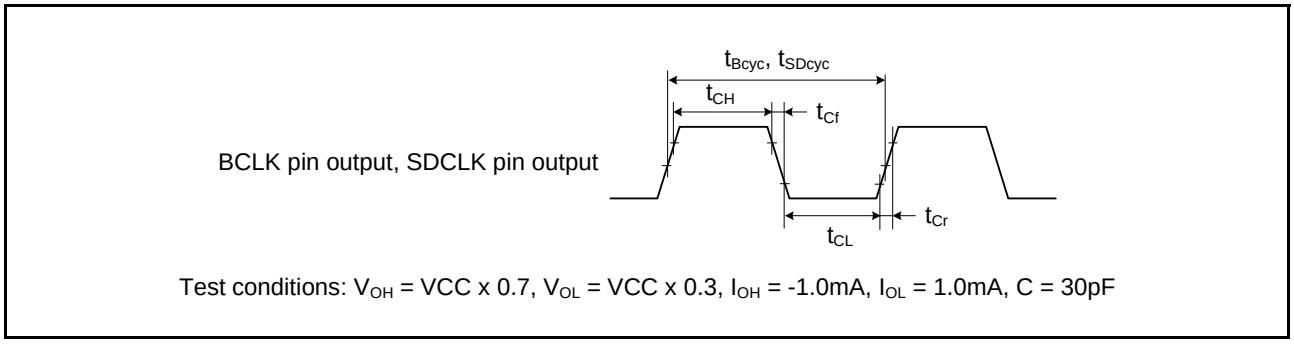


Figure 5.1 BCLK Pin Output, SDCLK Pin Output Timing

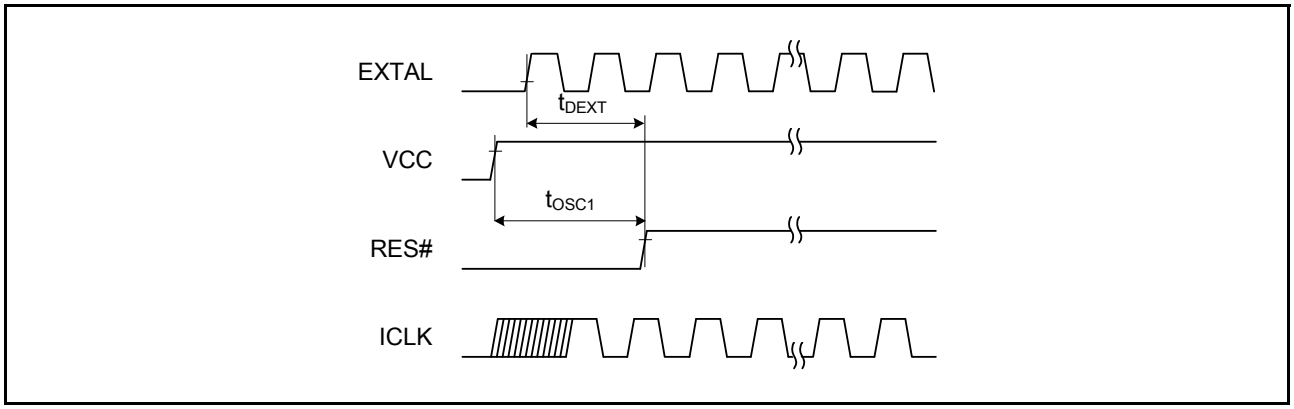


Figure 5.2 Oscillation Settling Timing

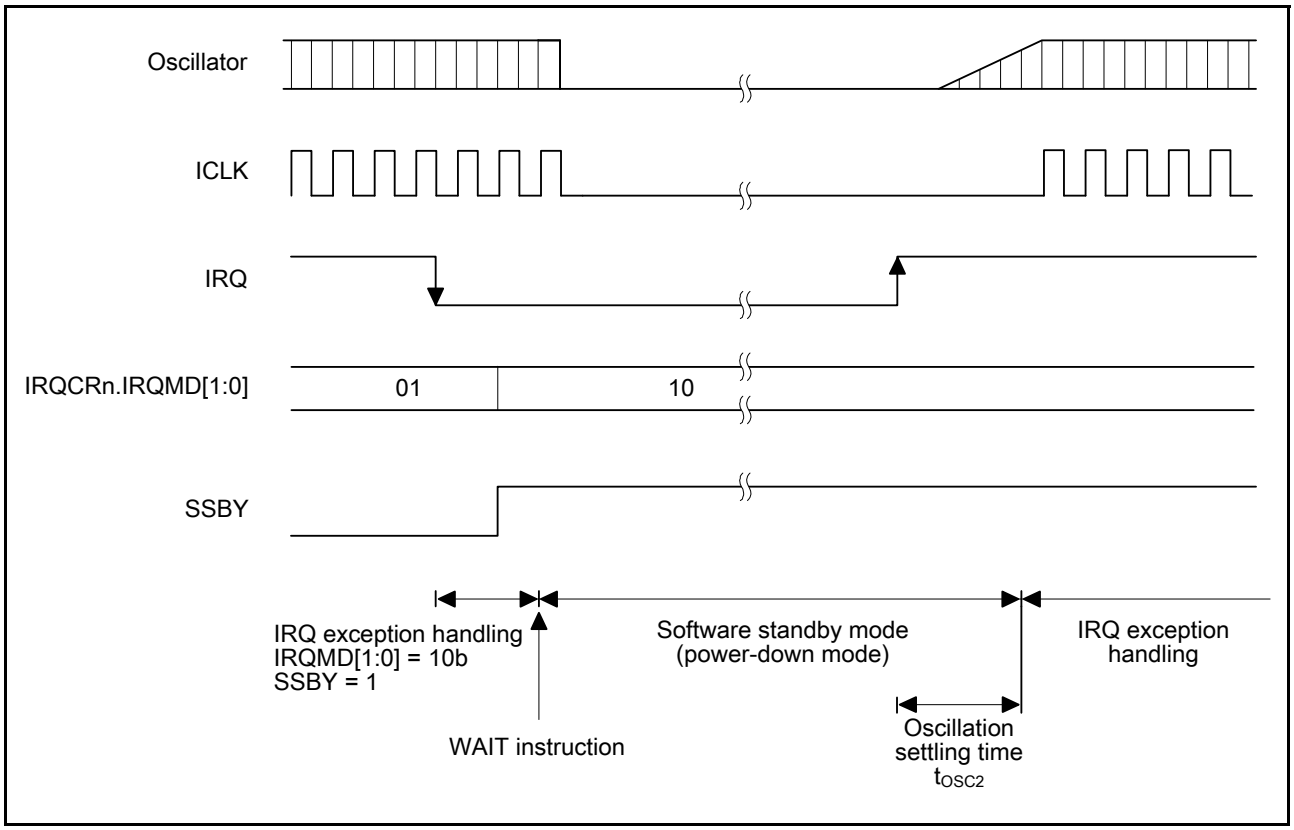


Figure 5.3 Oscillation Settling Timing after Software Standby Mode

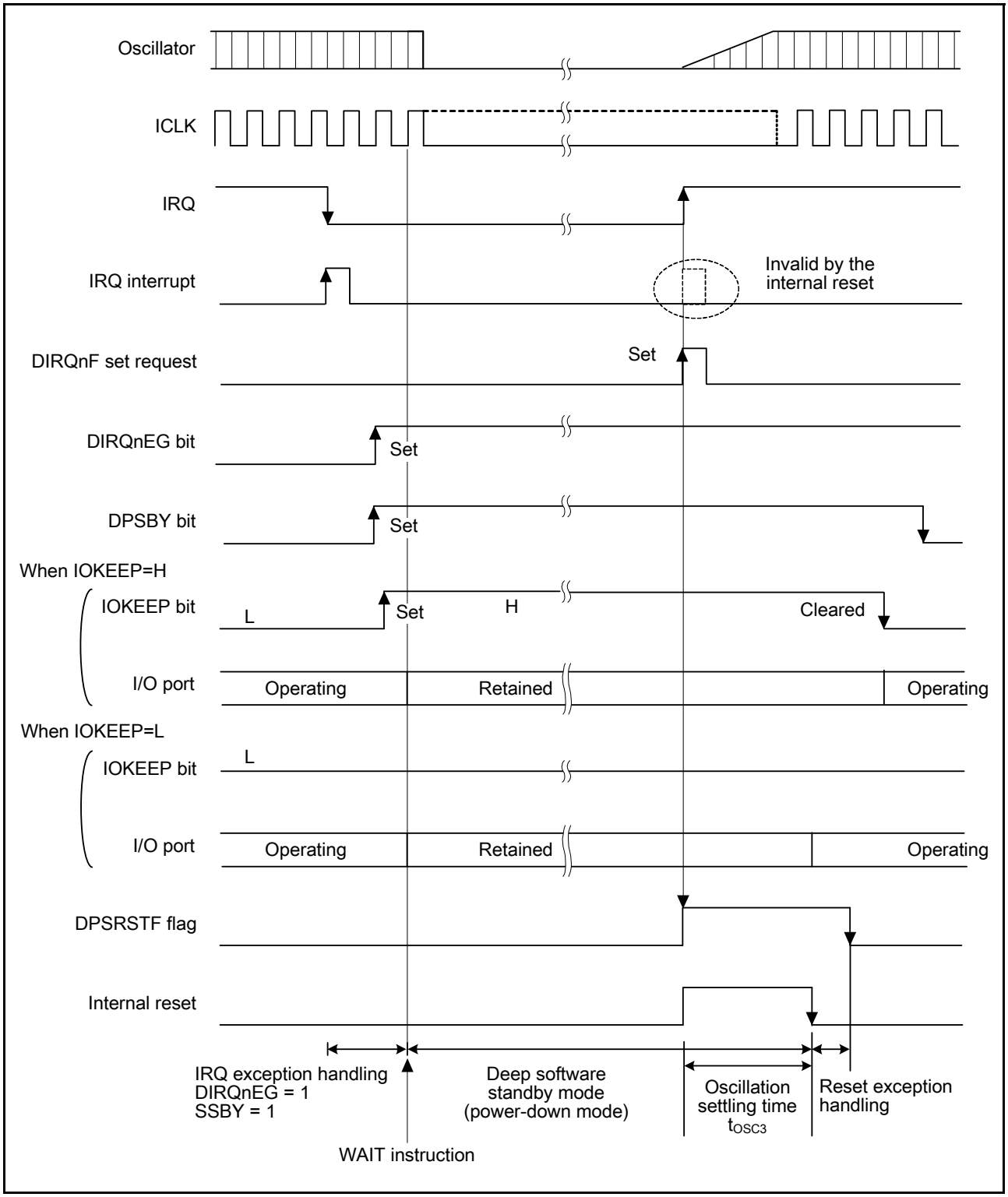
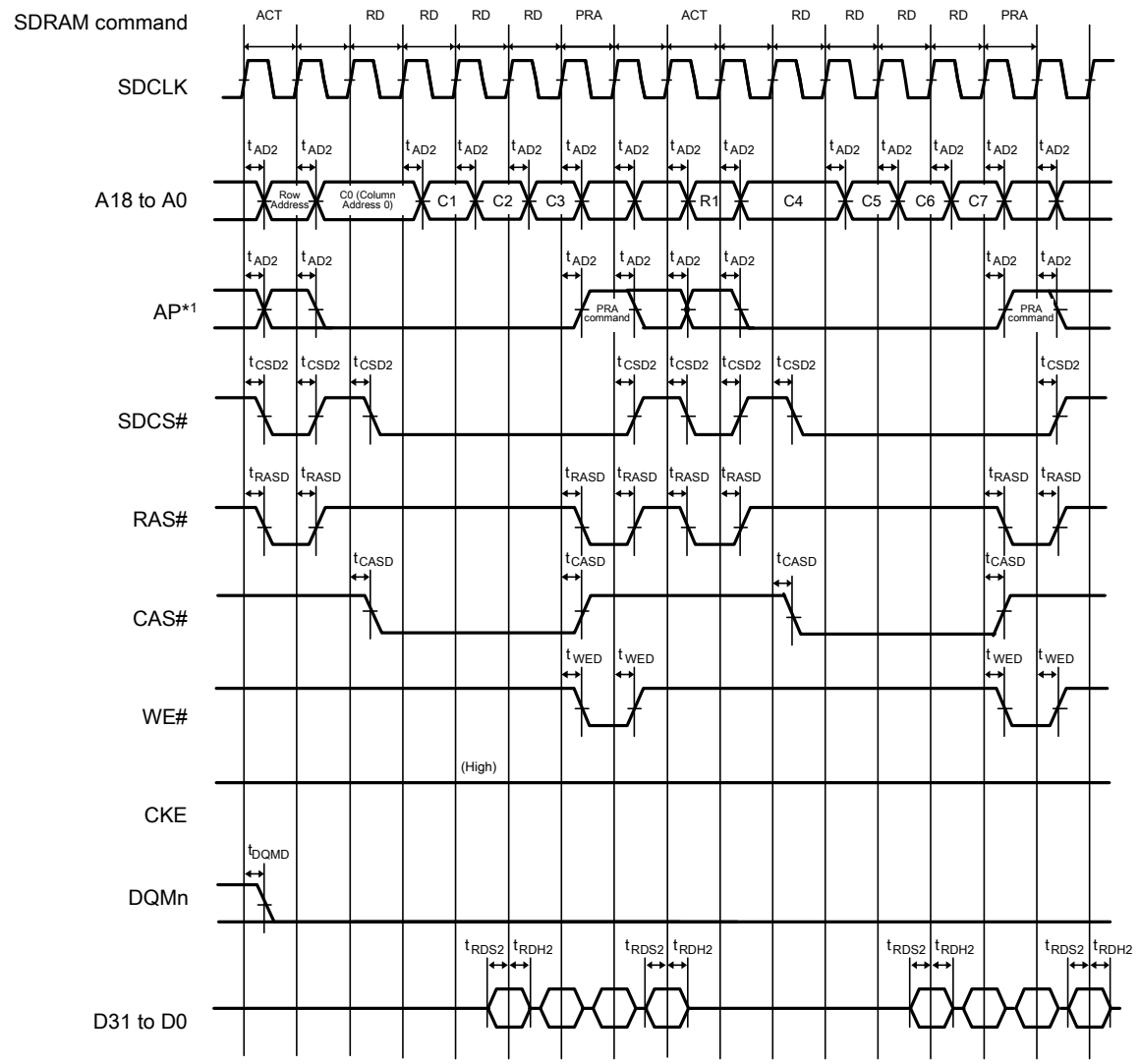


Figure 5.4 Oscillation Settling Timing after Deep Software Standby Mode



Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.19 SDRAM Space Multiple Read Line Stride Bus Timing

Table 5.17 Timing of On-Chip Peripheral Modules (9)

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
ICLK = 12.5 to 100 MHz
T_a = -40 to +85°C

Item		Symbol	Min.	Max.	Unit	Test Conditions
ETHERC(MII)	ET_TX_CLK cycle time	t_{Tcyc}	40	—	ns	—
	ET_TX_EN output delay time	t_{TENd}	1	20	ns	Figure 5.51
	ET_ETXD0 to ET_ETXD3 output delay time	t_{MTDd}	1	20	ns	
	ET_CRS setup time	t_{CRSs}	10	—	ns	
	ET_CRS hold time	t_{CRSh}	10	—	ns	
	ET_COL setup time	t_{COLs}	10	—	ns	Figure 5.52
	ET_COL hold time	t_{COLh}	10	—	ns	
	ET_RX_CLK cycle time	t_{TRcyc}	40	—	ns	—
	ET_RX_DV setup time	t_{RDVs}	10		ns	Figure 5.53
	ET_RX_DV hold time	t_{RDVh}	10	—	ns	
	ET_ERXD0 to ET_ERXD3 setup time	t_{MRDs}	10	—	ns	
	ET_ERXD0 to ET_ERXD3 hold time	t_{MRDh}	10	—	ns	
	ET_RX_ER setup time	t_{RERs}	10	—	ns	Figure 5.54
	ET_RX_ER hold time	t_{RESh}	10	—	ns	
	ET_MDIO setup time	t_{MDIOs}	10	—	ns	Figure 5.55
	ET_MDIO hold time	t_{MDIOh}	10	—	ns	
	ET_MDIO utput hold time	t_{MDIOdh}	5	—	ns	Figure 5.56
	ET_WOL output delay time	t_{WOLd}	1	20	ns	Figure 5.57

Note 1. RMII_TXD_EN, RMII_TXD1, RMII_TXD0
Note 2. RMII_CRS_DV, RMII_RXD1, RMII_RXD0, RMII_RX_ER
Note 3. The user program must make settings so that this stipulation is satisfied.

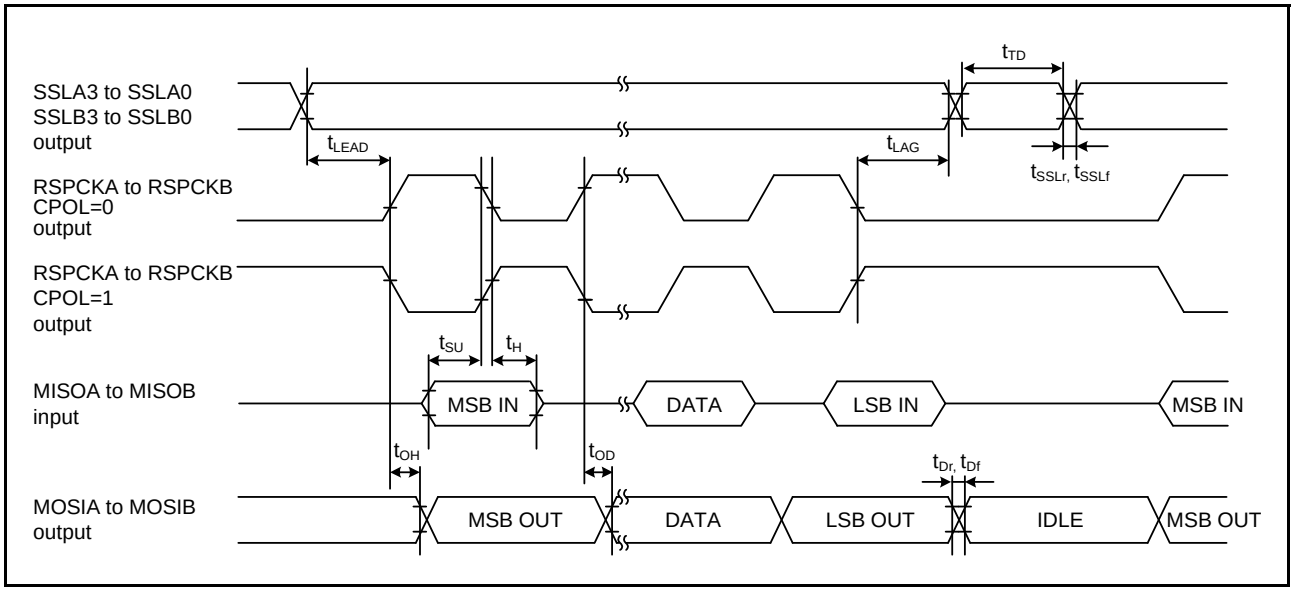


Figure 5.40 RSPI Timing (Master, CPHA = 1)

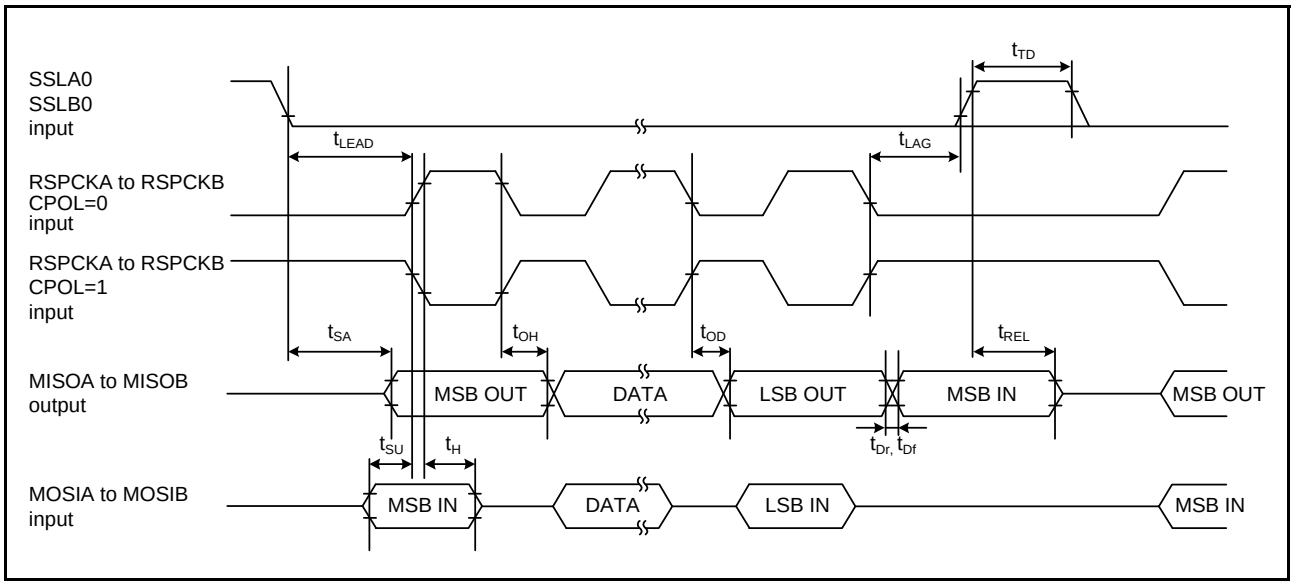
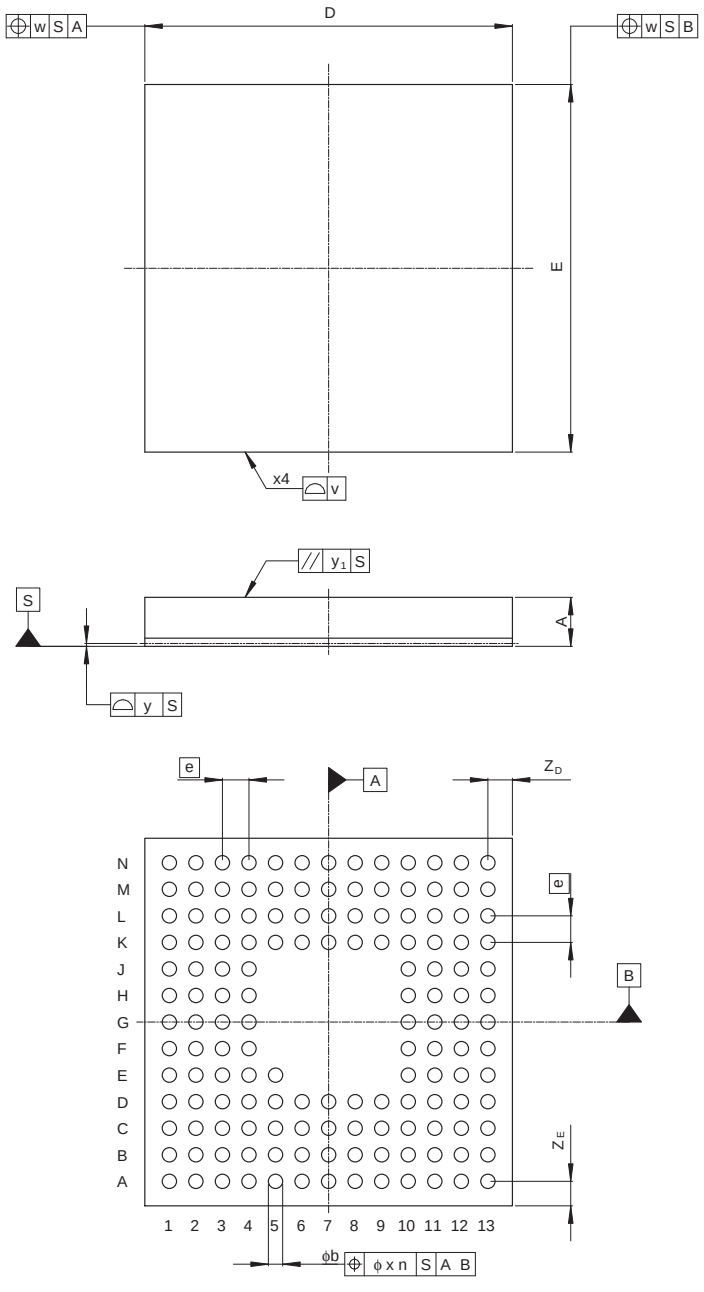


Figure 5.41 RSPI Timing (Slave, CPHA = 0)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA145-9x9-0.65	PTLG0145JB-A	-	0.15g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	9.0	—
E	—	9.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.2
A_1	—	—	—
e	—	0.65	—
b	0.30	0.35	0.40
x	—	—	0.08
y	—	—	0.1
y_1	—	—	0.20
S_D	—	—	—
S_E	—	—	—
Z_D	—	0.6	—
Z_E	—	0.6	—

Figure B 145-Pin TFLGA (PTLG0145JB-A) Package Dimensions