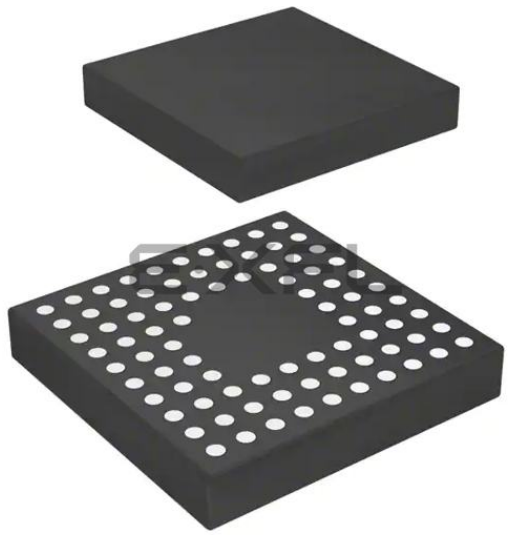
Renesas Electronics America Inc - R5F56216BDLD#U0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	58
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	85-TFLGA
Supplier Device Package	85-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f56216bdld-u0

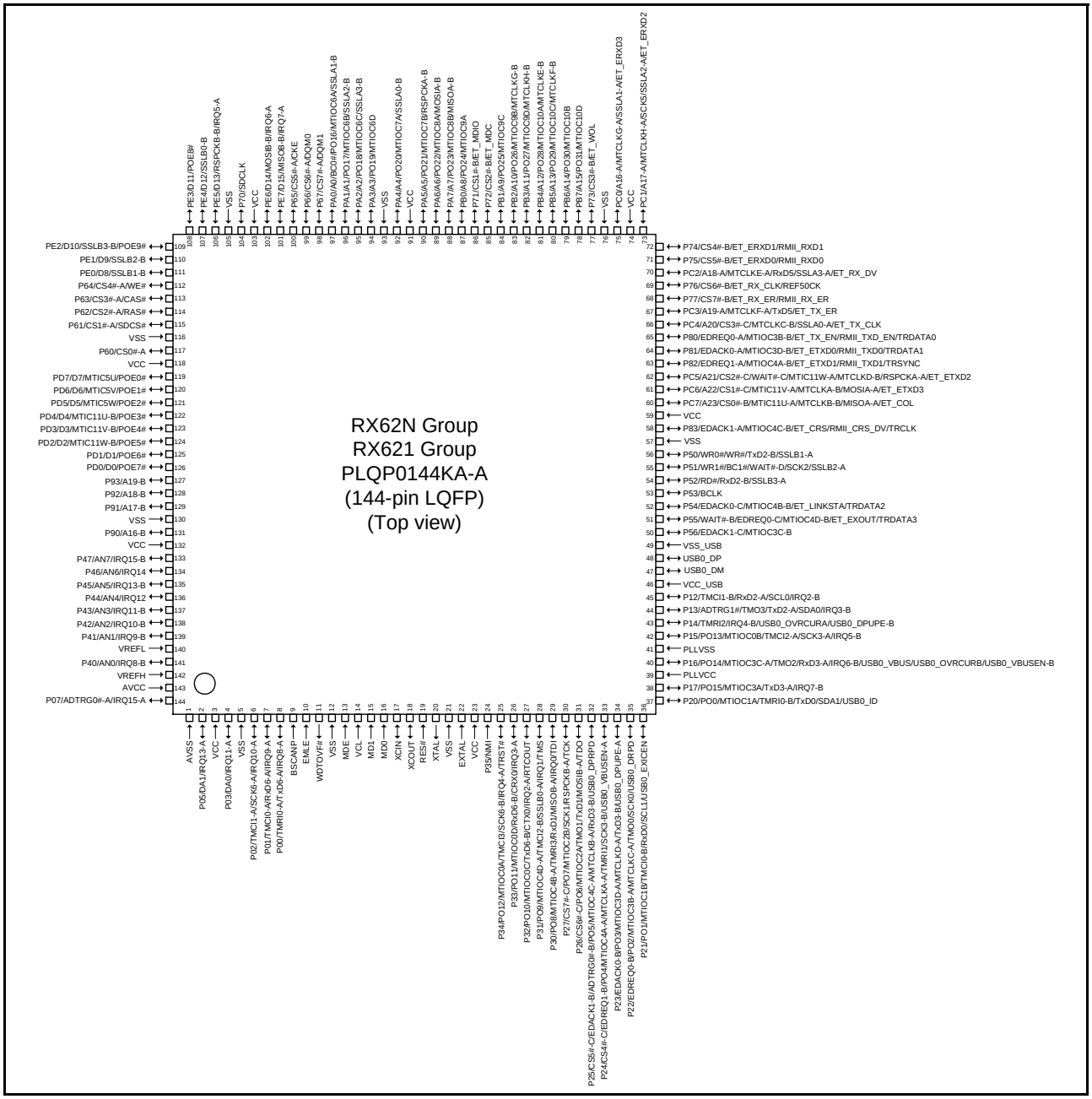


Figure 1.5 Pin Assignment of the 144-Pin LQFP

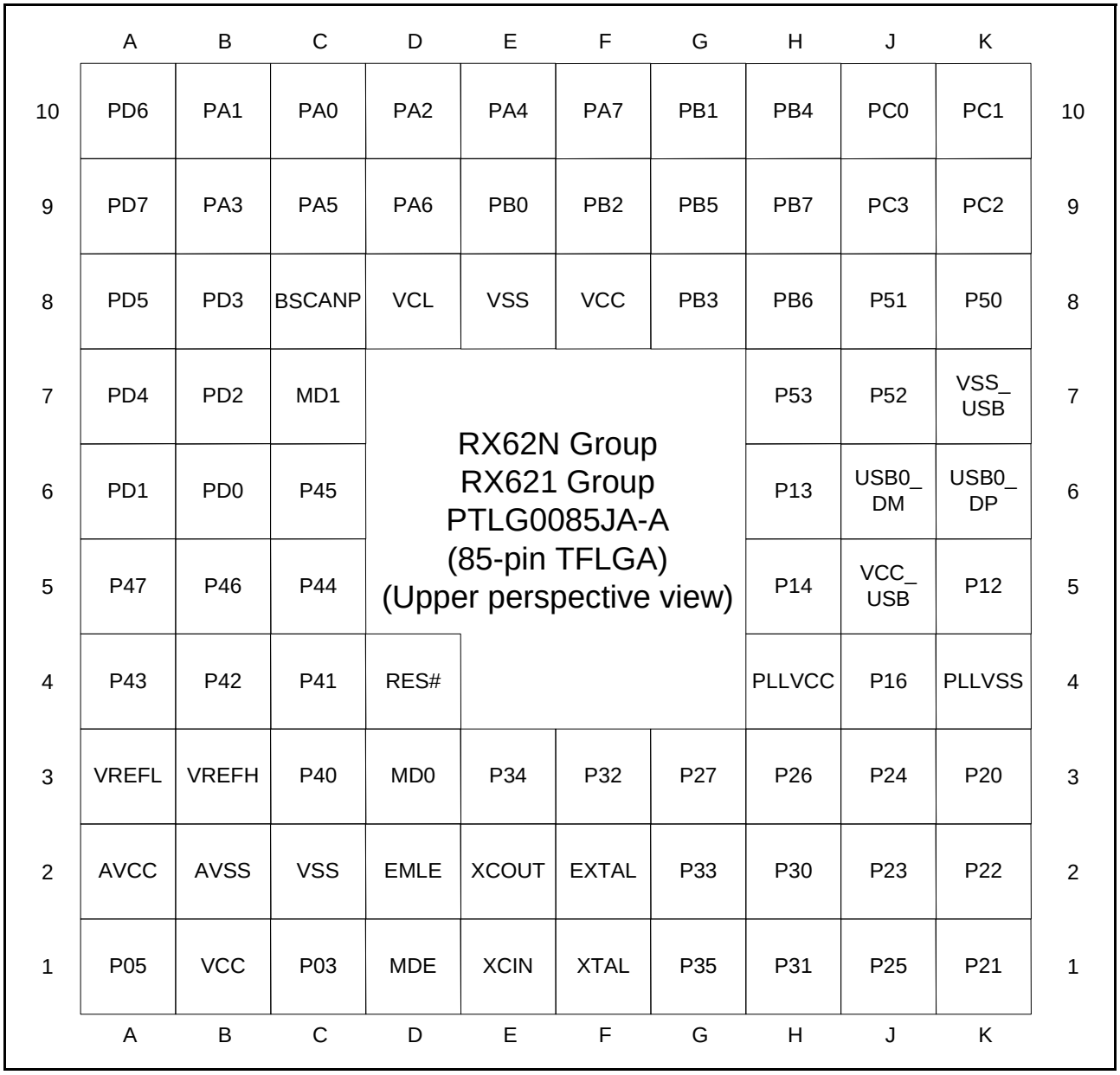


Figure 1.9 Pin Assignment of the 85-Pin TFLGA

Table 1.4 List of Pins and Pin Functions (176-Pin LFBGA) (3 / 6)

Pin No. 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	External Bus EXDMAC	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE, WDT)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
F15		PG5	D29					TRCLK
G1	VSS							
G2	MD1							
G3	MD0							
G4	MDE							
G12	VSS							
G13	VCC							
G14		PG6	D30					TRDATA2
G15		PA1	A1/DQM3			MTIOC6B/ PO17	SSLA2-B	
H1	XTAL							
H2		P35						NMI
H3	VCC							
H4	RES#							
H12		PG7	D31					TRDATA3
H13		PA2	A2			MTIOC6C/ PO18	SSLA3-B	
H14		PA4	A4			MTIOC7A/ PO20	SSLA0-B	
H15		PA3	A3			MTIOC6D/ PO19		
J1	EXTAL							
J2		P32				MTIOC0C/ PO10/ RTCOUT	CTX0/ TxD6-B	IRQ2-A
J3		PF3						TMS
J4		P34				MTIOC0A/ TMCI3-B/ PO12	SCK6-B	IRQ4-A
J12	VSS							
J13		PA5	A5			MTIOC7B/ PO21	RSPCKA-B	
J14		PA7	A7			MTIOC8B/ PO23	MISOA-B	
J15		PA6	A6			MTIOC8A/ PO22	MOSIA-B	
K1		P33				MTIOC0D/ PO11	CRX0/ RxD6-B	IRQ3-A
K2		P31			USB1_DPRPD	MTIOC4D-A/ TMCI2-B/ PO9	SSLB0-A	IRQ1-A
K3		PF0					TxD1-B	TDO
K4		PF4						TRST#
K12		PB1	A9			MTIOC9C/ PO25		
K13		P71	CS1#-B	ET_MDIO				
K14		P72	CS2#-B	ET_MDC				

Table 1.5 List of Pins and Pin Functions (145-Pin TFLGA) (2 / 5)

Pin No. 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	External Bus EXDMAC	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE, WDT)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
C10		P63	CS3#-A/ CAS#					
C11		PE5	D13				RSPCKB-B	IRQ5-A
C12		PE3	D11			POE8#		
C13	SDCLK	P70						
D1	EMLE							
D2	VCC							
D3		P02				TMCI1-A	SCK6-A	IRQ10-A
D4		P43						IRQ11-B/AN3
D5	VCC							
D6	VSS							
D7		P93	A19-B					
D8		PD4	D4			MTIC11U-B/ POE3#		
D9	VCC							
D10	VSS							
D11	VCC							
D12		PE7	D15				MISOB-B	IRQ7-A
D13		PE6	D14				MOSIB-B	IRQ6-A
E1	VCL							
E2	VSS							
E3		P00				TMRI0-A	TxD6-A	IRQ8-A
E4	BSCANP							
E5	(N.C)							
E10		P65	CS5#-A/ CKE					
E11		P67	CS7#-A/ DQM1					
E12		PA0	A0/BC0#			MTIOC6A/ PO16	SSLA1-B	
E13		P66	CS6#-A/ DQM0					
F1	XCIN							
F2	XCOUT							
F3						WDTOVF#		
F4	MDE							
F10		PA1	A1			MTIOC6B/ PO17	SSLA2-B	
F11		PA3	A3			MTIOC6D/ PO19		
F12	VCC							
F13		PA2	A2			MTIOC6C/ PO18	SSLA3-B	
G1	XTAL							
G2	VSS							

Table 1.5 List of Pins and Pin Functions (145-Pin TFLGA) (3 / 5)

Pin No. 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	External Bus EXDMAC	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE, WDT)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
G3	MD1							
G4	MD0							
G10	VSS							
G11		PA5	A5			MTIOC7B/ PO21	RSPCKA-B	
G12		PA6	A6			MTIOC8A/ PO22	MOSIA-B	
G13		PA4	A4			MTIOC7A/ PO20	SSLA0-B	
H1	EXTAL							
H2		P34				MTIOC0A/ TMCI3/ PO12	SCK6-B	IRQ4-A/ TRST#
H3	VCC							
H4	RES#							
H10		PB0	A8			MTIOC9A/ PO24		
H11		P71	CS1#-B	ET_MDIO				
H12		PB1	A9			MTIOC9C/ PO25		
H13		PA7	A7			MTIOC8B/ PO23	MISOA-B	
J1		P33				MTIOC0D/ PO11	CRX0/ RxD6-B	IRQ3-A
J2		P27	CS7#-C			MTIOC2B/ PO7	RSPCKB-A/ SCK1	TCK
J3		P35						NMI
J4		P32				MTIOC0C/ PO10/ RTCOUT	CTX0/ TxD6-B	IRQ2-A
J10		PB2	A10			MTIOC9B/ MTCLKG-B/ PO26		
J11		PB4	A12			MTIOC10A/ MTCLKE-B/ PO28		
J12		PB5	A13			MTIOC10C/ MTCLKF-B/ PO29		
J13		P72	CS2#-B	ET_MDC				
K1		P30				MTIOC4B-A/ TMRI3/ PO8	RxD1/ MISOB-A	IRQ0/ TDI
K2		P24	CS4#-C/ EDREQ1-B		USB0_VBUSEN-A	MTIOC4A-A/ MTCLKA-A/ TMRI1/PO4	SCK3-B	
K3		P31				MTIOC4D-A/ TMCI2-B/ PO9	SSLB0-A	IRQ1/ TMS

Table 1.6 List of Pins and Pin Functions (144-Pin LQFP) (2 / 5)

Pin No. 144-Pin LQFP	Power Supply Clock System Control	I/O Port	External Bus EXDMAC	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE, WDT)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
32		P25	CS5#-C/ EDACK1-B		USB0_DPRPD	MTIOC4C-A/ MTCLKB-A/ PO5	RxD3-B	ADTRG0#-B
33		P24	CS4#-C/ EDREQ1-B		USB0_VBUSEN-A	MTIOC4A-A/ MTCLKA-A/ TMRI1/PO4	SCK3-B	
34		P23	EDACK0-B		USB0_DPUPE-A	MTIOC3D-A/ MTCLKD-A/ PO3	TxD3-B	
35		P22	EDREQ0-B		USB0_DRPD	MTIOC3B-A/ MTCLKC-A/ TMO0/PO2	SCK0	
36		P21			USB0_EXICEN	MTIOC1B/ TMCI0-B/ PO1	SCL1/RxD0	
37		P20			USB0_ID	MTIOC1A/ TMRI0-B/ PO0	SDA1/ TxD0	
38		P17				MTIOC3A/ PO15	TxD3-A	IRQ7-B
39	PLLVCC							
40		P16			USB0_VBUS/ USB0_OVRCURB/ USB0_VBUSEN-B	MTIOC3C-A/ TMO2/ PO14	RxD3-A	IRQ6-B
41	PLLVSS							
42		P15				MTIOC0B/ TMCI2-A/ PO13	SCK3-A	IRQ5-B
43		P14			USB0_OVRCURA/ USB0_DPUPE-B	TMRI2		IRQ4-B
44		P13				TMO3	SDA0/ TxD2-A	IRQ3-B/ ADTRG1#
45		P12				TMCI1-B	SCL0/ RxD2-A	IRQ2-B
46	VCC_USB							
47					USB0_DM			
48					USB0_DP			
49	VSS_USB							
50		P56	EDACK1-C			MTIOC3C-B		
51		P55	WAIT#-B/ EDREQ0-C	ET_EXOUT		MTIOC4D-B		TRDATA3
52		P54	EDACK0-C	ET_LINKSTA		MTIOC4B-B		TRDATA2
53	BCLK	P53						
54		P52	RD#				SSLB3-A/ RxD2-B	

Table 1.7 List of Pins and Pin Functions (100-Pin LQFP) (3 / 4)

Pin No. 100-Pin LQFP	Power Supply Clock System Control	I/O Port	External Bus	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
53		PB7	A15	ET_CRS/ RMII_CRS_DV		MTIOC10D/ PO31		
54		PB6	A14	ET_ETXD1/ RMII_TXD1		MTIOC10B/ PO30		
55		PB5	A13	ET_ETXD0/ RMII_TXD0		MTIOC10C/ MTCLKF-B/ PO29		
56		PB4	A12	ET_TX_EN/ RMII_TXD_EN		MTIOC10A/ MTCLKE-B/ PO28		
57		PB3	A11	ET_RX_ER/ RMII_RX_ER		MTIOC9D/ MTCLKH-B/ PO27		
58		PB2	A10	ET_RX_CLK/ REF50CK		MTIOC9B/ MTCLKG-B/ PO26		
59		PB1	A9	ET_ERXD0/ RMII_RXD0		MTIOC9C/ PO25		
60	VCC							
61		PB0	A8	ET_ERXD1/ RMII_RXD1		MTIOC9A/ PO24		
62	VSS							
63		PA7	A7	ET_WOL		MTIOC8B/ PO23	MISOA-B	
64		PA6	A6	ET_EXOUT		MTIOC8A/ PO22	MOSIA-B	
65		PA5	A5	ET_LINKSTA		MTIOC7B/ PO21	RSPCKA-B	
66		PA4	A4	ET_MDC		MTIOC7A/ PO20	SSLA0-B	
67		PA3	A3	ET_MDIO		MTIOC6D/ PO19		
68		PA2	A2			MTIOC6C/ PO18	SSLA3-B	
69		PA1	A1			MTIOC6B/ PO17	SSLA2-B	
70		PA0	A0/BC0#			MTIOC6A/ PO16	SSLA1-B	
71		PE7	D15				MISOB-B	IRQ7
72		PE6	D14				MOSIB-B	IRQ6-A
73		PE5	D13				RSPCKB-B	IRQ5
74		PE4	D12				SSLB0-B	
75		PE3	D11			POE8#		
76		PE2	D10			POE9#	SSLB3-B	
77		PE1	D9				SSLB2-B	
78		PE0	D8				SSLB1-B	
79		PD7	D7			MTIC5U/ POE0#		

Table 1.7 List of Pins and Pin Functions (100-Pin LQFP) (4 / 4)

Pin No. 100-Pin LQFP	Power Supply Clock System Control	I/O Port	External Bus	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
80		PD6	D6			MTIC5V/ POE1#		
81		PD5	D5			MTIC5W/ POE2#		
82		PD4	D4			MTIC11U-B/ POE3#		
83		PD3	D3			MTIC11V-B/ POE4#		
84		PD2	D2			MTIC11W-B/ POE5#		
85		PD1	D1			POE6#		
86		PD0	D0			POE7#		
87		P47						IRQ15-B/AN7
88		P46						IRQ14/AN6
89		P45						IRQ13-B/AN5
90		P44						IRQ12/AN4
91		P43						IRQ11/AN3
92		P42						IRQ10/AN2
93		P41						IRQ9/AN1
94	VREFL							
95		P40						IRQ8/AN0
96	VREFH							
97	AVCC							
98		P07						IRQ15-A/ ADTRG0#-A
99	AVSS							
100		P05						DA1/IRQ13-A

Table 1.8 List of Pins and Pin Functions (85-Pin TFLGA) (1 / 3)

Pin No. 85-Pin TFLGA	Power Supply Clock System Control	I/O Port	External Bus	USB	Timers (MTU, TMR, PPG)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
A1		P05					DA1/ IRQ13-A
A2	AVCC						
A3	VREFL						
A4		P43					IRQ11-B/AN3
A5		P47					IRQ15/ AN7
A6		PD1	D1				
A7		PD4	D4		MTIC11U		
A8		PD5	D5		MTIC5W		
A9		PD7	D7		MTIC5U		
A10		PD6	D6		MTIC5V		
B1	VCC						
B2	AVSS						
B3	VREFH						
B4		P42					IRQ10/ AN2
B5		P46					IRQ14/ AN6
B6		PD0	D0				
B7		PD2	D2		MTIC11W		
B8		PD3	D3		MTIC11V		
B9		PA3	A3		MTIOC6D/PO19		
B10		PA1	A1		MTIOC6B/PO17	SSLA2	
C1		P03					IRQ11-A/DA0
C2	VSS						
C3		P40					IRQ8/ AN0
C4		P41					IRQ9/ AN1
C5		P44					IRQ12/ AN4
C6		P45					IRQ13-B/AN5
C7	MD1						
C8	BSCANP						
C9		PA5	A5		MTIOC7B/PO21	RSPCKA	
C10		PA0	A0		MTIOC6A/PO16	SSLA1	
D1	MDE						
D2	EMLE						
D3	MD0						
D4	RES#						

2. CPU

The RX CPU has sixteen general-purpose registers, nine control registers, and one accumulator used for DSP instructions.

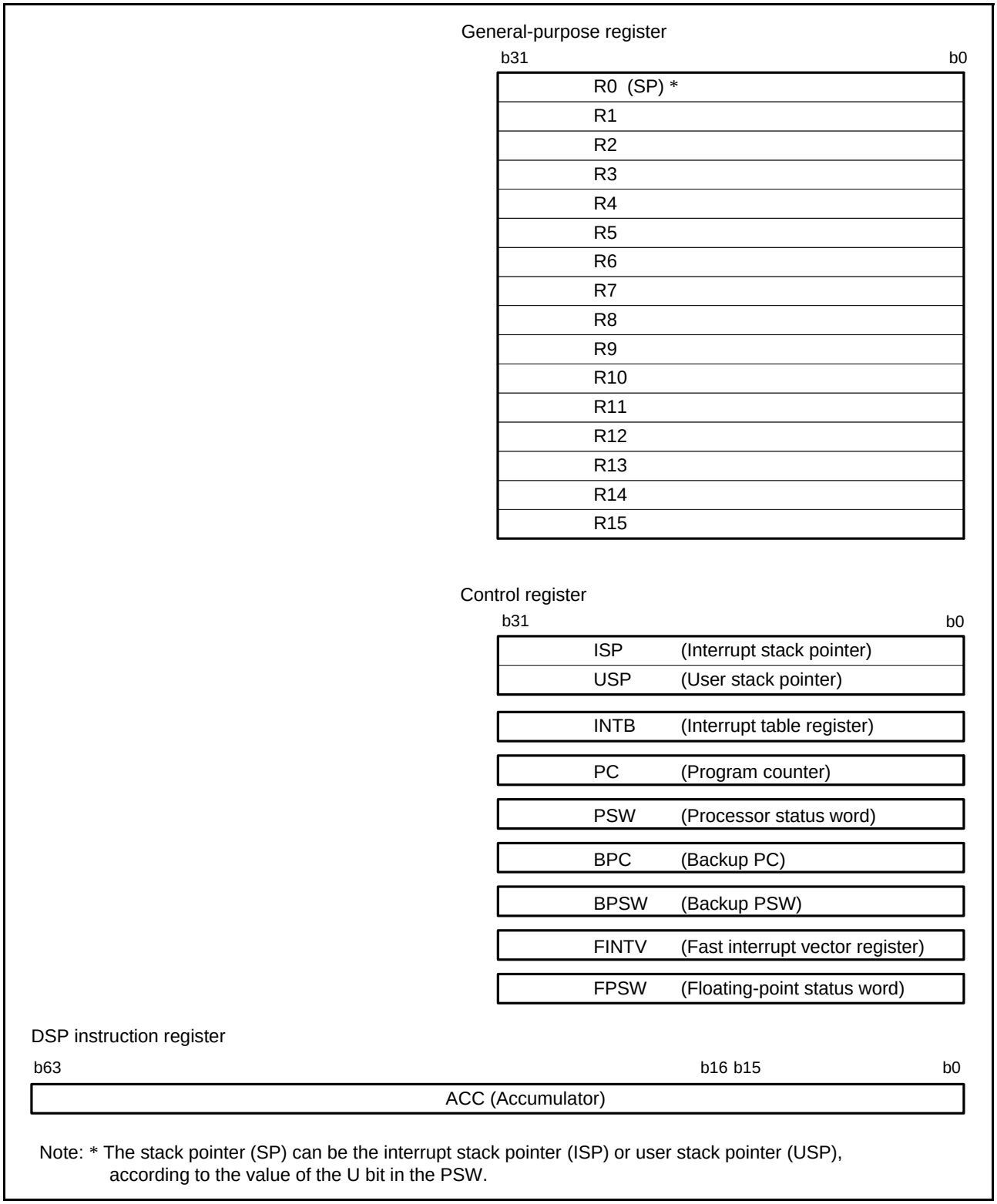


Figure 2.1 Register Set of the CPU

Table 4.1 List of I/O Registers (Address Order) (24 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 8A4Ah	MTU10	Timer A/D converter start request cycle set buffer register B	TADCOBRB	16	16	2 to 3 PCLK*8
0008 8A60h	MTUB	Timer waveform control register	TWCR	8	8	2 to 3 PCLK*8
0008 8A80h	MTUB	Timer start register	TSTR	8	8	2 to 3 PCLK*8
0008 8A81h	MTUB	MTUB Timer synchronous register	TSYR	8	8	2 to 3 PCLK*8
0008 8A84h	MTUB	MTUB Timer read/write enable register	TRWER	8	8	2 to 3 PCLK*8
0008 8B00h	MTU6	Timer control register	TCR	8	8	2 to 3 PCLK*8
0008 8B01h	MTU6	Timer mode register	TMDR	8	8	2 to 3 PCLK*8
0008 8B02h	MTU6	Timer I/O control register H	TIORH	8	8	2 to 3 PCLK*8
0008 8B03h	MTU6	Timer I/O control register L	TIORL	8	8	2 to 3 PCLK*8
0008 8B04h	MTU6	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK*8
0008 8B05h	MTU6	Timer status register	TSR	8	8	2 to 3 PCLK*8
0008 8B06h	MTU6	Timer counter	TCNT	16	16	2 to 3 PCLK*8
0008 8B08h	MTU6	Timer general register A	TGRA	16	16	2 to 3 PCLK*8
0008 8B0Ah	MTU6	Timer general register B	TGRB	16	16	2 to 3 PCLK*8
0008 8B0Ch	MTU6	Timer general register C	TGRC	16	16	2 to 3 PCLK*8
0008 8B0Eh	MTU6	Timer general register D	TGRD	16	16	2 to 3 PCLK*8
0008 8B20h	MTU6	Timer general register E	TGRE	16	16	2 to 3 PCLK*8
0008 8B22h	MTU6	Timer general register F	TGRF	16	16	2 to 3 PCLK*8
0008 8B24h	MTU6	Timer interrupt enable register 2	TIER2	8	8	2 to 3 PCLK*8
0008 8B26h	MTU6	Timer buffer operation transfer mode register	TBTM	8	8	2 to 3 PCLK*8
0008 8B80h	MTU7	Timer control register	TCR	8	8	2 to 3 PCLK*8
0008 8B81h	MTU7	Timer mode register	TMDR	8	8	2 to 3 PCLK*8
0008 8B82h	MTU7	Timer I/O control register	TIOR	8	8	2 to 3 PCLK*8
0008 8B84h	MTU7	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK*8
0008 8B85h	MTU7	Timer status register	TSR	8	8	2 to 3 PCLK*8
0008 8B86h	MTU7	Timer counter	TCNT	16	16	2 to 3 PCLK*8
0008 8B88h	MTU7	Timer general register A	TGRA	16	16	2 to 3 PCLK*8
0008 8B8Ah	MTU7	Timer general register B	TGRB	16	16	2 to 3 PCLK*8
0008 8B90h	MTU7	Timer input capture control register	TICCR	8	8	2 to 3 PCLK*8
0008 8C00h	MTU8	Timer control register	TCR	8	8	2 to 3 PCLK*8
0008 8C01h	MTU8	Timer mode register	TMDR	8	8	2 to 3 PCLK*8
0008 8C02h	MTU8	Timer I/O control register	TIOR	8	8	2 to 3 PCLK*8
0008 8C04h	MTU8	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK*8
0008 8C05h	MTU8	Timer status register	TSR	8	8	2 to 3 PCLK*8
0008 8C06h	MTU8	Timer counter	TCNT	16	16	2 to 3 PCLK*8
0008 8C08h	MTU8	Timer general register A	TGRA	16	16	2 to 3 PCLK*8
0008 8C0Ah	MTU8	Timer general register B	TGRB	16	16	2 to 3 PCLK*8
0008 8C80h	MTU11	Timer counter U	TCNTU	16	16	2 to 3 PCLK*8
0008 8C82h	MTU11	Timer general register U	TGRU	16	16	2 to 3 PCLK*8
0008 8C84h	MTU11	Timer control register U	TCRU	8	8	2 to 3 PCLK*8
0008 8C86h	MTU11	Timer I/O control register U	TIORU	8	8	2 to 3 PCLK*8
0008 8C90h	MTU11	Timer counter V	TCNTV	16	16	2 to 3 PCLK*8
0008 8C92h	MTU11	Timer general register V	TGRV	16	16	2 to 3 PCLK*8

Table 4.1 List of I/O Registers (Address Order) (30 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000A 0008h	USB0	Device state control register 0	DVSTCTR0	16	16	at least 9 PCLK*9
000A 0014h	USB0	CFIFO port register	CFIFO	16	8, 16	3 to 4 PCLK*8
000A 0018h	USB0	D0FIFO port register	D0FIFO	16	8, 16	3 to 4 PCLK*8
000A 001Ch	USB0	D1FIFO port register	D1FIFO	16	8, 16	3 to 4 PCLK*8
000A 0020h	USB0	CFIFO port select register	CFIFOSEL	16	16	3 to 4 PCLK*8
000A 0022h	USB0	CFIFO port control register	CFIFOCTR	16	16	3 to 4 PCLK*8
000A 0028h	USB0	D0FIFO port select register	D0FIFOSEL	16	16	3 to 4 PCLK*8
000A 002Ah	USB0	D0FIFO port control register	D0FIFOCTR	16	16	3 to 4 PCLK*8
000A 002Ch	USB0	D1FIFO port select register	D1FIFOSEL	16	16	3 to 4 PCLK*8
000A 002Eh	USB0	D1FIFO port control register	D1FIFOCTR	16	16	3 to 4 PCLK*8
000A 0030h	USB0	Interrupt enable register 0	INTENB0	16	16	at least 9 PCLK*9
000A 0032h	USB0	Interrupt enable register 1	INTENB1	16	16	at least 9 PCLK*9
000A 0036h	USB0	BRDY interrupt enable register	BRDYENB	16	16	at least 9 PCLK*9
000A 0038h	USB0	NRDY interrupt enable register	NRDYENB	16	16	at least 9 PCLK*9
000A 003Ah	USB0	BEMP interrupt enable register	BEMPENB	16	16	at least 9 PCLK*9
000A 003Ch	USB0	SOF output configuration register	SOFCFG	16	16	at least 9 PCLK*9
000A 0040h	USB0	Interrupt status register 0	INTSTS0	16	16	at least 9 PCLK*9
000A 0042h	USB0	Interrupt status register 1	INTSTS1	16	16	at least 9 PCLK*9
000A 0046h	USB0	BRDY interrupt enable register	BRDYSTS	16	16	at least 9 PCLK*9
000A 0048h	USB0	NRDY interrupt status register	NRDYSTS	16	16	at least 9 PCLK*9
000A 004Ah	USB0	BEMP interrupt status register	BEMPSTS	16	16	at least 9 PCLK*9
000A 004Ch	USB0	Frame number register	FRMNUM	16	16	at least 9 PCLK*9
000A 004Eh	USB0	Device state change register	DVCHGR	16	16	at least 9 PCLK*9
000A 0050h	USB0	USB address register	USBADDR	16	16	at least 9 PCLK*9
000A 0054h	USB0	USB request type register	USBREQ	16	16	at least 9 PCLK*9
000A 0056h	USB0	USB request value register	USBVAL	16	16	at least 9 PCLK*9
000A 0058h	USB0	USB request index register	USBINDX	16	16	at least 9 PCLK*9
000A 005Ah	USB0	USB request length register	USBLENG	16	16	at least 9 PCLK*9
000A 005Ch	USB0	DCP configuration register	DCPCFG	16	16	at least 9 PCLK*9
000A 005Eh	USB0	DCP maximum packet size register	DCPMAXP	16	16	at least 9 PCLK*9

Table 4.1 List of I/O Registers (Address Order) (32 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000A 00D4h	USB0	Device address 2 configuration register	DEVADD2	16	16	at least 9 PCLK*9
000A 00D6h	USB0	Device address 3 configuration register	DEVADD3	16	16	at least 9 PCLK*9
000A 00D8h	USB0	Device address 4 configuration register	DEVADD4	16	16	at least 9 PCLK*9
000A 00DAh	USB0	Device address 5 configuration register	DEVADD5	16	16	at least 9 PCLK*9
000A 0200h	USB1	System configuration control register	SYSCFG	16	16	3 to 4 PCLK*8
000A 0204h	USB1	System configuration status register 0	SYSSTS0	16	16	at least 9 PCLK*9
000A 0208h	USB1	Device state control register 0	DVSTCTR0	16	16	at least 9 PCLK*9
000A 0214h	USB1	CFIFO port register	CFIFO	16	8, 16	3 to 4 PCLK*8
000A 0218h	USB1	D0FIFO port register	D0FIFO	16	8, 16	3 to 4 PCLK*8
000A 021Ch	USB1	D1FIFO port register	D1FIFO	16	8, 16	3 to 4 PCLK*8
000A 0220h	USB1	CFIFO port select register	CFIFOSEL	16	16	3 to 4 PCLK*8
000A 0222h	USB1	CFIFO port control register	CFIFOCTR	16	16	3 to 4 PCLK*8
000A 0228h	USB1	D0FIFO port select register	D0FIFOSEL	16	16	3 to 4 PCLK*8
000A 022Ah	USB1	D0FIFO port control register	D0FIFOCTR	16	16	3 to 4 PCLK*8
000A 022Ch	USB1	D1FIFO port select register	D1FIFOSEL	16	16	3 to 4 PCLK*8
000A 022Eh	USB1	D1FIFO port control register	D1FIFOCTR	16	16	3 to 4 PCLK*8
000A 0230h	USB1	Interrupt enable register 0	INTENB0	16	16	at least 9 PCLK*9
000A 0232h	USB1	Interrupt enable register 1	INTENB1	16	16	at least 9 PCLK*9
000A 0236h	USB1	BRDY interrupt enable register	BRDYENB	16	16	at least 9 PCLK*9
000A 0238h	USB1	NRDY interrupt enable register	NRDYENB	16	16	at least 9 PCLK*9
000A 023Ah	USB1	BEMP interrupt enable register	BEMPENB	16	16	at least 9 PCLK*9
000A 023Ch	USB1	SOF output configuration register	SOFCFG	16	16	at least 9 PCLK*9
000A 0240h	USB1	Interrupt status register 0	INTSTS0	16	16	at least 9 PCLK*9
000A 0242h	USB1	Interrupt status register 1	INTSTS1	16	16	at least 9 PCLK*9
000A 0246h	USB1	BRDY interrupt status register	BRDYSTS	16	16	at least 9 PCLK*9
000A 0248h	USB1	NRDY interrupt status register	NRDYSTS	16	16	at least 9 PCLK*9
000A 024Ah	USB1	BEMP interrupt status register	BEMPSTS	16	16	at least 9 PCLK*9
000A 024Ch	USB1	Frame number register	FRMNUM	16	16	at least 9 PCLK*9
000A 024Eh	USB1	Device state change register	DVCHGR	16	16	at least 9 PCLK*9
000A 0250h	USB1	USB address register	USBADDR	16	16	at least 9 PCLK*9

Table 4.1 List of I/O Registers (Address Order) (34 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000A 029Ch	USB1	Pipe 4 transaction counter enable register	PIPE4TRE	16	16	at least 9 PCLK*9
000A 029Eh	USB1	Pipe 4 transaction counter register	PIPE4TRN	16	16	at least 9 PCLK*9
000A 02A0h	USB1	Pipe 5 transaction counter enable register	PIPE5TRE	16	16	at least 9 PCLK*9
000A 02A2h	USB1	Pipe 5 transaction counter register	PIPE5TRN	16	16	at least 9 PCLK*9
000A 02D0h	USB1	Device address 0 configuration register	DEVADD0	16	16	at least 9 PCLK*9
000A 02D2h	USB1	Device address 1 configuration register	DEVADD1	16	16	at least 9 PCLK*9
000A 02D4h	USB1	Device address 2 configuration register	DEVADD2	16	16	at least 9 PCLK*9
000A 02D6h	USB1	Device address 3 configuration register	DEVADD3	16	16	at least 9 PCLK*9
000A 02D8h	USB1	Device address 4 configuration register	DEVADD4	16	16	at least 9 PCLK*9
000A 02DAh	USB1	Device address 5 configuration register	DEVADD5	16	16	at least 9 PCLK*9
000A 0400h	USB	Deep standby USB transceiver control/ pin monitor register	DPUSR0R	32	32	1 to 2PCLK*8
000A 0404h	USB	Deep standby USB suspend/resume interrupt register	DPUSR1R	32	32	1 to 2PCLK*8
000C 0000h	EDMAC	EDMAC mode register	EDMR	32	32	4 to 5 ICLK
000C 0008h	EDMAC	EDMAC transmit request register	EDTRR	32	32	4 to 5 ICLK
000C 0010h	EDMAC	EDMAC receive request register	EDRRR	32	32	4 to 5 ICLK
000C 0018h	EDMAC	Transmit descriptor list start address register	TDLAR	32	32	4 to 5 ICLK
000C 0020h	EDMAC	Receive descriptor list start address register	RDLAR	32	32	4 to 5 ICLK
000C 0028h	EDMAC	ETHERC/EDMAC status register	EESR	32	32	4 to 5 ICLK
000C 0030h	EDMAC	ETHERC/EDMAC status interrupt permission register	EESIPR	32	32	4 to 5 ICLK
000C 0038h	EDMAC	Transmit/receive status copy enable register	TRSCER	32	32	4 to 5 ICLK
000C 0040h	EDMAC	Receive missed-frame counter register	RMFCR	32	32	4 to 5 ICLK
000C 0048h	EDMAC	Transmit FIFO threshold register	TFTR	32	32	4 to 5 ICLK
000C 0050h	EDMAC	FIFO depth register	FDR	32	32	4 to 5 ICLK
000C 0058h	EDMAC	Receiving method control register	RMCR	32	32	4 to 5 ICLK
000C 0064h	EDMAC	Transmit FIFO underrun counter	TFUCR	32	32	4 to 5 ICLK
000C 0068h	EDMAC	Receive FIFO overflow counter	RFOCR	32	32	4 to 5 ICLK
000C 006Ch	EDMAC	Independent output signal setting register	IOSR	32	32	4 to 5 ICLK
000C 0070h	EDMAC	Flow control start FIFO threshold setting register	FCFTR	32	32	4 to 5 ICLK
000C 0078h	EDMAC	Receive data padding insert register	RPADIR	32	32	4 to 5 ICLK
000C 007Ch	EDMAC	Transmit interrupt setting register	TRIMD	32	32	4 to 5 ICLK
000C 00C8h	EDMAC	Receive buffer write address register	RBWAR	32	32	4 to 5 ICLK
000C 00CCh	EDMAC	Receive descriptor fetch address register	RDFAR	32	32	4 to 5 ICLK

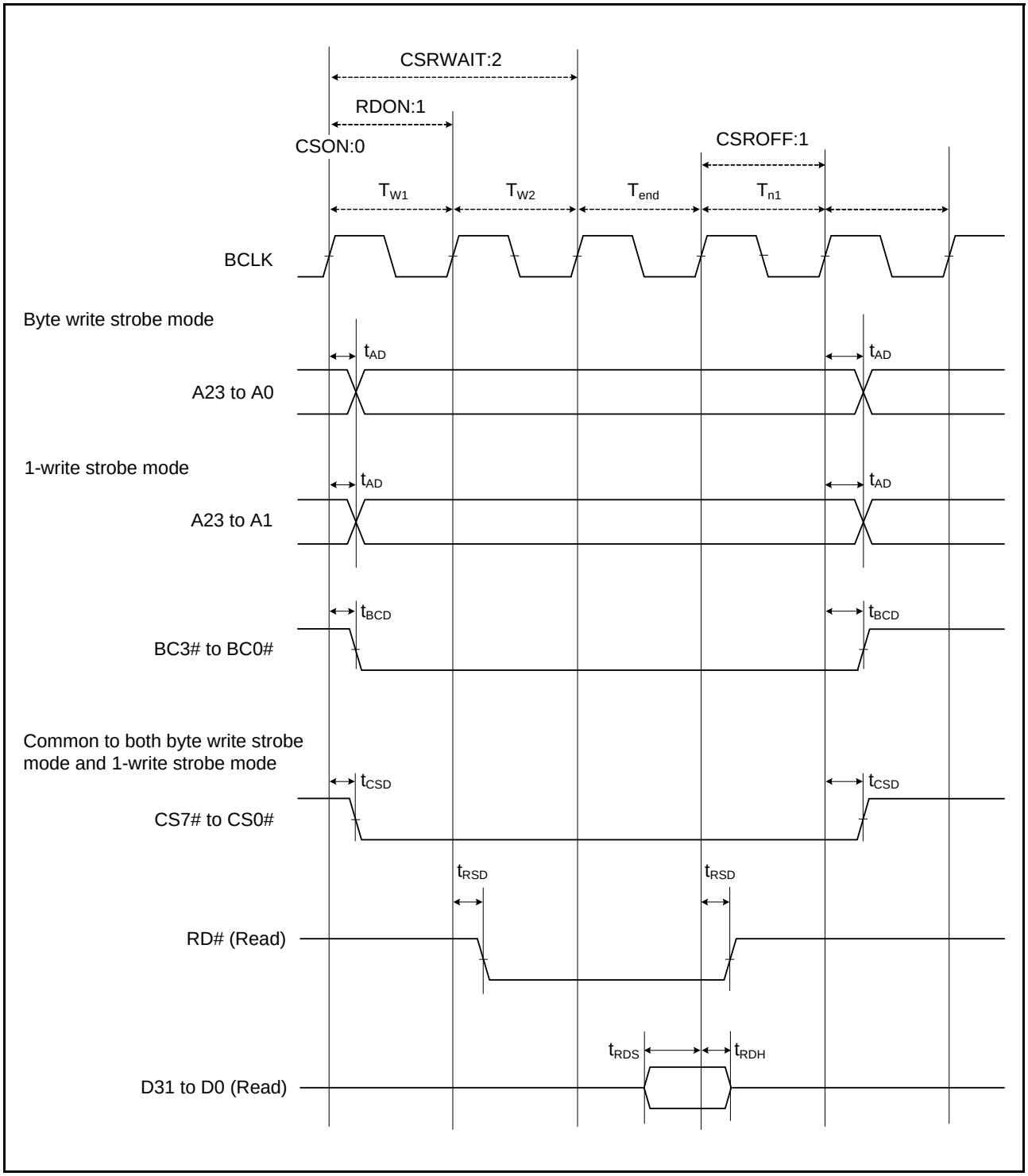


Figure 5.10 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)

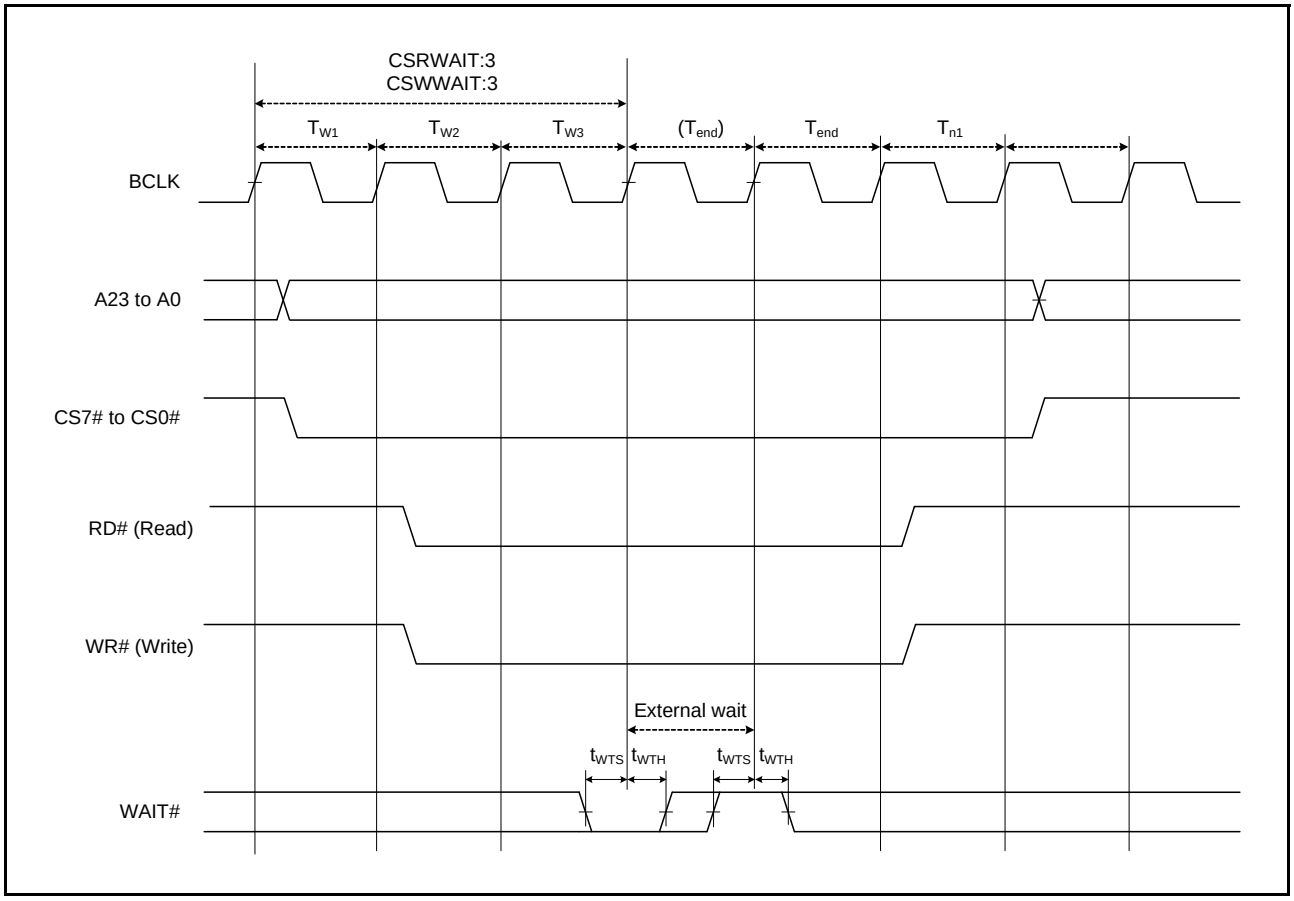


Figure 5.14 External Bus Timing/External Wait Control

5.3.5 Timing of On-Chip Peripheral Modules

Table 5.13 Timing of On-Chip Peripheral Modules (1)

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
PCLK = 8 to 50 MHz
T_a = -40 to +85°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
I/O ports	Output data delay time		t_{PWD}	—	40	ns	Figure 5.25
	Input data setup time		t_{PRS}	25	—	ns	
	Input data hold time		t_{PRH}	25	—	ns	
MTU2	Output compare output delay time		t_{TOCD}	—	40	ns	Figure 5.26
	Input capture input setup time		t_{TICS}	20	—	ns	
	Input capture input pulse width (single-edge setting)		t_{TICW}	1.5 × t_{Pcyc}	—	ns	
	Input capture input pulse width (both-edge setting)		t_{TICW}	2.5 × t_{Pcyc}	—	ns	
	Timer input setup time		t_{TCKS}	20	—	ns	Figure 5.27
	Timer clock pulse width (single-edge setting)		$t_{TCKWH/L}$	1.5 × t_{Pcyc}	—	ns	
	Timer clock pulse width (both-edge setting)		$t_{TCKWH/L}$	2.5 × t_{Pcyc}	—	ns	
	Timer clock pulse width (phase counting mode)		$t_{TCKWH/L}$	2.5 × t_{Pcyc}	—	ns	
POE2	POE# input setup time		t_{POES}	50	—	ns	Figure 5.28
	POE# input pulse width		t_{POEW}	1.5 × t_{Pcyc}	—	ns	
PPG	Pulse output delay time		t_{POD}	—	40	ns	Figure 5.29
8-bit timer	Timer output delay time		t_{TMOD}	—	40	ns	Figure 5.30
	Timer reset input setup time		t_{TMRS}	25	—	ns	Figure 5.31
	Timer clock input setup time		t_{TMCS}	25	—	ns	Figure 5.32
	Timer clock pulse width	Single-edge setting	t_{TMCWH}	1.5 × t_{Pcyc}	—	ns	
		Both-edge setting	t_{TMCWL}	2.5 × t_{Pcyc}	—	ns	
WDT	Overflow output delay time		t_{WOVD}	—	40	ns	Figure 5.33

Table 5.14 Timing of On-Chip Peripheral Modules (3)

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
PCLK = 8 to 50 MHz
T_a = -40 to +85°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
CAN	Transmit data delay time		t_{CTXD}	—	40.0	ns	Figure 5.37
	Receive data setup time		t_{CRXS}	40.0	—	ns	
	Receive data hold time		t_{CRXH}	40.0	—	ns	
RSPI	RSPCK clock cycle	Master	t_{SPcyc}	2	4096	t_{Pcyc} *1	Figure 5.38
		Slave		8	4096		
	RSPCK clock high pulse width	Master	t_{SPCKWH}	$(t_{SPcyc}-t_{SPCKR}-t_{SPCKF})$ / 2-3	—	ns	
		Slave		$(t_{SPcyc}-t_{SPCKR}-t_{SPCKF})$ / 2	—		
	RSPCK clock low pulse width	Master	t_{SPCKWL}	$(t_{SPcyc}-t_{SPCKR}-t_{SPCKF})$ / 2-3	—	ns	
		Slave		$(t_{SPcyc}-t_{SPCKR}-t_{SPCKF})$ / 2	—		
	RSPCK clock rise/fall time	Output [176-pin LFBGA/ 145-pin TFLGA/ 144-pin LQFP]	t_{SPCKr}, t_{SPCKf}	—	5	ns	
		Output [100-pin LQFP/ 85-pin TFLGA]		—	10		
		Input		—	1	µs	

Note 1. tPcyc: PCLK cycle

Table 5.15 Timing of On-Chip Peripheral Modules (5)

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
PCLK = 8 to 50 MHz
T_a = -40 to +85°C

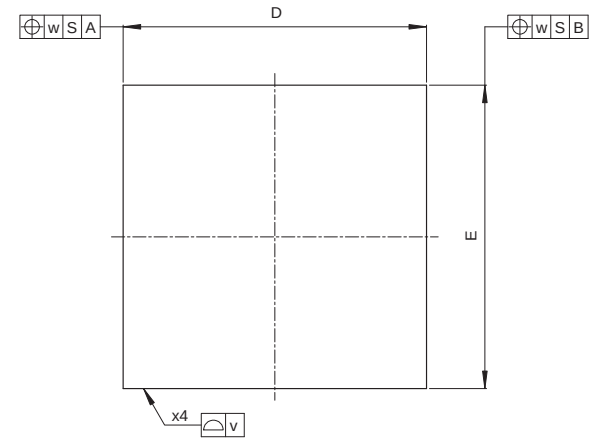
Item			Symbol	Min.	Max.	Unit	Test Conditions
RSPI	Data output hold time	Master	t_{OH}	0	—	ns	Figure 5.39 to Figure 5.42
		Slave		0	—		
	Successive transmission delay time	Master	t_{TD}	$t_{SPcyc}+2 \times t_{Pcyc}$	$8 \times t_{SPcyc}+2 \times t_{Pcyc}$	ns	
		Slave		$4 \times t_{Pcyc}$	—		
	MOSI, MISO rise/fall time	Output [176-pin LFBGA/ 145-pin TFLGA/ 144-pin LQFP]	t_{Dr}, t_{Df}	—	5	ns	
		Output [100-pin LQFP/ 85-pin TFLGA]		—	10		
		Input		—	1	µs	
	SSL rise/fall time	Output [176-pin LFBGA 145-pin TFLGA 144-pin LQFP]	t_{SSLr}, t_{SSLf}	—	5	ns	
		Output [100-pin LQFP/ 85-pin TFLGA]		—	10		
		Input		—	1	µs	
	Slave access time		t_{SA}	—	4	t_{Pcyc}	Figure 5.41 and Figure 5.42
	Slave output release time		t_{REL}	—	3	t_{Pcyc}	

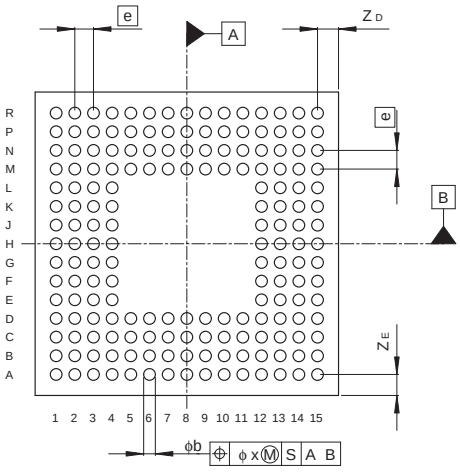
Note 1. tPcyc: PCLK cycle

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in "Packages" on Renesas Electronics Corp website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFBGA176-13x13-0.80	PLBG0176GA-A	BP-176/BP-176V	0.45g





Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	13.0	—
E	—	13.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.40
A_1	0.35	0.40	0.45
e	—	0.80	—
b	0.45	0.50	0.55
x	—	—	0.08
y	—	—	0.10
y_1	—	—	0.2
S_D	—	—	—
S_E	—	—	—
Z_D	—	0.90	—
Z_E	—	0.90	—

Figure A 176-Pin LFBGA (PLBG0176GA-A) Package Dimensions