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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I ² C, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	103
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10/12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	145-TFLGA
Supplier Device Package	145-TFLGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f56216bdle-u0

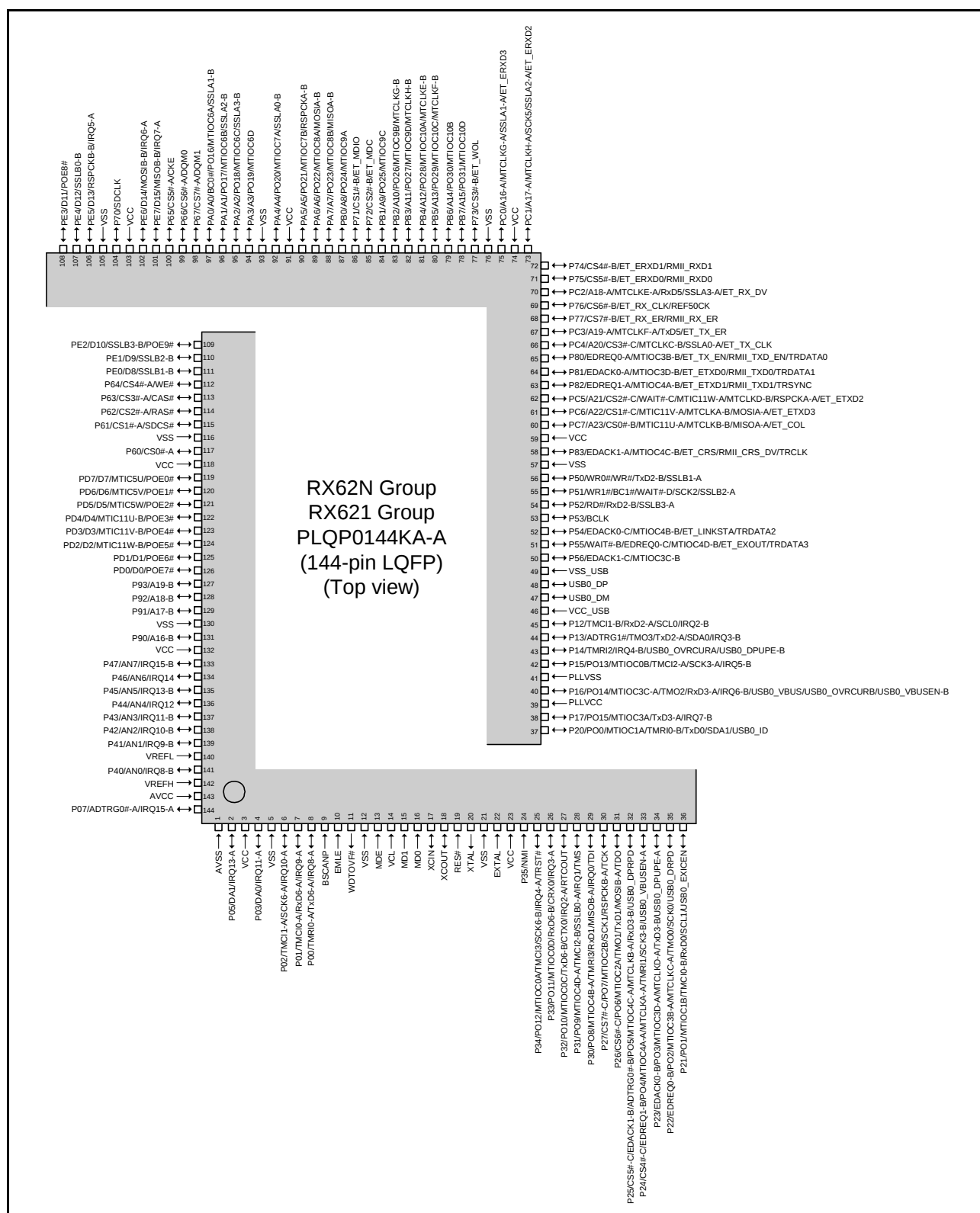


Figure 1.6 Pin Assignment of the 144-Pin LQFP (Assistance Diagram)

Table 1.5 List of Pins and Pin Functions (145-Pin TFLGA) (2 / 5)

Pin No.	Power Supply					Timers	Communi-	
145-Pin TFLGA	Clock System Control	I/O Port	External Bus EXDMAC	ETHERC EDMAC	USB	(MTU, TMR, PPG, POE, WDT)	cation (SCI, CAN, RSPI, RIIC)	Others
C10		P63	CS3#-A/ CAS#					
C11		PE5	D13				RSPCKB-B	IRQ5-A
C12		PE3	D11			POE8#		
C13	SDCLK	P70						
D1	EMLE							
D2	VCC							
D3		P02				TMCI1-A	SCK6-A	IRQ10-A
D4		P43						IRQ11-B/AN3
D5	VCC							
D6	VSS							
D7		P93	A19-B					
D8		PD4	D4			MTIC11U-B/ POE3#		
D9	VCC							
D10	VSS							
D11	VCC							
D12		PE7	D15				MISOB-B	IRQ7-A
D13		PE6	D14				MOSIB-B	IRQ6-A
E1	VCL							
E2	VSS							
E3		P00				TMRI0-A	TxD6-A	IRQ8-A
E4	BSCANP							
E5	(N.C)							
E10		P65	CS5#-A/ CKE					
E11		P67	CS7#-A/ DQM1					
E12		PA0	A0/BC0#			MTIOC6A/ PO16	SSLA1-B	
E13		P66	CS6#-A/ DQM0					
F1	XCIN							
F2	XCOUT							
F3						WDTOVF#		
F4	MDE							
F10		PA1	A1			MTIOC6B/ PO17	SSLA2-B	
F11		PA3	A3			MTIOC6D/ PO19		
F12	VCC							
F13		PA2	A2			MTIOC6C/ PO18	SSLA3-B	
G1	XTAL							
G2	VSS							

Table 1.7 List of Pins and Pin Functions (100-Pin LQFP) (1 / 4)

Pin No.	Power Supply								
100-Pin LQFP	Clock System Control	I/O Port	External Bus	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE)	Communication (SCI, CAN, RSPI, RIIC)	Others	
1	VCC								
2	EMLE								
3	VSS								
4	MDE								
5	VCL								
6	MD1								
7	MD0								
8	XCIN								
9	XCOUT								
10	RES#								
11	XTAL								
12	VSS								
13	EXTAL								
14	VCC								
15		P35							NMI
16		P34				MTIOC0A/ TMCI3/ PO12	SCK6	IRQ4-A/ TRST#	
17		P33				MTIOC0D/ PO11	CRX0/ RxD6	IRQ3-A	
18		P32				MTIOC0C/ PO10/ RTCOUT	CTX0/ TxD6	IRQ2-A	
19		P31				MTIOC4D- A/ TMCI2/ PO9	SSLB0-A	IRQ1/ TMS	
20		P30				MTIOC4B- A/ TMRI3/ PO8	RxD1/ MISOB-A	IRQ0/ TDI	
21		P27	CS7#			MTIOC2B/ PO7	RSPCKB- A/ SCK1	TCK	
22		P26	CS6#			MTIOC2A/ TMO1/ PO6	MOSIB-A/ TxD1	TDO	
23		P25	CS5#		USB0_DPRPD	MTIOC4C/ MTCLKB-A/ PO5	RxD3	ADTRG0#-B	
24		P24	CS4#		USB0_VBUSE N-A	MTIOC4A/ MTCLKA-A/ TMRI1/PO4	SCK3		
25		P23			USB0_DPUPE- A	MTIOC3D/ MTCLKD-A/ PO3	TxD3		
26		P22			USB0_DRPD	MTIOC3B/ MTCLKC-A/ TMO0/PO2	SCK0		

Table 1.7 List of Pins and Pin Functions (100-Pin LQFP) (4 / 4)

Pin No.	Power Supply Clock System Control	I/O Port	External Bus	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE)	Communi- cation (SCI, CAN, RSPI, RIIC)	Others
80		PD6	D6			MTIC5V/ POE1#		
81		PD5	D5			MTIC5W/ POE2#		
82		PD4	D4			MTIC11U-B/ POE3#		
83		PD3	D3			MTIC11V-B/ POE4#		
84		PD2	D2			MTIC11W- B/ POE5#		
85		PD1	D1			POE6#		
86		PD0	D0			POE7#		
87		P47						IRQ15-B/AN7
88		P46						IRQ14/AN6
89		P45						IRQ13-B/AN5
90		P44						IRQ12/AN4
91		P43						IRQ11/AN3
92		P42						IRQ10/AN2
93		P41						IRQ9/AN1
94	VREFL							
95		P40						IRQ8/AN0
96	VREFH							
97	AVCC							
98		P07						IRQ15-A/ ADTRG0#-A
99	AVSS							
100		P05						DA1/IRQ13-A

2. CPU

The RX CPU has sixteen general-purpose registers, nine control registers, and one accumulator used for DSP instructions.

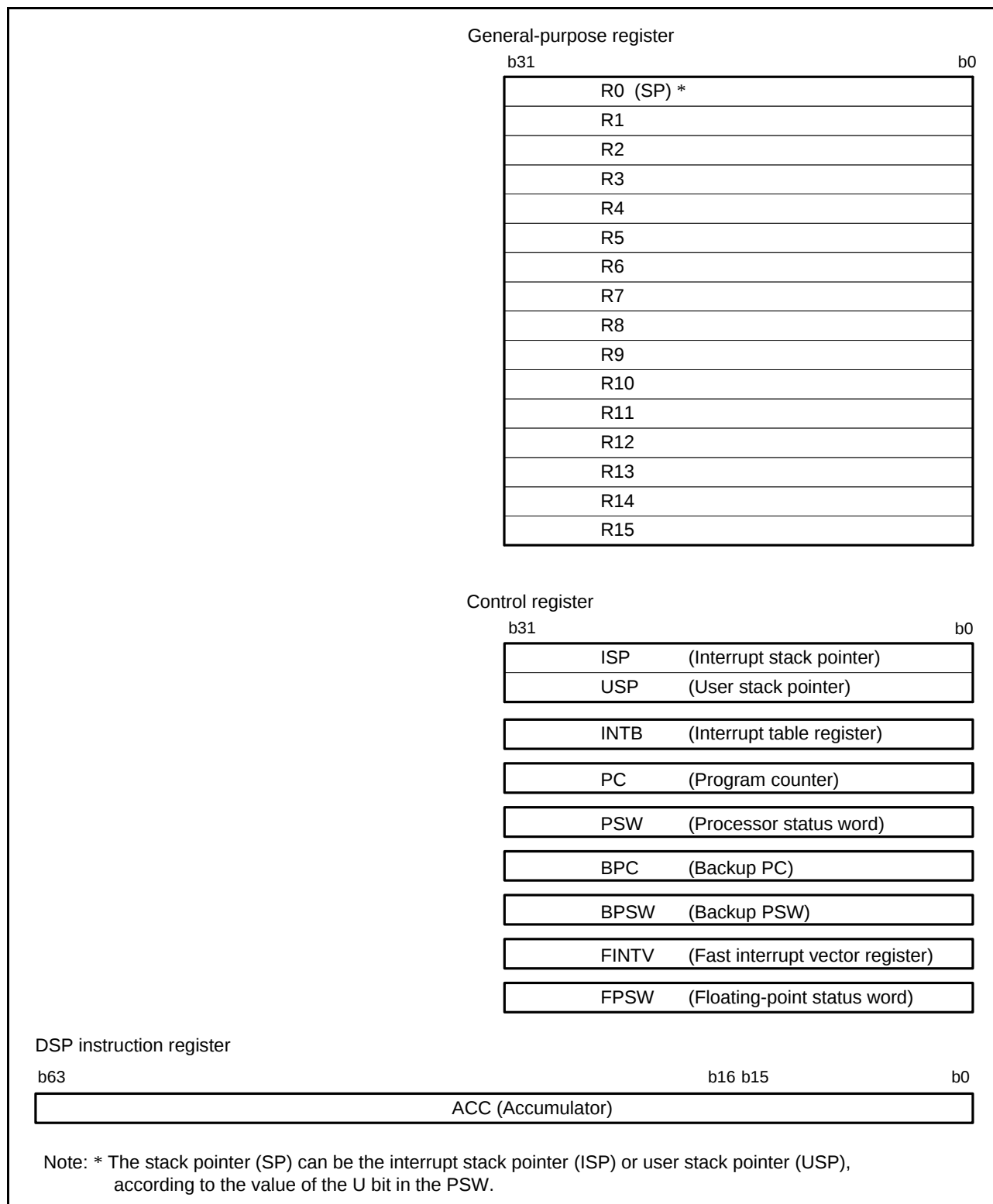


Figure 2.1 Register Set of the CPU

(9) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.

Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively.

Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

Table 4.1 List of I/O Registers (Address Order) (8 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 70B9h	ICU	Interrupt request register 185	IR185	8	8	2 ICLK
0008 70C6h	ICU	Interrupt request register 198	IR198	8	8	2 ICLK
0008 70C7h	ICU	Interrupt request register 199	IR199	8	8	2 ICLK
0008 70C8h	ICU	Interrupt request register 200	IR200	8	8	2 ICLK
0008 70C9h	ICU	Interrupt request register 201	IR201	8	8	2 ICLK
0008 70CAh	ICU	Interrupt request register 202	IR202	8	8	2 ICLK
0008 70CBh	ICU	Interrupt request register 203	IR203	8	8	2 ICLK
0008 70D6h	ICU	Interrupt request register 214	IR214	8	8	2 ICLK
0008 70D7h	ICU	Interrupt request register 215	IR215	8	8	2 ICLK
0008 70D8h	ICU	Interrupt request register 216	IR216	8	8	2 ICLK
0008 70D9h	ICU	Interrupt request register 217	IR217	8	8	2 ICLK
0008 70DAh	ICU	Interrupt request register 218	IR218	8	8	2 ICLK
0008 70DBh	ICU	Interrupt request register 219	IR219	8	8	2 ICLK
0008 70DCh	ICU	Interrupt request register 220	IR220	8	8	2 ICLK
0008 70DDh	ICU	Interrupt request register 221	IR221	8	8	2 ICLK
0008 70DEh	ICU	Interrupt request register 222	IR222	8	8	2 ICLK
0008 70DFh	ICU	Interrupt request register 223	IR223	8	8	2 ICLK
0008 70E0h	ICU	Interrupt request register 224	IR224	8	8	2 ICLK
0008 70E1h	ICU	Interrupt request register 225	IR225	8	8	2 ICLK
0008 70E2h	ICU	Interrupt request register 226	IR226	8	8	2 ICLK
0008 70E3h	ICU	Interrupt request register 227	IR227	8	8	2 ICLK
0008 70E4h	ICU	Interrupt request register 228	IR228	8	8	2 ICLK
0008 70E5h	ICU	Interrupt request register 229	IR229	8	8	2 ICLK
0008 70EAh	ICU	Interrupt request register 234	IR234	8	8	2 ICLK
0008 70EBh	ICU	Interrupt request register 235	IR235	8	8	2 ICLK
0008 70ECh	ICU	Interrupt request register 236	IR236	8	8	2 ICLK
0008 70EDh	ICU	Interrupt request register 237	IR237	8	8	2 ICLK
0008 70EEh	ICU	Interrupt request register 238	IR238	8	8	2 ICLK
0008 70EFh	ICU	Interrupt request register 239	IR239	8	8	2 ICLK
0008 70F0h	ICU	Interrupt request register 240	IR240	8	8	2 ICLK
0008 70F1h	ICU	Interrupt request register 241	IR241	8	8	2 ICLK
0008 70F6h	ICU	Interrupt request register 246	IR246	8	8	2 ICLK
0008 70F7h	ICU	Interrupt request register 247	IR247	8	8	2 ICLK
0008 70F8h	ICU	Interrupt request register 248	IR248	8	8	2 ICLK
0008 70F9h	ICU	Interrupt request register 249	IR249	8	8	2 ICLK
0008 70FAh	ICU	Interrupt request register 250	IR250	8	8	2 ICLK
0008 70FBh	ICU	Interrupt request register 251	IR251	8	8	2 ICLK
0008 70FCh	ICU	Interrupt request register 252	IR252	8	8	2 ICLK
0008 70FDh	ICU	Interrupt request register 253	IR253	8	8	2 ICLK
0008 711Bh	ICU	DTC activation enable register 027	DTCER027	8	8	2 ICLK
0008 711Ch	ICU	DTC activation enable register 028	DTCER028	8	8	2 ICLK
0008 711Dh	ICU	DTC activation enable register 029	DTCER029	8	8	2 ICLK
0008 711Eh	ICU	DTC activation enable register 030	DTCER030	8	8	2 ICLK
0008 711Fh	ICU	DTC activation enable register 031	DTCER031	8	8	2 ICLK
0008 7124h	ICU	DTC activation enable register 036	DTCER036	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (9 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 7125h	ICU	DTC activation enable register 037	DTCER037	8	8	2 ICLK
0008 7128h	ICU	DTC activation enable register 040	DTCER040	8	8	2 ICLK
0008 7129h	ICU	DTC activation enable register 041	DTCER041	8	8	2 ICLK
0008 712Dh	ICU	DTC activation enable register 045	DTCER045	8	8	2 ICLK
0008 712Eh	ICU	DTC activation enable register 046	DTCER046	8	8	2 ICLK
0008 7131h	ICU	DTC activation enable register 049	DTCER049	8	8	2 ICLK
0008 7132h	ICU	DTC activation enable register 050	DTCER050	8	8	2 ICLK
0008 7140h	ICU	DTC activation enable register 064	DTCER064	8	8	2 ICLK
0008 7141h	ICU	DTC activation enable register 065	DTCER065	8	8	2 ICLK
0008 7142h	ICU	DTC activation enable register 066	DTCER066	8	8	2 ICLK
0008 7143h	ICU	DTC activation enable register 067	DTCER067	8	8	2 ICLK
0008 7144h	ICU	DTC activation enable register 068	DTCER068	8	8	2 ICLK
0008 7145h	ICU	DTC activation enable register 069	DTCER069	8	8	2 ICLK
0008 7146h	ICU	DTC activation enable register 070	DTCER070	8	8	2 ICLK
0008 7147h	ICU	DTC activation enable register 071	DTCER071	8	8	2 ICLK
0008 7148h	ICU	DTC activation enable register 072	DTCER072	8	8	2 ICLK
0008 7149h	ICU	DTC activation enable register 073	DTCER073	8	8	2 ICLK
0008 714Ah	ICU	DTC activation enable register 074	DTCER074	8	8	2 ICLK
0008 714Bh	ICU	DTC activation enable register 075	DTCER075	8	8	2 ICLK
0008 714Ch	ICU	DTC activation enable register 076	DTCER076	8	8	2 ICLK
0008 714Dh	ICU	DTC activation enable register 077	DTCER077	8	8	2 ICLK
0008 714Eh	ICU	DTC activation enable register 078	DTCER078	8	8	2 ICLK
0008 714Fh	ICU	DTC activation enable register 079	DTCER079	8	8	2 ICLK
0008 7162h	ICU	DTC activation enable register 098	DTCER098	8	8	2 ICLK
0008 7163h	ICU	DTC activation enable register 099	DTCER099	8	8	2 ICLK
0008 7166h	ICU	DTC activation enable register 102	DTCER102	8	8	2 ICLK
0008 7172h	ICU	DTC activation enable register 114	DTCER114	8	8	2 ICLK
0008 7173h	ICU	DTC activation enable register 115	DTCER115	8	8	2 ICLK
0008 7174h	ICU	DTC activation enable register 116	DTCER116	8	8	2 ICLK
0008 7175h	ICU	DTC activation enable register 117	DTCER117	8	8	2 ICLK
0008 7179h	ICU	DTC activation enable register 121	DTCER121	8	8	2 ICLK
0008 717Ah	ICU	DTC activation enable register 122	DTCER122	8	8	2 ICLK
0008 717Dh	ICU	DTC activation enable register 125	DTCER125	8	8	2 ICLK
0008 717Eh	ICU	DTC activation enable register 126	DTCER126	8	8	2 ICLK
0008 7181h	ICU	DTC activation enable register 129	DTCER129	8	8	2 ICLK
0008 7182h	ICU	DTC activation enable register 130	DTCER130	8	8	2 ICLK
0008 7183h	ICU	DTC activation enable register 131	DTCER131	8	8	2 ICLK
0008 7184h	ICU	DTC activation enable register 132	DTCER132	8	8	2 ICLK
0008 7186h	ICU	DTC activation enable register 134	DTCER134	8	8	2 ICLK
0008 7187h	ICU	DTC activation enable register 135	DTCER135	8	8	2 ICLK
0008 7188h	ICU	DTC activation enable register 136	DTCER136	8	8	2 ICLK
0008 7189h	ICU	DTC activation enable register 137	DTCER137	8	8	2 ICLK
0008 718Ah	ICU	DTC activation enable register 138	DTCER138	8	8	2 ICLK
0008 718Bh	ICU	DTC activation enable register 139	DTCER139	8	8	2 ICLK
0008 718Ch	ICU	DTC activation enable register 140	DTCER140	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (18 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 826Fh	SCI5	Serial extended mode register	SEMR	8	8	2 to 3 PCLK*8
0008 8268h	SMCI5	Serial mode register	SMR	8	8	2 to 3 PCLK*8
0008 8269h	SMCI5	Bit rate register	BRR	8	8	2 to 3 PCLK*8
0008 826Ah	SMCI5	Serial control register	SCR	8	8	2 to 3 PCLK*8
0008 826Bh	SMCI5	Transmit data register	TDR	8	8	2 to 3 PCLK*8
0008 826Ch	SMCI5	Serial status register	SSR	8	8	2 to 3 PCLK*8
0008 826Dh	SMCI5	Receive data register	RDR	8	8	2 to 3 PCLK*8
0008 826Eh	SMCI5	Smart card mode register	SCMR	8	8	2 to 3 PCLK*8
0008 8270h	SCI6	Serial mode register	SMR	8	8	2 to 3 PCLK*8
0008 8271h	SCI6	Bit rate register	BRR	8	8	2 to 3 PCLK*8
0008 8272h	SCI6	Serial control register	SCR	8	8	2 to 3 PCLK*8
0008 8273h	SCI6	Transmit data register	TDR	8	8	2 to 3 PCLK*8
0008 8274h	SCI6	Serial status register	SSR	8	8	2 to 3 PCLK*8
0008 8275h	SCI6	Receive data register	RDR	8	8	2 to 3 PCLK*8
0008 8276h	SCI6	Smart card mode register	SCMR	8	8	2 to 3 PCLK*8
0008 8277h	SCI6	Serial extended mode register	SEMR	8	8	2 to 3 PCLK*8
0008 8270h	SMCI6	Serial mode register	SMR	8	8	2 to 3 PCLK*8
0008 8271h	SMCI6	Bit rate register	BRR	8	8	2 to 3 PCLK*8
0008 8272h	SMCI6	Serial control register	SCR	8	8	2 to 3 PCLK*8
0008 8273h	SMCI6	Transmit data register	TDR	8	8	2 to 3 PCLK*8
0008 8274h	SMCI6	Serial status register	SSR	8	8	2 to 3 PCLK*8
0008 8275h	SMCI6	Receive data register	RDR	8	8	2 to 3 PCLK*8
0008 8276h	SMCI6	Smart card mode register	SCMR	8	8	2 to 3 PCLK*8
0008 8280h	CRC	CRC control register	CRCCR	8	8	2 to 3 PCLK*8
0008 8281h	CRC	CRC data input register	CRCDIR	8	8	2 to 3 PCLK*8
0008 8282h	CRC	CRC data output register	CRCDOR	16	16	2 to 3 PCLK*8
0008 8300h	RIIC0	I ² C bus control register 1	ICCR1	8	8	2 to 3 PCLK*8
0008 8301h	RIIC0	I ² C bus control register 2	ICCR2	8	8	2 to 3 PCLK*8
0008 8302h	RIIC0	I ² C bus mode register 1	ICMR1	8	8	2 to 3 PCLK*8
0008 8303h	RIIC0	I ² C bus mode register 2	ICMR2	8	8	2 to 3 PCLK*8
0008 8304h	RIIC0	I ² C bus mode register 3	ICMR3	8	8	2 to 3 PCLK*8
0008 8305h	RIIC0	I ² C bus function enable register	ICFER	8	8	2 to 3 PCLK*8
0008 8306h	RIIC0	I ² C bus status enable register	ICSER	8	8	2 to 3 PCLK*8
0008 8307h	RIIC0	I ² C bus interrupt enable register	ICIER	8	8	2 to 3 PCLK*8
0008 8308h	RIIC0	I ² C bus status register 1	ICSR1	8	8	2 to 3 PCLK*8
0008 8309h	RIIC0	I ² C bus status register 2	ICSR2	8	8	2 to 3 PCLK*8
0008 830Ah	RIIC0	Slave address register L0	SARL0	8	8	2 to 3 PCLK*8
0008 830Ah	RIIC0	Timeout internal counter	TMOCNT	16	16	2 to 3 PCLK*8
0008 830Ah	RIIC0	Timeout internal counter L	TMOCNTL	8	8	2 to 3 PCLK*8
0008 830Bh	RIIC0	Slave address register U0	SARU0	8	8	2 to 3 PCLK*8
0008 830Bh	RIIC0	Timeout internal counter U	TMOCNTU	8	8	2 to 3 PCLK*8
0008 830Ch	RIIC0	Slave address register L1	SARL1	8	8	2 to 3 PCLK*8
0008 830Dh	RIIC0	Slave address register U1	SARU1	8	8	2 to 3 PCLK*8
0008 830Eh	RIIC0	Slave address register L2	SARL2	8	8	2 to 3 PCLK*8
0008 830Fh	RIIC0	Slave address register U2	SARU2	8	8	2 to 3 PCLK*8

Table 4.1 List of I/O Registers (Address Order) (22 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 8726h	MTU0	Timer buffer operation transfer mode register	TBTM	8	8	2 to 3 PCLK*8
0008 8780h	MTU1	Timer control register	TCR	8	8	2 to 3 PCLK*8
0008 8781h	MTU1	Timer mode register	TMDR	8	8	2 to 3 PCLK*8
0008 8782h	MTU1	Timer I/O control register	TIOR	8	8	2 to 3 PCLK*8
0008 8784h	MTU1	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK*8
0008 8785h	MTU1	Timer status register	TSR	8	8	2 to 3 PCLK*8
0008 8786h	MTU1	Timer counter	TCNT	16	16	2 to 3 PCLK*8
0008 8788h	MTU1	Timer general register A	TGRA	16	16	2 to 3 PCLK*8
0008 878Ah	MTU1	Timer general register B	TGRB	16	16	2 to 3 PCLK*8
0008 8790h	MTU1	Timer input capture control register	TICCR	8	8	2 to 3 PCLK*8
0008 8800h	MTU2	Timer control register	TCR	8	8	2 to 3 PCLK*8
0008 8801h	MTU2	Timer mode register	TMDR	8	8	2 to 3 PCLK*8
0008 8802h	MTU2	Timer I/O control register	TIOR	8	8	2 to 3 PCLK*8
0008 8804h	MTU2	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK*8
0008 8805h	MTU2	Timer status register	TSR	8	8	2 to 3 PCLK*8
0008 8806h	MTU2	Timer counter	TCNT	16	16	2 to 3 PCLK*8
0008 8808h	MTU2	Timer general register A	TGRA	16	16	2 to 3 PCLK*8
0008 880Ah	MTU2	Timer general register B	TGRB	16	16	2 to 3 PCLK*8
0008 8880h	MTU5	Timer counter U	TCNTU	16	16	2 to 3 PCLK*8
0008 8882h	MTU5	Timer general register U	TGRU	16	16	2 to 3 PCLK*8
0008 8884h	MTU5	Timer control register U	TCRU	8	8	2 to 3 PCLK*8
0008 8886h	MTU5	Timer I/O control register U	TIORU	8	8	2 to 3 PCLK*8
0008 8890h	MTU5	Timer counter V	TCNTV	16	16	2 to 3 PCLK*8
0008 8892h	MTU5	Timer general register V	TGRV	16	16	2 to 3 PCLK*8
0008 8894h	MTU5	Timer control register V	TCRV	8	8	2 to 3 PCLK*8
0008 8896h	MTU5	Timer I/O control register V	TIORV	8	8	2 to 3 PCLK*8
0008 88A0h	MTU5	Timer counter W	TCNTW	16	16	2 to 3 PCLK*8
0008 88A2h	MTU5	Timer general register W	TGRW	16	16	2 to 3 PCLK*8
0008 88A4h	MTU5	Timer control register W	TCRW	8	8	2 to 3 PCLK*8
0008 88A6h	MTU5	Timer I/O control register W	TIORW	8	8	2 to 3 PCLK*8
0008 88B2h	MTU5	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK*8
0008 88B4h	MTU5	Timer start register	TSTR	8	8	2 to 3 PCLK*8
0008 88B6h	MTU5	Timer compare match clear register	TCNTCMPCLR	8	8	2 to 3 PCLK*8
0008 8900h	POE	Input level control/status register 1	ICSR1	16	16	2 to 3 PCLK*8
0008 8902h	POE	Output level control/status register 1	OCSR1	16	16	2 to 3 PCLK*8
0008 8904h	POE	Input level control/status register 2	ICSR2	16	16	2 to 3 PCLK*8
0008 8906h	POE	Output level control/status register 2	OCSR2	16	16	2 to 3 PCLK*8
0008 8908h	POE	Input level control/status register 3	ICSR3	16	16	2 to 3 PCLK*8
0008 890Ah	POE	Software port output enable register	SPOER	8	8	2 to 3 PCLK*8
0008 890Bh	POE	Port output enable control register 1	POECR1	8	8	2 to 3 PCLK*8
0008 890Ch	POE	Port output enable control register 2	POECR2	16	16	2 to 3 PCLK*8
0008 890Eh	POE	Input level control/status register 4	ICSR4	16	16	2 to 3 PCLK*8
0008 8A00h	MTU9	Timer control register	TCR	8	8	2 to 3 PCLK*8

Table 4.1 List of I/O Registers (Address Order) (25 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 8C94h	MTU11	Timer control register V	TCRV	8	8	2 to 3 PCLK*8
0008 8C96h	MTU11	Timer I/O control register V	TIORV	8	8	2 to 3 PCLK*8
0008 8CA0h	MTU11	Timer counter W	TCNTW	16	16	2 to 3 PCLK*8
0008 8CA2h	MTU11	Timer general register W	TGRW	16	16	2 to 3 PCLK*8
0008 8CA4h	MTU11	Timer control register W	TCRW	8	8	2 to 3 PCLK*8
0008 8CA6h	MTU11	Timer I/O control register W	TIORW	8	8	2 to 3 PCLK*8
0008 8CB2h	MTU11	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK*8
0008 8CB4h	MTU11	Timer start register	TSTR	8	8	2 to 3 PCLK*8
0008 8CB6h	MTU11	Timer compare match clear register	TCNTCMPCLR	8	8	2 to 3 PCLK*8
0008 9000h	S12AD	A/D control register	ADCSR	8	8	2 to 3 PCLK*8
0008 9004h	S12AD	A/D channel select register	ADANS	16	16	2 to 3 PCLK*8
0008 9008h	S12AD	A/D-converted value addition mode select register	ADADS	16	16	2 to 3 PCLK*8
0008 900Ch	S12AD	A/D-converted value addition count select register	ADADC	8	8	2 to 3 PCLK*8
0008 900Eh	S12AD	A/D control extended register	ADCER	16	16	2 to 3 PCLK*8
0008 9010h	S12AD	A/D start trigger select register	ADSTRGR	8	8	2 to 3 PCLK*8
0008 9020h	S12AD	A/D data register 0	ADDR0	16	16	2 to 3 PCLK*8
0008 9022h	S12AD	A/D data register 1	ADDR1	16	16	2 to 3 PCLK*8
0008 9024h	S12AD	A/D data register 2	ADDR2	16	16	2 to 3 PCLK*8
0008 9026h	S12AD	A/D data register 3	ADDR3	16	16	2 to 3 PCLK*8
0008 9028h	S12AD	A/D data register 4	ADDR4	16	16	2 to 3 PCLK*8
0008 902Ah	S12AD	A/D data register 5	ADDR5	16	16	2 to 3 PCLK*8
0008 902Ch	S12AD	A/D data register 6	ADDR6	16	16	2 to 3 PCLK*8
0008 902Eh	S12AD	A/D data register 7	ADDR7	16	16	2 to 3 PCLK*8
0008 C000h	PORT0	Data direction register	DDR	8	8	2 to 3 PCLK*8
0008 C001h	PORT1	Data direction register	DDR	8	8	2 to 3 PCLK*8
0008 C002h	PORT2	Data direction register	DDR	8	8	2 to 3 PCLK*8
0008 C003h	PORT3	Data direction register	DDR	8	8	2 to 3 PCLK*8
0008 C004h	PORT4	Data direction register	DDR	8	8	2 to 3 PCLK*8
0008 C005h	PORT5	Data direction register	DDR	8	8	2 to 3 PCLK*8
0008 C006h	PORT6	Data direction register	DDR*6*7	8	8	2 to 3 PCLK*8
0008 C007h	PORT7	Data direction register	DDR*6*7	8	8	2 to 3 PCLK*8
0008 C008h	PORT8	Data direction register	DDR*6*7	8	8	2 to 3 PCLK*8
0008 C009h	PORT9	Data direction register	DDR*6*7	8	8	2 to 3 PCLK*8
0008 C00Ah	PORTA	Data direction register	DDR	8	8	2 to 3 PCLK*8
0008 C00Bh	PORTB	Data direction register	DDR	8	8	2 to 3 PCLK*8
0008 C00Ch	PORTC	Data direction register	DDR	8	8	2 to 3 PCLK*8
0008 C00Dh	PORTD	Data direction register	DDR	8	8	2 to 3 PCLK*8
0008 C00Eh	PORTE	Data direction register	DDR*7	8	8	2 to 3 PCLK*8
0008 C00Fh	PORTF	Data direction register	DDR*5*6*7	8	8	2 to 3 PCLK*8
0008 C010h	PORTG	Data direction register	DDR*5*6*7	8	8	2 to 3 PCLK*8
0008 C020h	PORT0	Data register	DR	8	8	2 to 3 PCLK*8
0008 C021h	PORT1	Data register	DR	8	8	2 to 3 PCLK*8
0008 C022h	PORT2	Data register	DR	8	8	2 to 3 PCLK*8

Table 4.1 List of I/O Registers (Address Order) (33 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000A 0254h	USB1	USB request type register	USBREQ	16	16	at least 9 PCLK*9
000A 0256h	USB1	USB request value register	USBVAL	16	16	at least 9 PCLK*9
000A 0258h	USB1	USB request index register	USBINDX	16	16	at least 9 PCLK*9
000A 025Ah	USB1	USB request length register	USBLENG	16	16	at least 9 PCLK*9
000A 025Ch	USB1	DCP configuration register	DCPCFG	16	16	at least 9 PCLK*9
000A 025Eh	USB1	DCP maximum packet size register	DCPMAXP	16	16	at least 9 PCLK*9
000A 0260h	USB1	DCP control register	DCPCTR	16	16	at least 9 PCLK*9
000A 0264h	USB1	Pipe window select register	PIPESEL	16	16	at least 9 PCLK*9
000A 0268h	USB1	Pipe configuration register	PIPECFG	16	16	at least 9 PCLK*9
000A 026Ch	USB1	Pipe maximum packet size register	PIPEMAXP	16	16	at least 9 PCLK*9
000A 026Eh	USB1	Pipe cycle control register	PIPEPERI	16	16	at least 9 PCLK*9
000A 0270h	USB1	Pipe 1 control register	PIPE1CTR	16	16	at least 9 PCLK*9
000A 0272h	USB1	Pipe 2 control register	PIPE2CTR	16	16	at least 9 PCLK*9
000A 0274h	USB1	Pipe 3 control register	PIPE3CTR	16	16	at least 9 PCLK*9
000A 0276h	USB1	Pipe 4 control register	PIPE4CTR	16	16	at least 9 PCLK*9
000A 0278h	USB1	Pipe 5 control register	PIPE5CTR	16	16	at least 9 PCLK*9
000A 027Ah	USB1	Pipe 6 control register	PIPE6CTR	16	16	at least 9 PCLK*9
000A 027Ch	USB1	Pipe 7 control register	PIPE7CTR	16	16	at least 9 PCLK*9
000A 027Eh	USB1	Pipe 8 control register	PIPE8CTR	16	16	at least 9 PCLK*9
000A 0280h	USB1	Pipe 9 control register	PIPE9CTR	16	16	at least 9 PCLK*9
000A 0290h	USB1	Pipe 1 transaction counter enable register	PIPE1TRE	16	16	at least 9 PCLK*9
000A 0292h	USB1	Pipe 1 transaction counter register	PIPE1TRN	16	16	at least 9 PCLK*9
000A 0294h	USB1	Pipe 2 transaction counter enable register	PIPE2TRE	16	16	at least 9 PCLK*9
000A 0296h	USB1	Pipe 2 transaction counter register	PIPE2TRN	16	16	at least 9 PCLK*9
000A 0298h	USB1	Pipe 3 transaction counter enable register	PIPE3TRE	16	16	at least 9 PCLK*9
000A 029Ah	USB1	Pipe 3 transaction counter register	PIPE3TRN	16	16	at least 9 PCLK*9

Table 5.11 Bus Timing [100-pin LQFP/85-pin TFLGA]

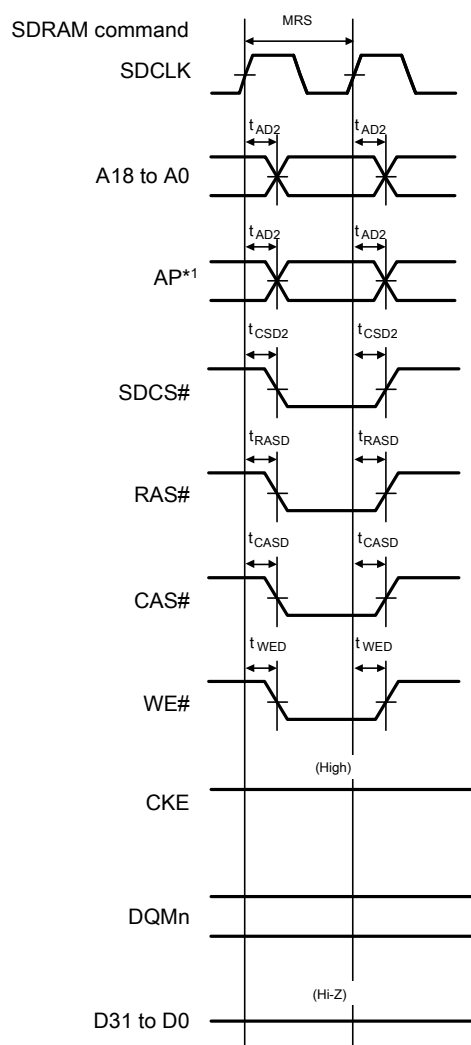
Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC

VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V

ICLK = 8 to 100 MHz, PCLK = 8 to 50 MHz, BCLK = 8 to 50 MHz

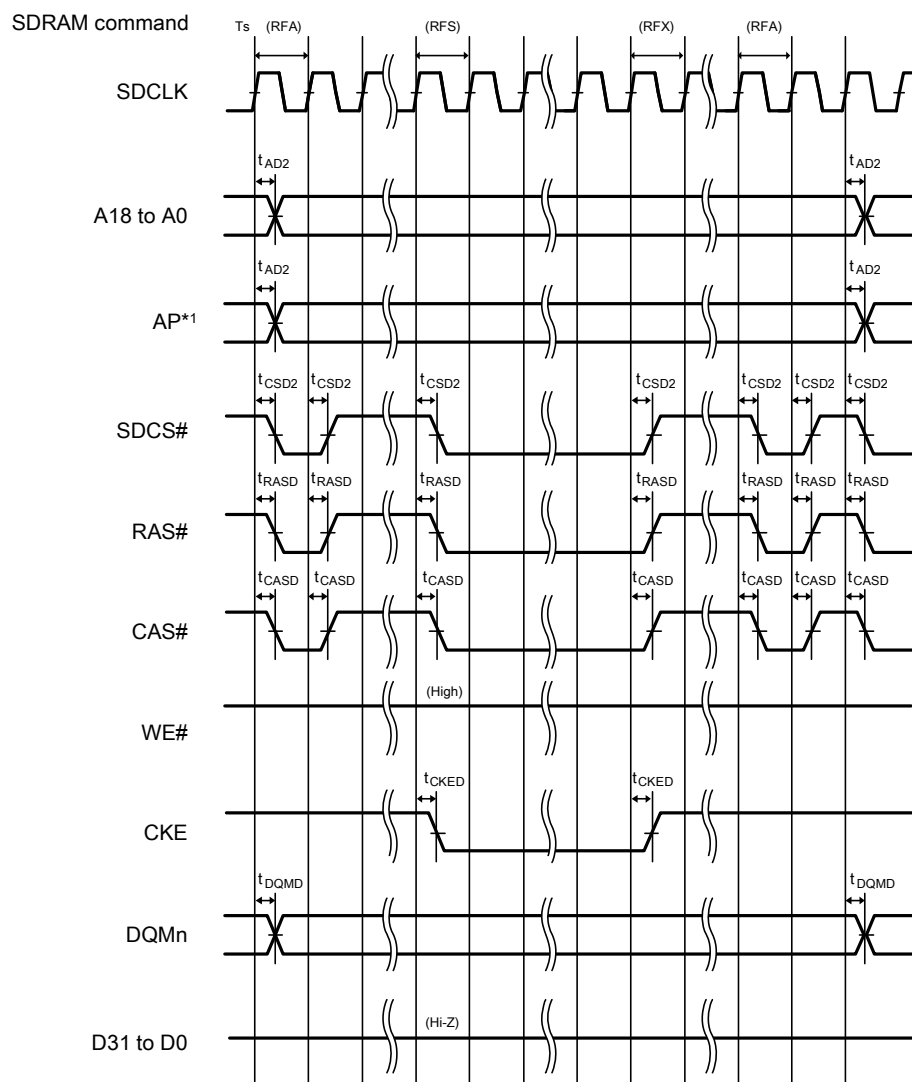
T_a = -40 to +85°COutput load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, I_{OH} = -1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t _{AD}	—	30	ns	Figure 5.10 to Figure 5.13
Byte control delay time	t _{BCD}	—	30	ns	
CS# delay time	t _{CSD}	—	30	ns	
RD# delay time	t _{RSD}	—	30	ns	
Read data setup time	t _{RDS}	15	—	ns	
Read data hold time	t _{RDH}	0.0	—	ns	
WR# delay time	t _{WRD}	—	30	ns	
Write data delay time	t _{WDD}	—	35	ns	
Write data hold time	t _{WDH}	0	—	ns	
WAIT# setup time	t _{WTS}	15	—	ns	Figure 5.14
WAIT# hold time	t _{WTH}	0.0	—	ns	



Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.20 SDRAM Space Mode Register Set Bus Timing



Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.21 SDRAM Space Self-Refresh Bus Timing

Table 5.15 Timing of On-Chip Peripheral Modules (5)

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC

VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V

PCLK = 8 to 50 MHz

T_a = -40 to +85°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
RSPi	Data output hold time	Master	t_{OH}	0	—	ns	Figure 5.39 to Figure 5.42
		Slave		0	—		
	Successive transmission delay time	Master	t_{TD}	$t_{SPcyc}+2 \times t_{Pcyc}$	$8 \times t_{SPcyc}+2 \times t_{Pcyc}$	ns	
		Slave		$4 \times t_{Pcyc}$	—		
	MOSI, MISO rise/fall time	Output [176-pin LFBGA/ 145-pin TFLGA/ 144-pin LQFP]	t_{Dr} , t_{Df}	—	5	ns	
		Output [100-pin LQFP/ 85-pin TFLGA]		—	10		
		Input		—	1	μs	
	SSL rise/fall time	Output [176-pin LFBGA 145-pin TFLGA 144-pin LQFP]	t_{SSLr} , t_{SSLf}	—	5	ns	
		Output [100-pin LQFP/ 85-pin TFLGA]		—	10		
		Input		—	1	μs	
	Slave access time		t_{SA}	—	4	t_{Pcyc}	Figure 5.41 and Figure 5.42
	Slave output release time		t_{REL}	—	3	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle

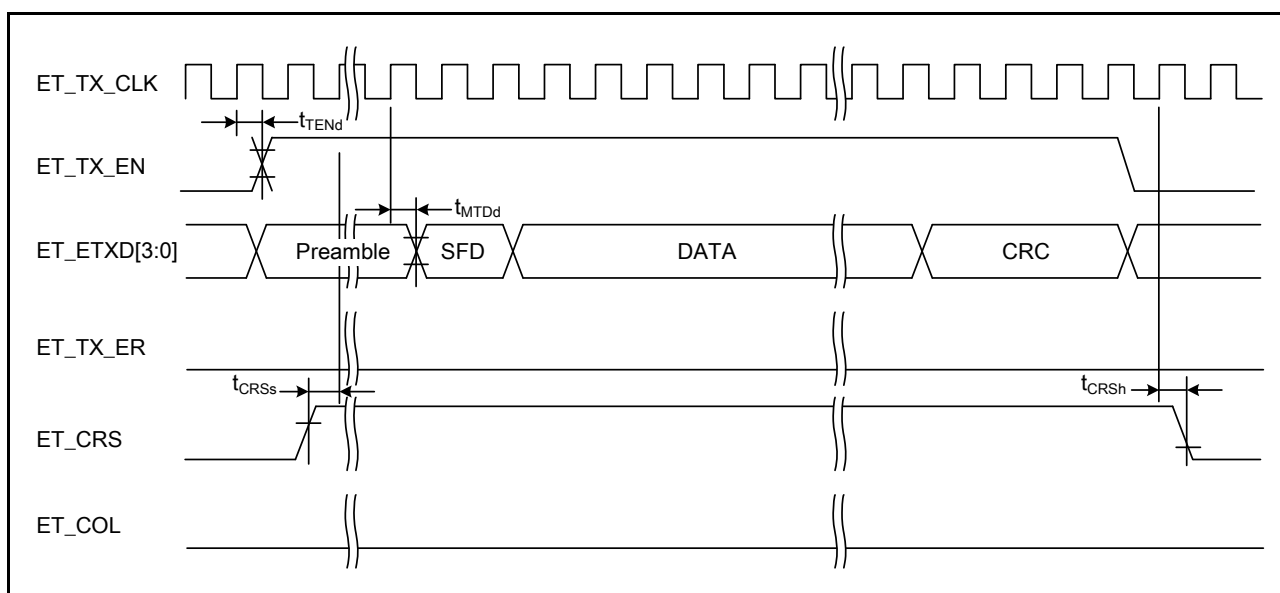


Figure 5.51 MII Transmission Timing (Normal Operation)

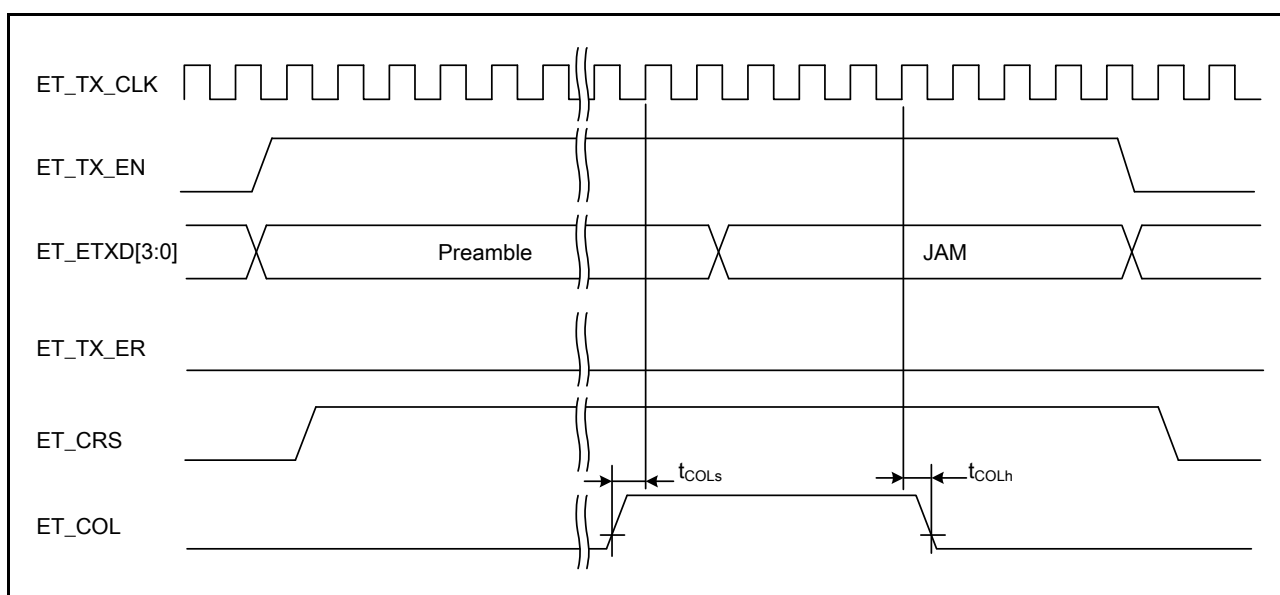


Figure 5.52 MII Transmission Timing (Conflict Occurrence)

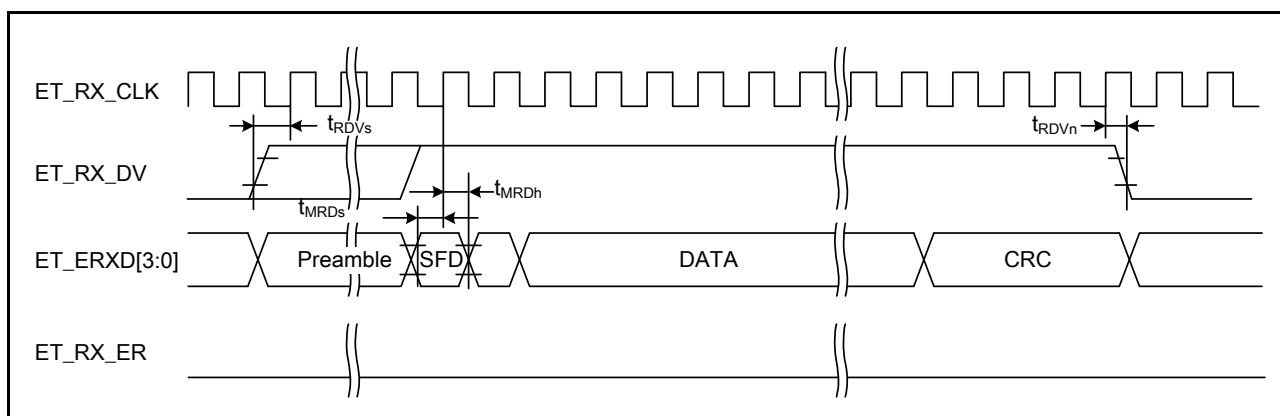


Figure 5.53 MII Reception Timing (Normal Operation)

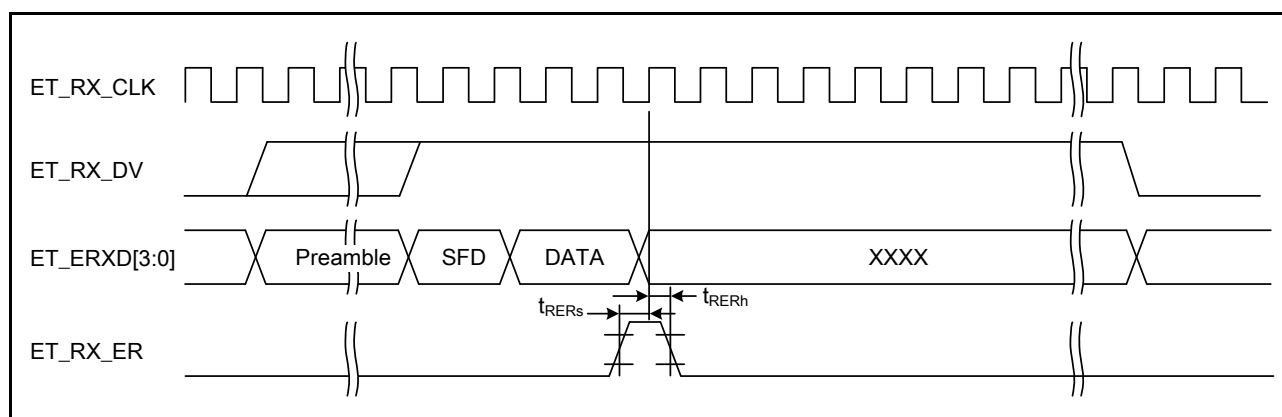


Figure 5.54 MII Reception Timing (Error Occurrence)

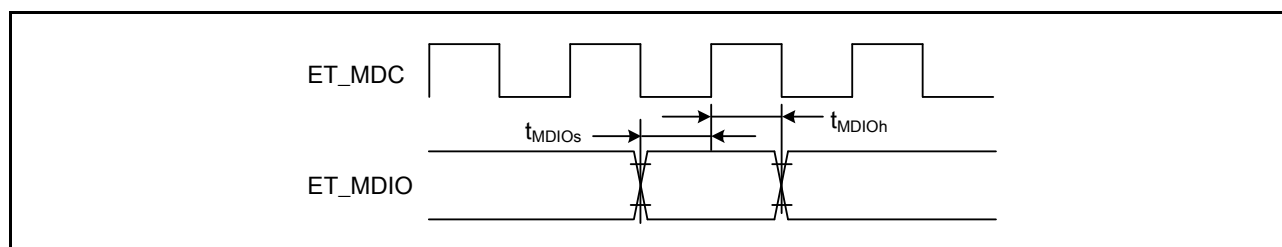


Figure 5.55 MDIO Input Timing (MII)

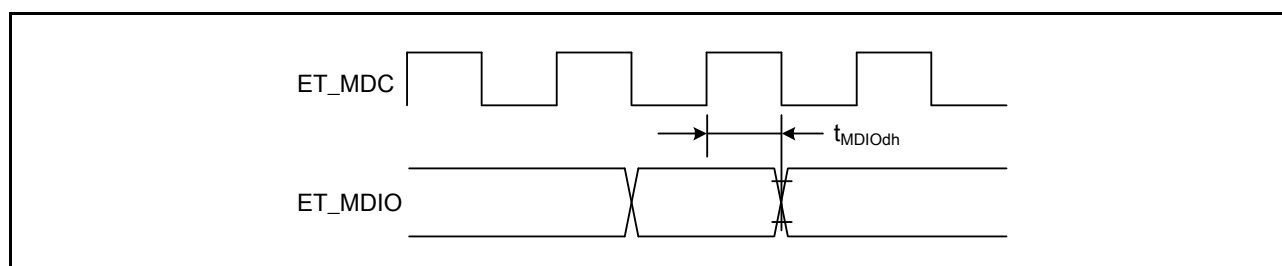


Figure 5.56 MDIO Output Timing (MII)

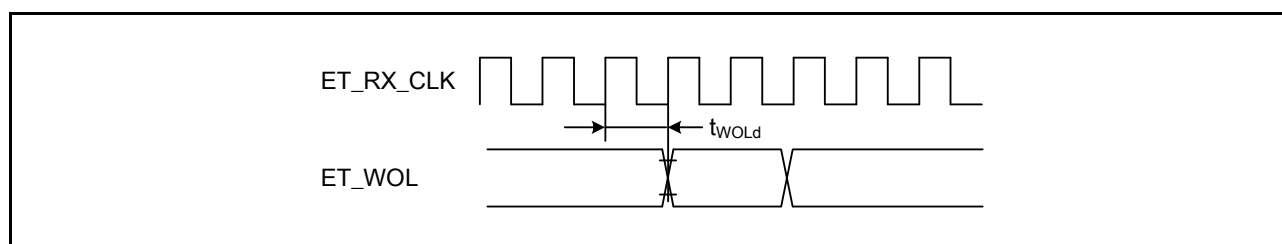


Figure 5.57 WOL Output Timing (MII)

5.4 USB Characteristics

Table 5.19 Internal USB Full-Speed Characteristics (DP, DM Pin Characteristics)

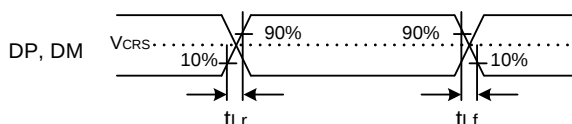
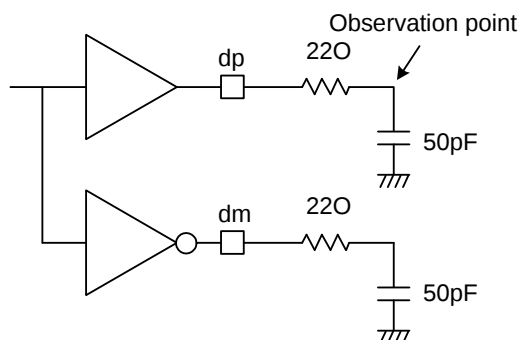
Conditions: VCC = PLLVCC = AVCC = VCC_USB = 3.0 to 3.6 V, VREFH = 3.0 V to AVCC

VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V

PCLK = 24 to 50 MHz

T_a = -40 to +85°C

Item		Symbol	Min.	Max.	Unit	Test Conditions	
Input characteristics	Input high level voltage	V _{IH}	2.0	—	V		Figure 5.61 and Figure 5.62
	Input low level voltage	V _{IL}	—	0.8	V		
	Differential input Sensitivity	V _{DI}	0.2	—	V	DP — DM	
	Differential common mode range	V _{CM}	0.8	2.5	V		
Output characteristics	Output high level voltage	V _{OH}	2.8	3.6	V	I _{OH} = -200μA	
	Output low level voltage	V _{OL}	0.0	0.3	V	I _{OL} = 2 mA	
	Cross over voltage	V _{CRS}	1.3	2.0	V		
	Rising time	t _{Lr}	4	20	ns		
	Falling time	t _{Lf}	4	20	ns		
	Rising/falling time ratio	t _{Lr} / t _{Lf}	90	111.11	%	t _{Lr} / t _{Lf}	
	Output resistance	Z _{DRV}	28	44	Ω	Rs = 22Ω included	

**Figure 5.61 DP, DM Output Timing (Full-Speed)****Figure 5.62 Test Circuit (Full-Speed)**

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

- The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.