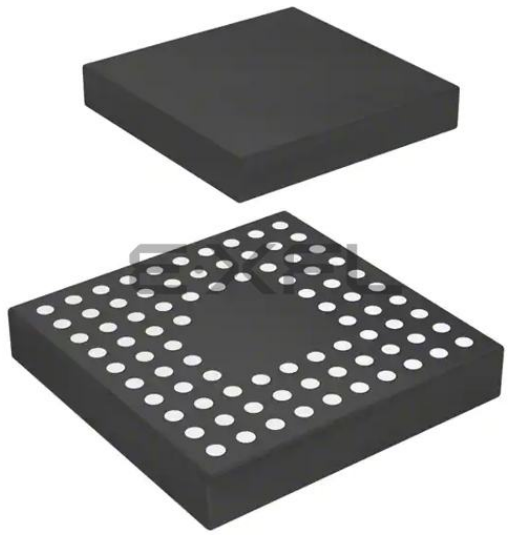
Renesas Electronics America Inc - R5F56217BDLD#U0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	58
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	85-TFLGA
Supplier Device Package	85-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f56217bdld-u0

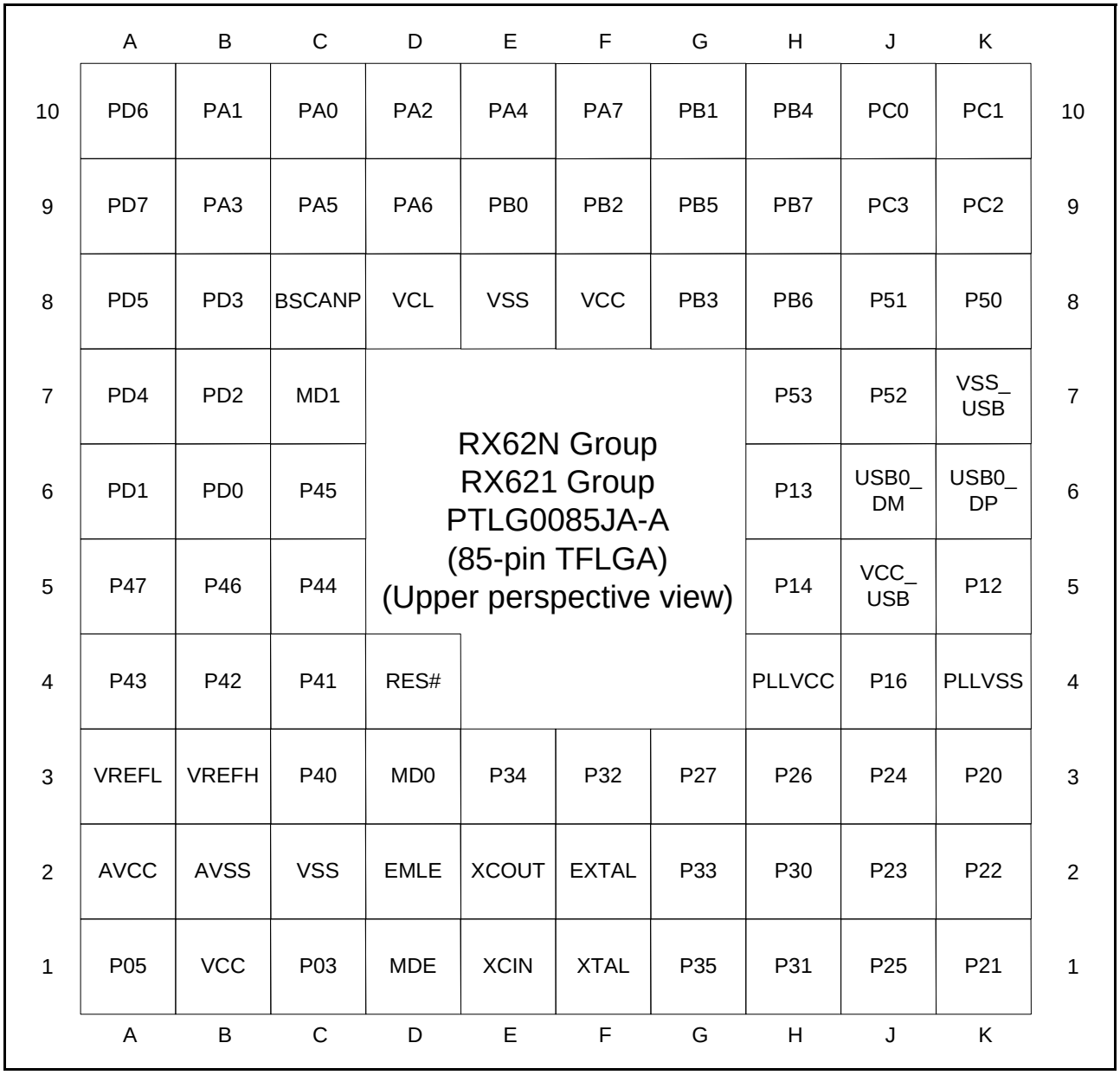


Figure 1.9 Pin Assignment of the 85-Pin TFLGA

Table 1.4 List of Pins and Pin Functions (176-Pin LFBGA) (5 / 6)

Pin No. 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	External Bus EXDMAC	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE, WDT)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
N2		P23	EDACK0-B		USB0_DPUPE-A	MTIOC3D-A/ MTCLKD-A/ PO3	TxD3-B	
N3		P20			USB0_ID	MTIOC1A/ TMRI0-B/ PO0	SDA1/ TxD0	
N4		P17			USB1_VBUS/ USB1_OVRCURB/ USB1_VBUSEN-B	MTIOC3A/ PO15	TxD3-A	IRQ7-B
N5		P15			USB1_OVRCURA/ USB1_DPUPE-B	MTIOC0B/ TMCI2-A/ PO13	SCK3-A	IRQ5-B
N6		P57	WAIT#-A/ WR3#/ BC3#/ EDREQ1-C					
N7		P10			USB1_DPUPE-A	MTIC5W-A/ TMRI3-A		IRQ0-B
N8		P52	RD#				SSLB3-A/ RxD2-B	
N9	VCC							
N10		PC5	A21-A/ CS2#-C/ WAIT#-C	ET_ETXD2		MTIC11W-A/ MTCLKD-B	RSPCKA-A	
N11		PC3	A19-A	ET_TX_ER		MTCLKF-A	TxD5	
N12		PC2	A18-A	ET_RX_DV		MTCLKE-A	SSLA3-A/ RxD5	
N13		P74	CS4#-B	ET_ERXD1/ RMII_RXD1				
N14		P73	CS3#-B	ET_WOL				
N15		PB5	A13			MTIOC10C/ MTCLKF-B/ PO29		
P1		P24	CS4#-C/ EDREQ1-B		USB0_VBUSEN-A	MTIOC4A-A/ MTCLKA-A/ TMRI1/ PO4	SCK3-B	
P2	PLLVCC							
P3		P16			USB0_VBUS/ USB0_OVRCURB/ USB0_VBUSEN-B	MTIOC3C-A/ TMO2/ PO14	RxD3-A	IRQ6-B
P4		P14			USB0_OVRCURA/ USB0_DPUPE-B	TMRI2		IRQ4-B
P5		P13				TMO3	SDA0/ TxD2-A	IRQ3-B/ ADTRG1#
P6	VCC_USB							

Table 1.5 List of Pins and Pin Functions (145-Pin TFLGA) (4 / 5)

Pin No. 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	External Bus EXDMAC	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE, WDT)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
K4		P26	CS6#-C			MTIOC2A/ TMO1/ PO6	MOSIB-A/ TxD1	TDO
K5	BCLK	P53						
K6	VSS							
K7		PC7	A23/ CS0#-B	ET_COL		MTIC11U-A/ MTCLKB-B	MISOA-A	
K8		P82	EDREQ1-A	ET_ETXD1/ RMII_TXD1		MTIOC4A-B		TRSYNC
K9		PC3	A19-A	ET_TX_ER		MTCLKF-A	TxD5	
K10		PB7	A15			MTIOC10D/ PO31		
K11		P73	CS3#-B	ET_WOL				
K12		PC0	A16-A	ET_ERXD3		MTCLKG-A	SSLA1-A	
K13		PB3	A11			MTIOC9D/ MTCLKH-B/ PO27		
L1		P25	CS5#-C/ EDACK1-B		USB0_DPRPD	MTIOC4C-A/ MTCLKB-A/ PO5	RxD3-B	ADTRG0#-B
L2		P22	EDREQ0-B		USB0_DRPD	MTIOC3B-A/ MTCLKC-A/ TMO0/PO2	SCK0	
L3		P17				MTIOC3A/ PO15	TxD3-A	IRQ7-B
L4		P12				TMCI1-B	SCL0/ RxD2-A	IRQ2-B
L5	VCC_USB							
L6		P56	EDACK1-C			MTIOC3C-B		
L7		P52	RD#				SSLB3-A/ RxD2-B	
L8		P83	EDACK1-A	ET_CRS/ RMII_CRS_DV		MTIOC4C-B		TRCLK
L9		P81	EDACK0-A	ET_ETXD0/ RMII_TXD0		MTIOC3D-B		TRDATA1
L10		P77	CS7#-B	ET_RX_ER/ RMII_RX_ER				
L11		P75	CS5#-B	ET_ERXD0/ RMII_RXD0				
L12	VCC							
L13		PB6	A14			MTIOC10B/ PO30		
M1		P23	EDACK0-B		USB0_DPUPE-A	MTIOC3D-A/ MTCLKD-A/ PO3	TxD3-B	
M2		P20			USB0_ID	MTIOC1A/ TMRI0-B/ PO0	SDA1/ TxD0	
M3	PLLVCC							

Table 1.5 List of Pins and Pin Functions (145-Pin TFLGA) (5 / 5)

Pin No. 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	External Bus EXDMAC	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE, WDT)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
M4		P15				MTIOC0B/ TMCI2-A/ PO13	SCK3-A	IRQ5-B
M5		P14			USB0_OVRCURA/ USB0_DPUPE-B	TMRI2		IRQ4-B
M6	VSS_USB							
M7		P55	WAIT#-B/ EDREQ0-C	ET_EXOUT		MTIOC4D-B		TRDATA3
M8		P50	WR0#/ WR#				SSLB1-A/ TxD2-B	
M9		PC6	A22/CS1#-C	ET_ETXD3		MTIC11V-A/ MTCLKA-B	MOSIA-A	
M10		P80	EDREQ0-A	ET_TX_EN/ RMII_TXD_EN		MTIOC3B-B		TRDATA0
M11		PC2	A18-A	ET_RX_DV		MTCLKE-A	SSLA3-A/ RxD5	
M12		PC1	A17-A	ET_ERXD2		MTCLKH-A	SSLA2-A/ SCK5	
M13	VSS							
N1		P21			USB0_EXICEN	MTIOC1B/ TMCI0-B/ PO1	SCL1/RxD0	
N2		P16			USB0_VBUS/ USB0_OVRCURB/ USB0_VBUSEN-B	MTIOC3C-A/ TMO2/ PO14	RxD3-A	IRQ6-B
N3	PLLVSS							
N4		P13				TMO3	SDA0/ TxD2-A	IRQ3-B/ ADTRG1#
N5					USB0_DM			
N6					USB0_DP			
N7		P54	EDACK0-C	ET_LINKSTA		MTIOC4B-B		TRDATA2
N8		P51	WR1#/BC1#/ WAIT#-D				SSLB2-A/ SCK2	
N9	VCC							
N10		PC5	A21/CS2#-C/ WAIT#-C	ET_ETXD2		MTIC11W-A/ MTCLKD-B	RSPCKA-A	
N11		PC4	A20/CS3#-C	ET_TX_CLK		MTCLKC-B	SSLA0-A	
N12		P76	CS6#-B	ET_RX_CLK/ REF50CK				
N13		P74	CS4#-B	ET_ERXD1/ RMII_RXD1				

Table 1.9 Pin Functions (5 / 7)

Classifications	Pin Name	I/O	Description
Ethernet controller	REF50CK	Input	50-MHz reference clock. This pin inputs reference signals for transmission/reception timings in RMII mode.
	RMII_CRS_DV	Input	Indicates that there are carrier detection signals and valid receive data on RMII_RXD1 and RMII_RXD0 in RMII mode.
	RMII_TXD0, RMII_TXD1	Output	2-bit transmit data in RMII mode.
	RMII_RXD0, RMII_RXD1	Input	2-bit receive data in RMII mode.
	RMII_TXD_EN	Output	Output pin for data transmit enable signals in RMII mode.
	RMII_RX_ER	Input	Indicates an error has occurred during reception of data in RMII mode.
	ET_CRS	Input	Carrier detection/data reception enable pin.
	ET_RX_DV	Input	Indicates that there are valid receive data on ET_ERXD3 to ET_ERXD0.
	ET_EXOUT	Output	General-purpose external output pin.
	ET_LINKSTA	Input	Inputs link status from the PHY-LSI.
	ET_ETXD0 to ET_ETXD3	Output	4 bits of MII transmit data.
	ET_ERXD0 to ET_ERXD3	Input	4 bits of MII receive data.
	ET_TX_EN	Output	Transmit enable pin. Indicates that transmit data is ready on ET_ETXD3 to ET_ETXD0.
	ET_TX_ER	Output	Transmit error pin. Notifies the PHY_LSI of an error during transmission.
	ET_RX_ER	Input	Receive error pin. Recognizes an error during reception.
	ET_TX_CLK	Input	Transmit clock pin. This pin inputs reference signals for output timings from ET_TX_EN, ET_ETXD3 to ET_ETXD0, and ET_TX_ER.
	ET_RX_CLK	Input	Receive clock pin. This pin inputs reference signals for input timings to ET_RX_DV, ET_ERXD3 to ET_ERXD0, and ET_RX_ER.
	ET_COL	Input	Inputs collision detection signals.
	ET_WOL	Output	Receives Magic Packets™
	ET_MDC	Output	Outputs reference clock signals for information transfer via ET_MDIO.
	ET_MDIO	I/O	These pins carry bidirectional signals for the exchange of management information between the RX62N Group and the PHY-LSI.

Table 1.9 Pin Functions (6 / 7)

Classifications	Pin Name	I/O	Description
USB 2.0 host/function module	VCC_USB	Input	Power-supply pin for the USB. Connect this pin to the system power supply even when the USB is not to be used.
	VSS_USB	Input	Ground pin for the USB. Connect this pin to the system power supply (0 V) even when the USB is not to be used.
	USB0_DP USB1_DP	I/O	Inputs or outputs D+ data for the USB bus.
	USB0_DM USB1_DM	I/O	Inputs or outputs D- data for the USB bus.
	USB0_DPRPD USB1_DPRPD	Output	Enable D+ pull-down.
	USB0_DRPD USB1_DRPD	Output	Enable D- pull-down.
	USB0_EXICEN USB1_EXICEN	Output	Connect these pins to the OTG power supply IC.
	USB0_ID USB1_ID	Input	Connect these pins to the OTG power supply IC.
	USB0_VBUSEN-A/ USB0_VBUSEN-B USB1_VBUSEN-A/ USB1_VBUSEN-B	Output	VBUS power enable pins for the USB.
	USB0_DPUPE-A/ USB0_DPUPE-B USB1_DPUPE-A/ USB1_DPUPE-B	Output	Pull-up pins for the USB.
	USB0_OVRCURA/ USB0_OVRCURB USB1_OVRCURA/ USB1_OVRCURB	Input	Over current pins for the USB.
	USB0_VBUS USB1_VBUS	Input	Input pins for detection of connection and disconnection of the USB cable.
CAN module	CRX0	Input	Input pins for the CAN.
	CTX0	Output	Output pins for the CAN.
Serial peripheral interfaces	RSPCKA-A/ RSPCKA-B	I/O	Clock input/output pins for the RSPI.
	RSPCKB-A/ RSPCKB-B	I/O	Clock input/output pins for the RSPI
	MOSIA-A/MOSIA-B MOSIB-A/MOSIB-B	I/O	Input or output data output from the master for the RSPI.
	MISOA-A/MISOA-B MISOB-A/MISOB-B	I/O	Input or output data output from the slave for the RSPI.
	SSLA0-A/SSLA0-B	I/O	Select the slave for the RSPI.
	SSLA1-A/SSLA1-B SSLA2-A/SSLA2-B SSLA3-A/SSLA3-B	Output	
	SSLB0-A/SSLB0-B	I/O	
	SSLB1-A/SSLB1-B SSLB2-A/SSLB2-B SSLB3-A/SSLB3-B	Output	
Realtime clock	RTCOUT	Output	Output pin for 1-Hz clock.
A/D converter	AN0 to AN7	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRG0#-A/ADTRG0#-B ADTRG1#	Input	Input pins for the external trigger signals that start the A/D conversion.
D/A converter	DA0, DA1	Output	Output pins for the analog signals from the D/A converter.

2. CPU

The RX CPU has sixteen general-purpose registers, nine control registers, and one accumulator used for DSP instructions.

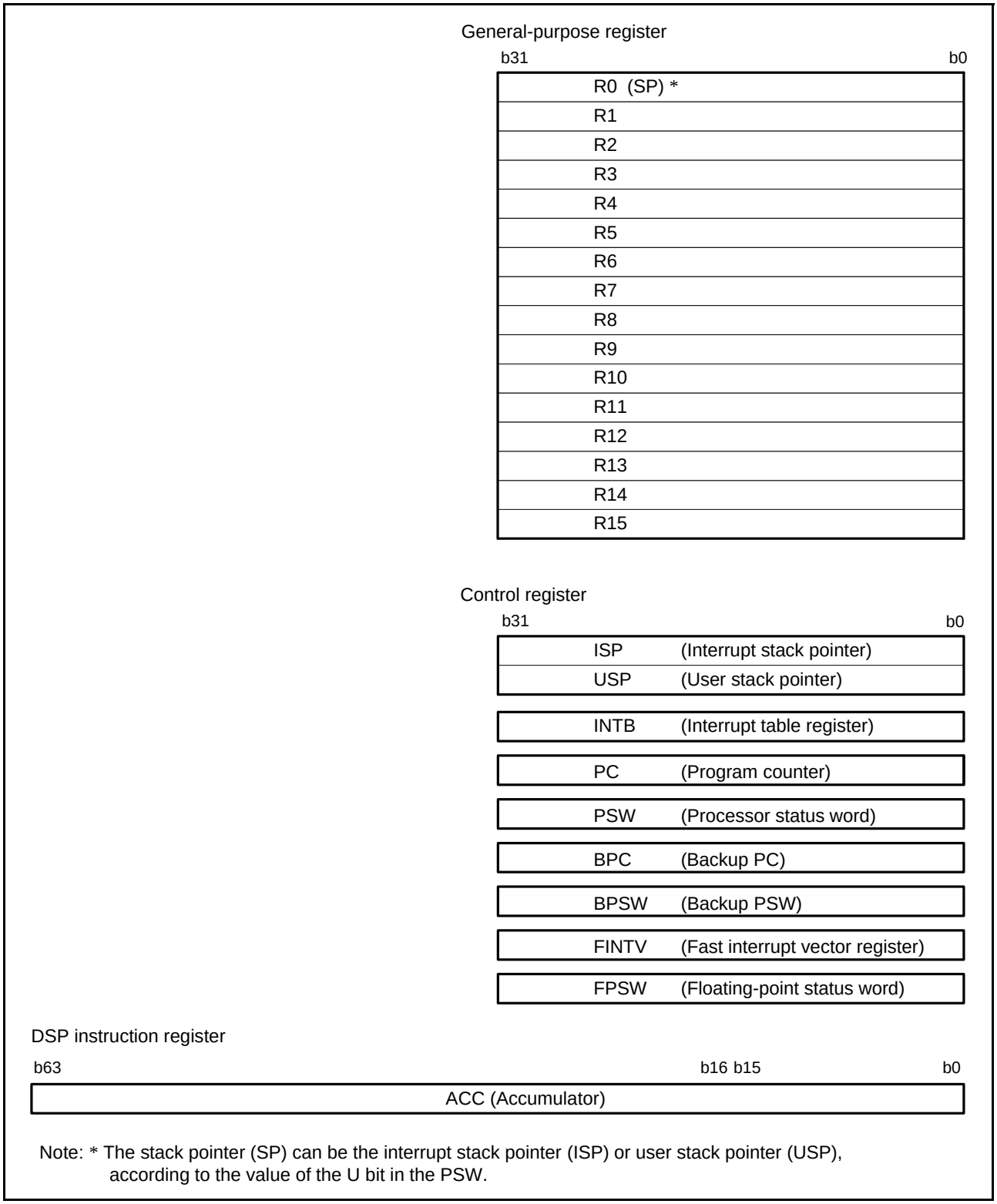


Figure 2.1 Register Set of the CPU

Table 4.1 List of I/O Registers (Address Order) (15 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 8053h	AD0	A/D sampling state register	ADSSTR	8	8	2 to 3 PCLK*8
0008 805Fh	AD0	A/D self-diagnostic register	ADDIAGR	8	8	2 to 3 PCLK*8
0008 8060h	AD1	A/D data register A	ADDRA	16	16	2 to 3 PCLK*8
0008 8062h	AD1	A/D data register B	ADDRB	16	16	2 to 3 PCLK*8
0008 8064h	AD1	A/D data register C	ADDRC	16	16	2 to 3 PCLK*8
0008 8066h	AD1	A/D data register D	ADDRD	16	16	2 to 3 PCLK*8
0008 8070h	AD1	A/D control/status register	ADCSR	8	8	2 to 3 PCLK*8
0008 8071h	AD1	A/D control register	ADCR	8	8	2 to 3 PCLK*8
0008 8072h	AD1	ADDRn format select register	ADDPR	8	8	2 to 3 PCLK*8
0008 8073h	AD1	A/D sampling state register	ADSSTR	8	8	2 to 3 PCLK*8
0008 807Fh	AD1	A/D self-diagnostic register	ADDIAGR	8	8	2 to 3 PCLK*8
0008 80C0h	DA	D/A data register 0	DADR0	16	16	2 to 3 PCLK*8
0008 80C2h	DA	D/A data register 1	DADR1	16	16	2 to 3 PCLK*8
0008 80C4h	DA	D/A control register	DACR	8	8	2 to 3 PCLK*8
0008 80C5h	DA	DADRm format select register	DADPR	8	8	2 to 3 PCLK*8
0008 81E6h	PPG0	PPG output control register	PCR	8	8	2 to 3 PCLK*8
0008 81E7h	PPG0	PPG output mode register	PMR	8	8	2 to 3 PCLK*8
0008 81E8h	PPG0	Next data enable register H	NDERH	8	8	2 to 3 PCLK*8
0008 81E9h	PPG0	Next data enable register L	NDERL	8	8	2 to 3 PCLK*8
0008 81EAh	PPG0	Output data register H	PODRH	8	8	2 to 3 PCLK*8
0008 81EBh	PPG0	Output data register L	PODRL	8	8	2 to 3 PCLK*8
0008 81ECh*1	PPG0	Next data register H	NDRH	8	8	2 to 3 PCLK*8
0008 81EDh*2	PPG0	Next data register L	NDRL	8	8	2 to 3 PCLK*8
0008 81EEh*1	PPG0	Next data register H2	NDRH2	8	8	2 to 3 PCLK*8
0008 81EFh*2	PPG0	Next data register L2	NDRL2	8	8	2 to 3 PCLK*8
0008 81F0h	PPG1	PPG trigger select register	PTRSLR	8	8	2 to 3 PCLK*8
0008 81F6h	PPG1	PPG output control register	PCR	8	8	2 to 3 PCLK*8
0008 81F7h	PPG1	PPG output mode register	PMR	8	8	2 to 3 PCLK*8
0008 81F8h	PPG1	Next data enable register H	NDERH	8	8	2 to 3 PCLK*8
0008 81F9h	PPG1	Next data enable register L	NDERL	8	8	2 to 3 PCLK*8
0008 81FAh	PPG1	Output data register H	PODRH	8	8	2 to 3 PCLK*8
0008 81FBh	PPG1	Output data register L	PODRL	8	8	2 to 3 PCLK*8
0008 81FCh*3	PPG1	Next data register H	NDRH	8	8	2 to 3 PCLK*8
0008 81FDh*4	PPG1	Next data register L	NDRL	8	8	2 to 3 PCLK*8
0008 81FEh*3	PPG1	Next data register H2	NDRH2	8	8	2 to 3 PCLK*8
0008 81FFh*4	PPG1	Next data register L2	NDRL2	8	8	2 to 3 PCLK*8
0008 8200h	TMR0	Timer control register	TCR	8	8	2 to 3 PCLK*8
0008 8201h	TMR1	Timer control register	TCR	8	8	2 to 3 PCLK*8
0008 8202h	TMR0	Timer control/status register	TCSR	8	8	2 to 3 PCLK*8
0008 8203h	TMR1	Timer control/status register	TCSR	8	8	2 to 3 PCLK*8
0008 8204h	TMR0	Time constant register A	TCORA	8	8	2 to 3 PCLK*8
0008 8205h	TMR1	Time constant register A	TCORA	8	8	2 to 3 PCLK*8
0008 8206h	TMR0	Time constant register B	TCORB	8	8	2 to 3 PCLK*8
0008 8207h	TMR1	Time constant register B	TCORB	8	8	2 to 3 PCLK*8
0008 8208h	TMR0	Timer counter	TCNT	8	8	2 to 3 PCLK*8

Table 4.1 List of I/O Registers (Address Order) (22 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 8726h	MTU0	Timer buffer operation transfer mode register	TBTM	8	8	2 to 3 PCLK*8
0008 8780h	MTU1	Timer control register	TCR	8	8	2 to 3 PCLK*8
0008 8781h	MTU1	Timer mode register	TMDR	8	8	2 to 3 PCLK*8
0008 8782h	MTU1	Timer I/O control register	TIOR	8	8	2 to 3 PCLK*8
0008 8784h	MTU1	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK*8
0008 8785h	MTU1	Timer status register	TSR	8	8	2 to 3 PCLK*8
0008 8786h	MTU1	Timer counter	TCNT	16	16	2 to 3 PCLK*8
0008 8788h	MTU1	Timer general register A	TGRA	16	16	2 to 3 PCLK*8
0008 878Ah	MTU1	Timer general register B	TGRB	16	16	2 to 3 PCLK*8
0008 8790h	MTU1	Timer input capture control register	TICCR	8	8	2 to 3 PCLK*8
0008 8800h	MTU2	Timer control register	TCR	8	8	2 to 3 PCLK*8
0008 8801h	MTU2	Timer mode register	TMDR	8	8	2 to 3 PCLK*8
0008 8802h	MTU2	Timer I/O control register	TIOR	8	8	2 to 3 PCLK*8
0008 8804h	MTU2	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK*8
0008 8805h	MTU2	Timer status register	TSR	8	8	2 to 3 PCLK*8
0008 8806h	MTU2	Timer counter	TCNT	16	16	2 to 3 PCLK*8
0008 8808h	MTU2	Timer general register A	TGRA	16	16	2 to 3 PCLK*8
0008 880Ah	MTU2	Timer general register B	TGRB	16	16	2 to 3 PCLK*8
0008 8880h	MTU5	Timer counter U	TCNTU	16	16	2 to 3 PCLK*8
0008 8882h	MTU5	Timer general register U	TGRU	16	16	2 to 3 PCLK*8
0008 8884h	MTU5	Timer control register U	TCRU	8	8	2 to 3 PCLK*8
0008 8886h	MTU5	Timer I/O control register U	TIORU	8	8	2 to 3 PCLK*8
0008 8890h	MTU5	Timer counter V	TCNTV	16	16	2 to 3 PCLK*8
0008 8892h	MTU5	Timer general register V	TGRV	16	16	2 to 3 PCLK*8
0008 8894h	MTU5	Timer control register V	TCRV	8	8	2 to 3 PCLK*8
0008 8896h	MTU5	Timer I/O control register V	TIORV	8	8	2 to 3 PCLK*8
0008 88A0h	MTU5	Timer counter W	TCNTW	16	16	2 to 3 PCLK*8
0008 88A2h	MTU5	Timer general register W	TGRW	16	16	2 to 3 PCLK*8
0008 88A4h	MTU5	Timer control register W	TCRW	8	8	2 to 3 PCLK*8
0008 88A6h	MTU5	Timer I/O control register W	TIORW	8	8	2 to 3 PCLK*8
0008 88B2h	MTU5	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK*8
0008 88B4h	MTU5	Timer start register	TSTR	8	8	2 to 3 PCLK*8
0008 88B6h	MTU5	Timer compare match clear register	TCNTCMPCLR	8	8	2 to 3 PCLK*8
0008 8900h	POE	Input level control/status register 1	ICSR1	16	16	2 to 3 PCLK*8
0008 8902h	POE	Output level control/status register 1	OCSR1	16	16	2 to 3 PCLK*8
0008 8904h	POE	Input level control/status register 2	ICSR2	16	16	2 to 3 PCLK*8
0008 8906h	POE	Output level control/status register 2	OCSR2	16	16	2 to 3 PCLK*8
0008 8908h	POE	Input level control/status register 3	ICSR3	16	16	2 to 3 PCLK*8
0008 890Ah	POE	Software port output enable register	SPOER	8	8	2 to 3 PCLK*8
0008 890Bh	POE	Port output enable control register 1	POECR1	8	8	2 to 3 PCLK*8
0008 890Ch	POE	Port output enable control register 2	POECR2	16	16	2 to 3 PCLK*8
0008 890Eh	POE	Input level control/status register 4	ICSR4	16	16	2 to 3 PCLK*8
0008 8A00h	MTU9	Timer control register	TCR	8	8	2 to 3 PCLK*8

Table 4.1 List of I/O Registers (Address Order) (23 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 8A01h	MTU10	Timer control register	TCR	8	8	2 to 3 PCLK*8
0008 8A02h	MTU9	Timer mode register	TMDR	8	8	2 to 3 PCLK*8
0008 8A03h	MTU10	Timer mode register	TMDR	8	8	2 to 3 PCLK*8
0008 8A04h	MTU9	Timer I/O control register H	TIORH	8	8	2 to 3 PCLK*8
0008 8A05h	MTU9	Timer I/O control register L	TIORL	8	8	2 to 3 PCLK*8
0008 8A06h	MTU10	Timer I/O control register H	TIORH	8	8	2 to 3 PCLK*8
0008 8A07h	MTU10	Timer I/O control register L	TIORL	8	8	2 to 3 PCLK*8
0008 8A08h	MTU9	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK*8
0008 8A09h	MTU10	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK*8
0008 8A0Ah	MTUB	Timer output master enable register	TOER	8	8	2 to 3 PCLK*8
0008 8A0Dh	MTUB	Timer gate control register	TGCR	8	8	2 to 3 PCLK*8
0008 8A0Eh	MTUB	Timer output control register 1	TOCR1	8	8	2 to 3 PCLK*8
0008 8A0Fh	MTUB	Timer output control register 2	TOCR2	8	8	2 to 3 PCLK*8
0008 8A10h	MTU9	Timer counter	TCNT	16	16	2 to 3 PCLK*8
0008 8A12h	MTU10	Timer counter	TCNT	16	16	2 to 3 PCLK*8
0008 8A14h	MTUB	Timer cycle data register	TCDR	16	16	2 to 3 PCLK*8
0008 8A16h	MTUB	Timer dead time data register	TDDR	16	16	2 to 3 PCLK*8
0008 8A18h	MTU9	Timer general register A	TGRA	16	16	2 to 3 PCLK*8
0008 8A1Ah	MTU9	Timer general register B	TGRB	16	16	2 to 3 PCLK*8
0008 8A1Ch	MTU10	Timer general register A	TGRA	16	16	2 to 3 PCLK*8
0008 8A1Eh	MTU10	Timer general register B	TGRB	16	16	2 to 3 PCLK*8
0008 8A20h	MTUB	Timer subcounter	TCNTS	16	16	2 to 3 PCLK*8
0008 8A22h	MTUB	MTUB Timer cycle buffer register	TCBR	16	16	2 to 3 PCLK*8
0008 8A24h	MTU9	Timer general register C	TGRC	16	16	2 to 3 PCLK*8
0008 8A26h	MTU9	Timer general register D	TGRD	16	16	2 to 3 PCLK*8
0008 8A28h	MTU10	Timer general register C	TGRC	16	16	2 to 3 PCLK*8
0008 8A2Ah	MTU10	Timer general register D	TGRD	16	16	2 to 3 PCLK*8
0008 8A2Ch	MTU9	Timer status register	TSR	8	8	2 to 3 PCLK*8
0008 8A2Dh	MTU10	Timer status register	TSR	8	8	2 to 3 PCLK*8
0008 8A30h	MTUB	Timer interrupt skipping set register	TITCR	8	8	2 to 3 PCLK*8
0008 8A31h	MTUB	Timer interrupt skipping counter	TITCNT	8	8	2 to 3 PCLK*8
0008 8A32h	MTUB	TUB Timer dead time enable register	TBTER	8	8	2 to 3 PCLK*8
0008 8A34h	MTUB	Timer dead time enable register	TDER	8	8	2 to 3 PCLK*8
0008 8A36h	MTUB	Timer output level buffer register	TOLBR	8	8	2 to 3 PCLK*8
0008 8A38h	MTU9	Timer buffer operation transfer mode register	TBTM	8	8	2 to 3 PCLK*8
0008 8A39h	MTU10	Timer buffer operation transfer mode register	TBTM	8	8	2 to 3 PCLK*8
0008 8A40h	MTU10	Timer A/D converter start request control register	TADCR	16	16	2 to 3 PCLK*8
0008 8A44h	MTU10	Timer A/D converter start request cycle set register A	TADCORA	16	16	2 to 3 PCLK*8
0008 8A46h	MTU10	Timer A/D converter start request cycle set register B	TADCORB	16	16	2 to 3 PCLK*8
0008 8A48h	MTU10	Timer A/D converter start request cycle set buffer register A	TADCOBRA	16	16	2 to 3 PCLK*8

Table 4.1 List of I/O Registers (Address Order) (30 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000A 0008h	USB0	Device state control register 0	DVSTCTR0	16	16	at least 9 PCLK*9
000A 0014h	USB0	CFIFO port register	CFIFO	16	8, 16	3 to 4 PCLK*8
000A 0018h	USB0	D0FIFO port register	D0FIFO	16	8, 16	3 to 4 PCLK*8
000A 001Ch	USB0	D1FIFO port register	D1FIFO	16	8, 16	3 to 4 PCLK*8
000A 0020h	USB0	CFIFO port select register	CFIFOSEL	16	16	3 to 4 PCLK*8
000A 0022h	USB0	CFIFO port control register	CFIFOCTR	16	16	3 to 4 PCLK*8
000A 0028h	USB0	D0FIFO port select register	D0FIFOSEL	16	16	3 to 4 PCLK*8
000A 002Ah	USB0	D0FIFO port control register	D0FIFOCTR	16	16	3 to 4 PCLK*8
000A 002Ch	USB0	D1FIFO port select register	D1FIFOSEL	16	16	3 to 4 PCLK*8
000A 002Eh	USB0	D1FIFO port control register	D1FIFOCTR	16	16	3 to 4 PCLK*8
000A 0030h	USB0	Interrupt enable register 0	INTENB0	16	16	at least 9 PCLK*9
000A 0032h	USB0	Interrupt enable register 1	INTENB1	16	16	at least 9 PCLK*9
000A 0036h	USB0	BRDY interrupt enable register	BRDYENB	16	16	at least 9 PCLK*9
000A 0038h	USB0	NRDY interrupt enable register	NRDYENB	16	16	at least 9 PCLK*9
000A 003Ah	USB0	BEMP interrupt enable register	BEMPENB	16	16	at least 9 PCLK*9
000A 003Ch	USB0	SOF output configuration register	SOFCFG	16	16	at least 9 PCLK*9
000A 0040h	USB0	Interrupt status register 0	INTSTS0	16	16	at least 9 PCLK*9
000A 0042h	USB0	Interrupt status register 1	INTSTS1	16	16	at least 9 PCLK*9
000A 0046h	USB0	BRDY interrupt enable register	BRDYSTS	16	16	at least 9 PCLK*9
000A 0048h	USB0	NRDY interrupt status register	NRDYSTS	16	16	at least 9 PCLK*9
000A 004Ah	USB0	BEMP interrupt status register	BEMPSTS	16	16	at least 9 PCLK*9
000A 004Ch	USB0	Frame number register	FRMNUM	16	16	at least 9 PCLK*9
000A 004Eh	USB0	Device state change register	DVCHGR	16	16	at least 9 PCLK*9
000A 0050h	USB0	USB address register	USBADDR	16	16	at least 9 PCLK*9
000A 0054h	USB0	USB request type register	USBREQ	16	16	at least 9 PCLK*9
000A 0056h	USB0	USB request value register	USBVAL	16	16	at least 9 PCLK*9
000A 0058h	USB0	USB request index register	USBINDX	16	16	at least 9 PCLK*9
000A 005Ah	USB0	USB request length register	USBLENG	16	16	at least 9 PCLK*9
000A 005Ch	USB0	DCP configuration register	DCPCFG	16	16	at least 9 PCLK*9
000A 005Eh	USB0	DCP maximum packet size register	DCPMAXP	16	16	at least 9 PCLK*9

Table 4.1 List of I/O Registers (Address Order) (34 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000A 029Ch	USB1	Pipe 4 transaction counter enable register	PIPE4TRE	16	16	at least 9 PCLK*9
000A 029Eh	USB1	Pipe 4 transaction counter register	PIPE4TRN	16	16	at least 9 PCLK*9
000A 02A0h	USB1	Pipe 5 transaction counter enable register	PIPE5TRE	16	16	at least 9 PCLK*9
000A 02A2h	USB1	Pipe 5 transaction counter register	PIPE5TRN	16	16	at least 9 PCLK*9
000A 02D0h	USB1	Device address 0 configuration register	DEVADD0	16	16	at least 9 PCLK*9
000A 02D2h	USB1	Device address 1 configuration register	DEVADD1	16	16	at least 9 PCLK*9
000A 02D4h	USB1	Device address 2 configuration register	DEVADD2	16	16	at least 9 PCLK*9
000A 02D6h	USB1	Device address 3 configuration register	DEVADD3	16	16	at least 9 PCLK*9
000A 02D8h	USB1	Device address 4 configuration register	DEVADD4	16	16	at least 9 PCLK*9
000A 02DAh	USB1	Device address 5 configuration register	DEVADD5	16	16	at least 9 PCLK*9
000A 0400h	USB	Deep standby USB transceiver control/ pin monitor register	DPUSR0R	32	32	1 to 2PCLK*8
000A 0404h	USB	Deep standby USB suspend/resume interrupt register	DPUSR1R	32	32	1 to 2PCLK*8
000C 0000h	EDMAC	EDMAC mode register	EDMR	32	32	4 to 5 ICLK
000C 0008h	EDMAC	EDMAC transmit request register	EDTRR	32	32	4 to 5 ICLK
000C 0010h	EDMAC	EDMAC receive request register	EDRRR	32	32	4 to 5 ICLK
000C 0018h	EDMAC	Transmit descriptor list start address register	TDLAR	32	32	4 to 5 ICLK
000C 0020h	EDMAC	Receive descriptor list start address register	RDLAR	32	32	4 to 5 ICLK
000C 0028h	EDMAC	ETHERC/EDMAC status register	EESR	32	32	4 to 5 ICLK
000C 0030h	EDMAC	ETHERC/EDMAC status interrupt permission register	EESIPR	32	32	4 to 5 ICLK
000C 0038h	EDMAC	Transmit/receive status copy enable register	TRSCER	32	32	4 to 5 ICLK
000C 0040h	EDMAC	Receive missed-frame counter register	RMFCR	32	32	4 to 5 ICLK
000C 0048h	EDMAC	Transmit FIFO threshold register	TFTR	32	32	4 to 5 ICLK
000C 0050h	EDMAC	FIFO depth register	FDR	32	32	4 to 5 ICLK
000C 0058h	EDMAC	Receiving method control register	RMCR	32	32	4 to 5 ICLK
000C 0064h	EDMAC	Transmit FIFO underrun counter	TFUCR	32	32	4 to 5 ICLK
000C 0068h	EDMAC	Receive FIFO overflow counter	RFOCR	32	32	4 to 5 ICLK
000C 006Ch	EDMAC	Independent output signal setting register	IOSR	32	32	4 to 5 ICLK
000C 0070h	EDMAC	Flow control start FIFO threshold setting register	FCFTR	32	32	4 to 5 ICLK
000C 0078h	EDMAC	Receive data padding insert register	RPADIR	32	32	4 to 5 ICLK
000C 007Ch	EDMAC	Transmit interrupt setting register	TRIMD	32	32	4 to 5 ICLK
000C 00C8h	EDMAC	Receive buffer write address register	RBWAR	32	32	4 to 5 ICLK
000C 00CCh	EDMAC	Receive descriptor fetch address register	RDFAR	32	32	4 to 5 ICLK

5.3.1 Clock Timing

Table 5.8 Clock Timing

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
T_a = -40 to +85°C

Item	Symbol	Min.	Max.	Unit	Test Conditions
BCLK pin output cycle time [176-pin LFBGA/145-pin TFLGA/144-pin LQFP]	t_{Bcyc}	20	125	ns	Figure 5.1
BCLK pin output cycle time [100-pin LQFP/85-pin TFLGA]	t_{Bcyc}	40	125	ns	
BCLK pin output high pulse width	t_{CH}	5	—	ns	
BCLK pin output low pulse width	t_{CL}	5	—	ns	
BCLK pin output rising time	t_{Cr}	—	5	ns	
BCLK pin output falling time	t_{Cf}	—	5	ns	
SDCLK pin output cycle time	t_{SDcyc}	20	125	ns	
SDCLK pin output high pulse width	t_{CH}	5	—	ns	
SDCLK pin output low pulse width	t_{CL}	5	—	ns	
SDCLK pin output rising time	t_{Cr}	—	5	ns	
SDCLK pin output falling time	t_{Cf}	—	5	ns	
Oscillation settling time after reset (crystal)	t_{OSC1}	10	—	ms	Figure 5.2
Oscillation settling time after leaving software standby mode (crystal)	t_{OSC2}	10	—	ms	Figure 5.3
Oscillation settling time after leaving deep software standby mode (crystal)	t_{OSC3}	10	—	ms	Figure 5.4
EXTAL external clock output delay settling time	t_{DEXT}	1	—	ms	Figure 5.2
EXTAL external clock input low pulse width	t_{EXL}	30.71	—	ns	Figure 5.5
EXTAL external clock input high pulse width	t_{EXH}	30.71	—	ns	
EXTAL external clock rising time	t_{EXr}	—	5	ns	
EXTAL external clock falling time	t_{EXf}	—	5	ns	
XCIN sub-clock oscillation settling time	t_{SUBOSC}	2	—	s	Figure 5.6
XCIN sub-clock oscillation frequency	f_{SUB}	32.768	—	kHz	
On-chip oscillator (IWDTCLK) oscillation frequency	$f_{IWDTCLK}$	62.5	187.5	kHz	

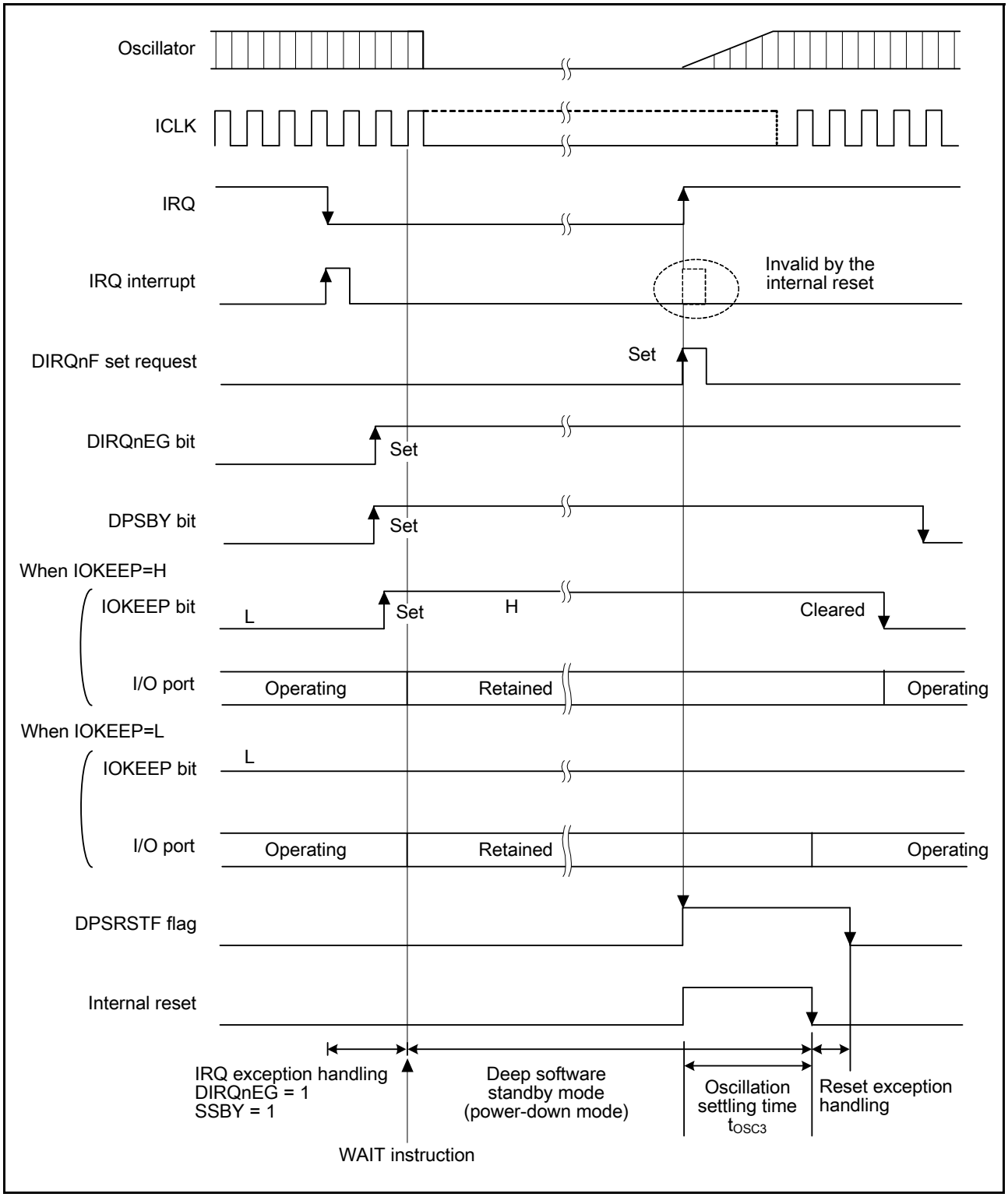
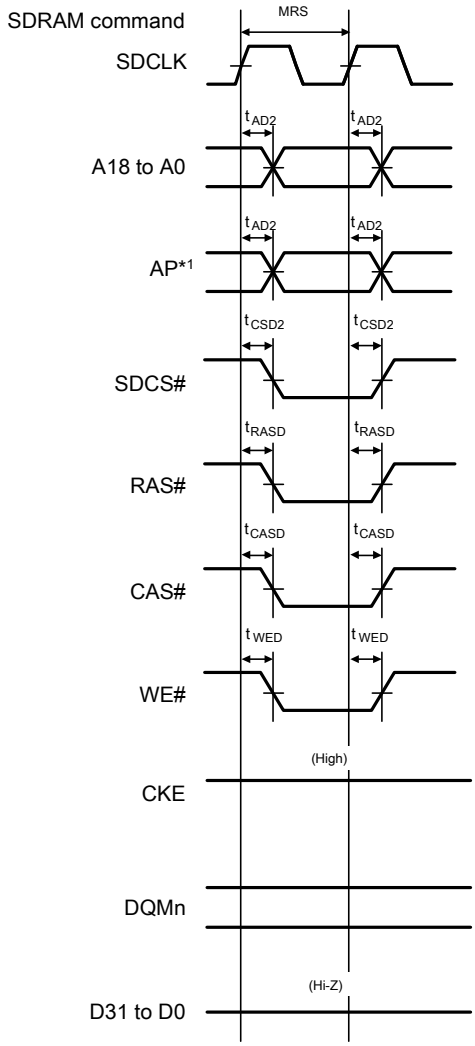


Figure 5.4 Oscillation Settling Timing after Deep Software Standby Mode



Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.20 SDRAM Space Mode Register Set Bus Timing

Table 5.18 Timing of On-Chip Peripheral Modules (10)

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
PCLK = 8 to 50 MHz
T_a = -40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
TCK clock cycle time	t_{TCKcyc}	100	—	—	ns	Figure 5.58
TCK clock high pulse width	t_{TCKH}	45	—	—	ns	
TCK clock low pulse width	t_{TCKL}	45	—	—	ns	
TCK clock rising time	t_{TCKr}	—	—	5	ns	
TCK clock falling time	t_{TCKf}	—	—	5	ns	
TRST# pulse width	t_{TRSTW}	20	—	—	t_{TCKcyc}	Figure 5.59
TMS setup time	t_{TMSS}	20	—	—	ns	Figure 5.60
TMS hold time	t_{TMSH}	20	—	—	ns	
TDI setup time	t_{TDIS}	20	—	—	ns	
TDI hold time	t_{TDIH}	20	—	—	ns	
TDO data delay time	t_{TDOD}	—	—	40	ns	

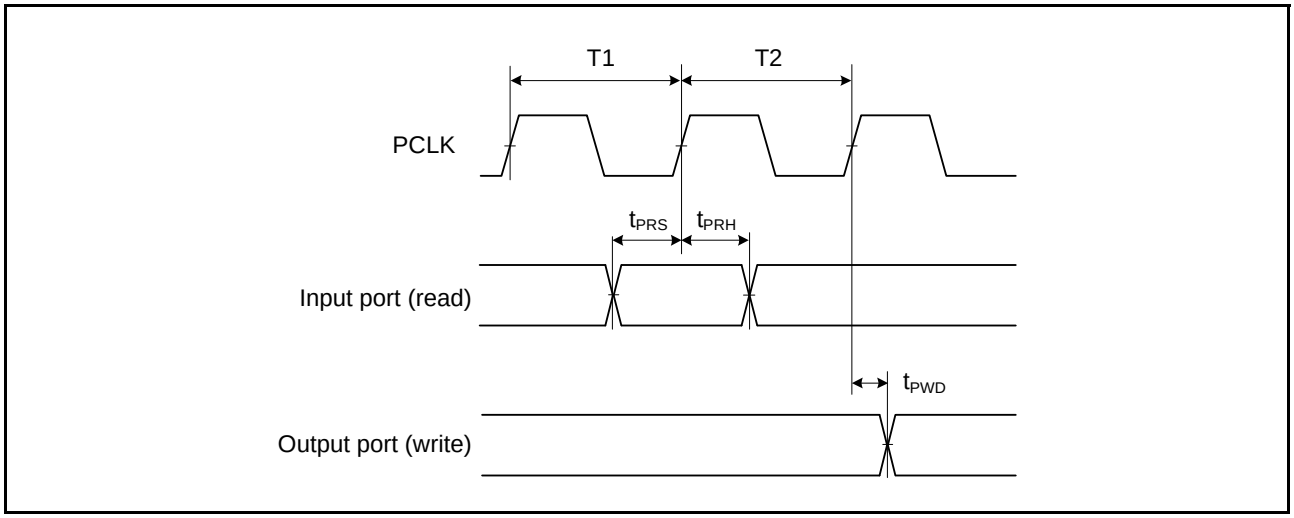


Figure 5.25 I/O Port Input/Output Timing

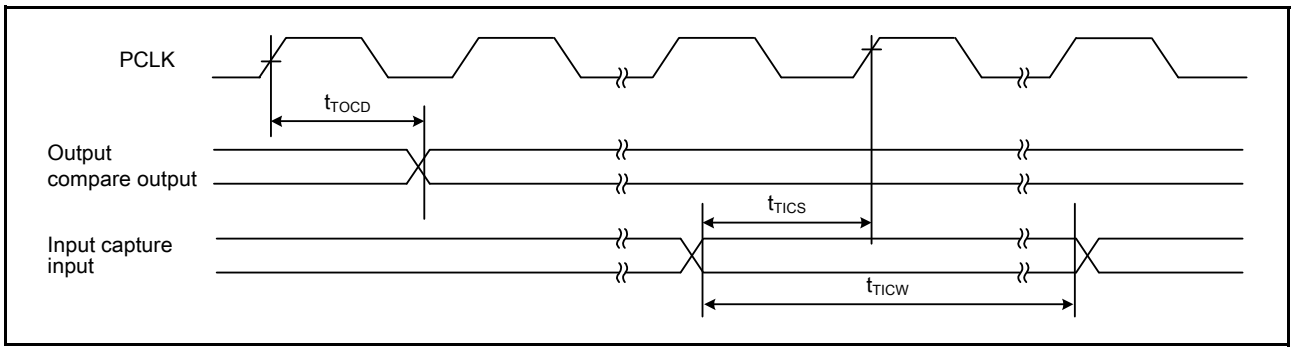


Figure 5.26 MTU2 Input/Output Timing

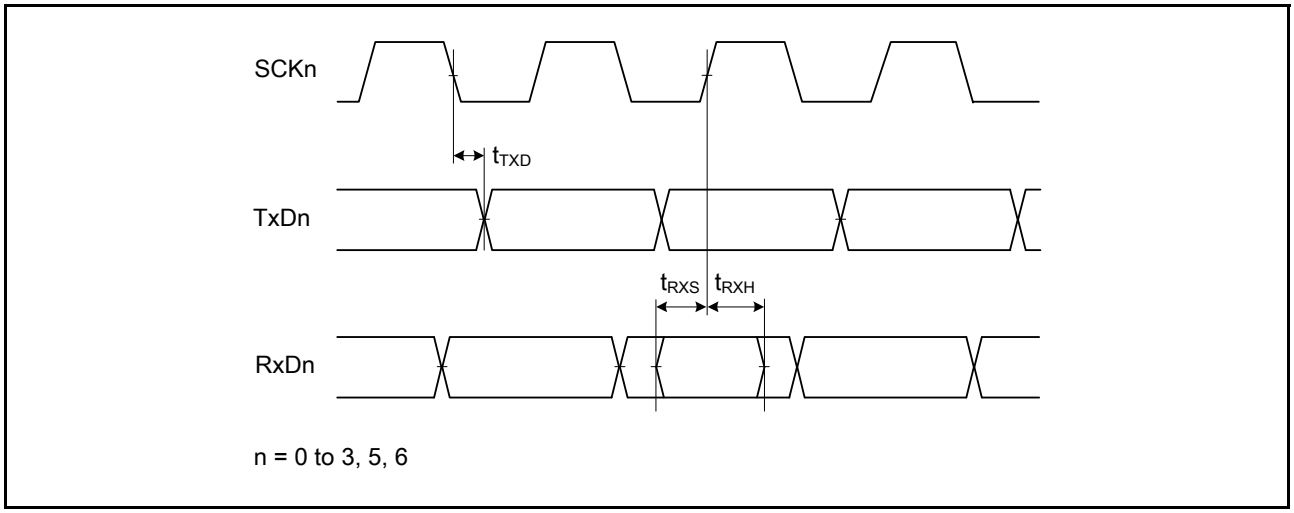


Figure 5.35 SCI Input/Output Timing: Clock Synchronous Mode

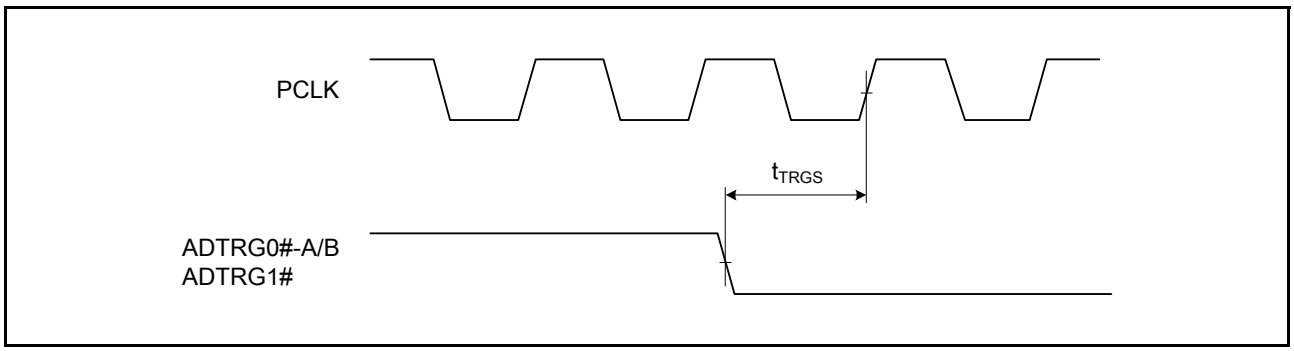


Figure 5.36 A/D Converter External Trigger Input Timing

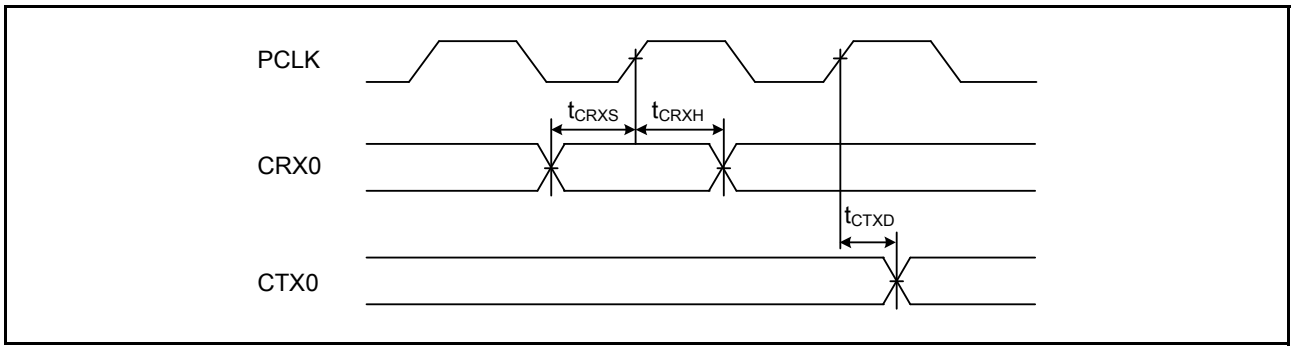


Figure 5.37 CAN Input/Output Timing

5.7 Power-on Reset Circuit, Voltage Detection Circuit Characteristics

Table 5.23 Power-on Reset Circuit, Voltage Detection Circuit Characteristics

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
T_a = -40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	2.48	2.58	2.68	V	Figure 5.63
	Voltage detection circuit (LVD)	Vdet1	2.75	2.85	2.95		Figure 5.64 and Figure 5.65
		Vdet2	3.05	3.15	3.25		
Internal reset time		t_{POR}	20	35	50	ms	
Min. VCC down time*1		t_{VOFF}	200	—	—	µs	Figure 5.64 and Figure 5.65
Reply delay time		tdet	—	—	200	µs	

Note 1. The power-off time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, Vdet1, and Vdet2 for the POR/ LVD.

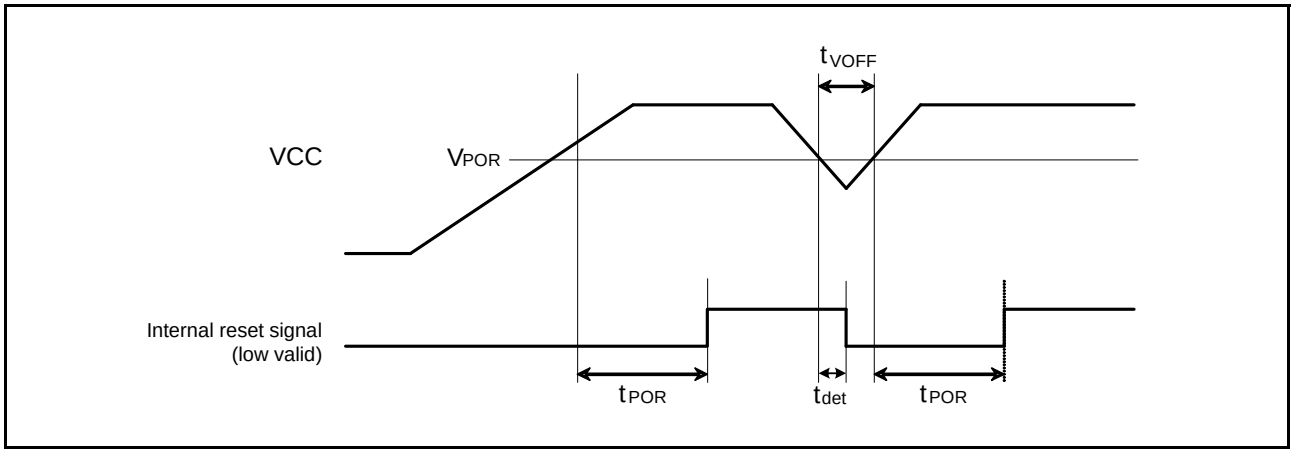


Figure 5.63 Power-on Reset Timing

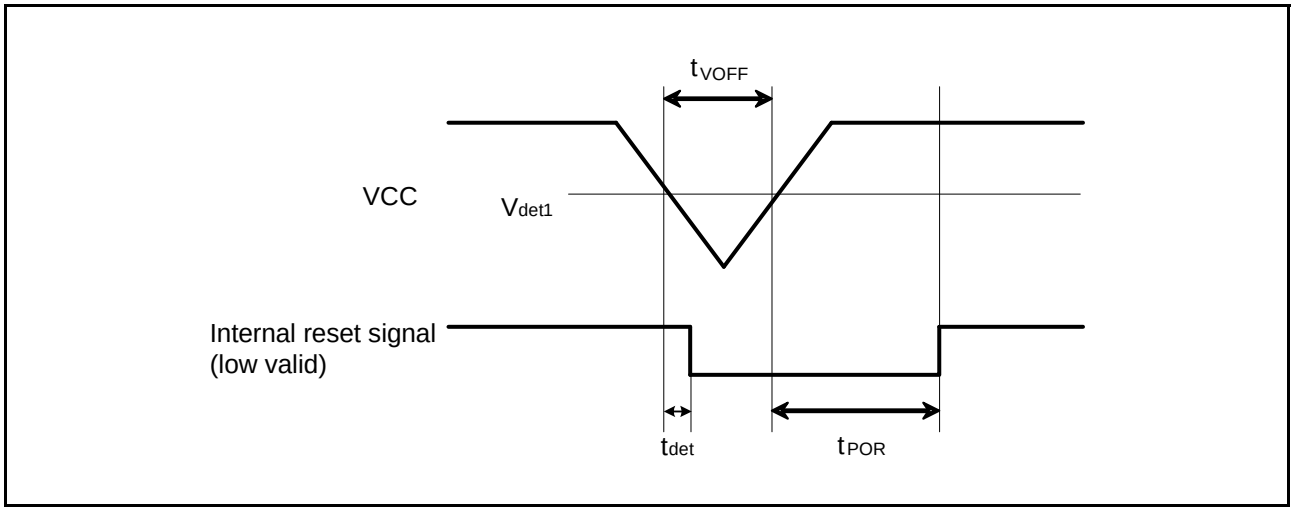


Figure 5.64 Voltage Detection Circuit Timing (Vdet1)

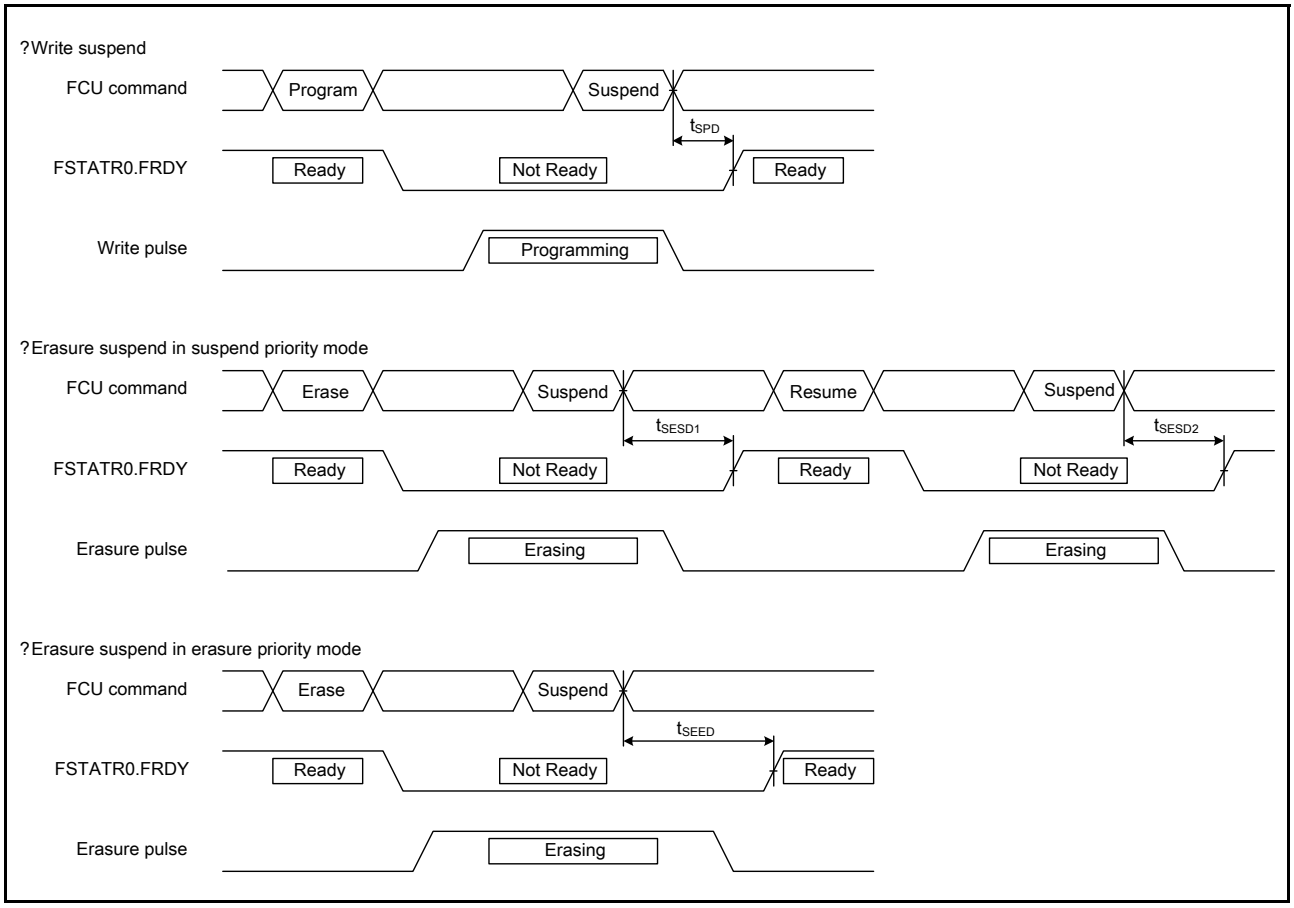
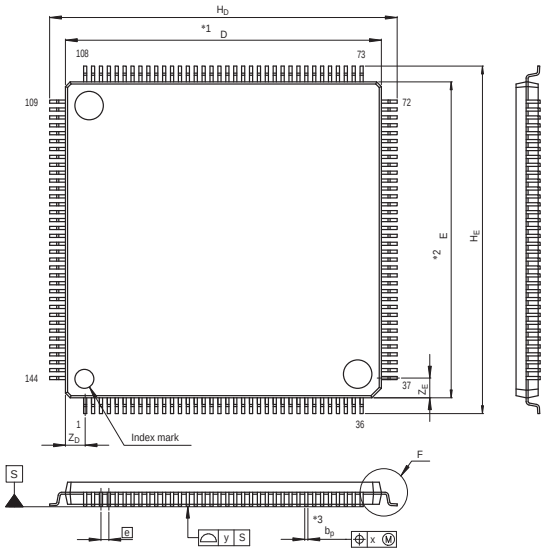
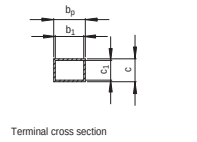
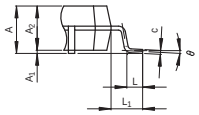


Figure 5.67 Flash Memory Write/Erase Suspend Timing

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP144-20x20-0.50	PLQP0144KA-A	144P6Q-A / FP-144L / FP-144LV	1.2g





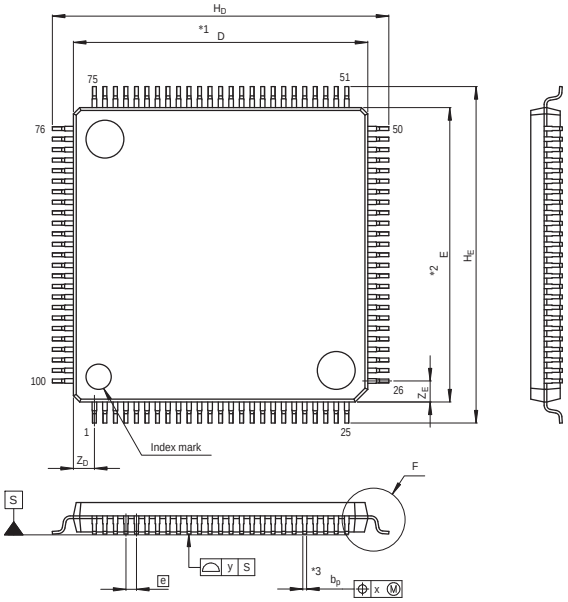


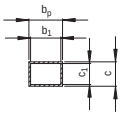
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

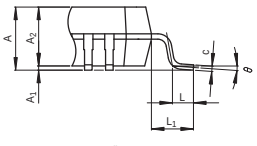
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure C 144-Pin LQFP (PLQP0144KA-A) Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g







NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure D 100-Pin LQFP (PLQP0100KB-A) Package Dimensions