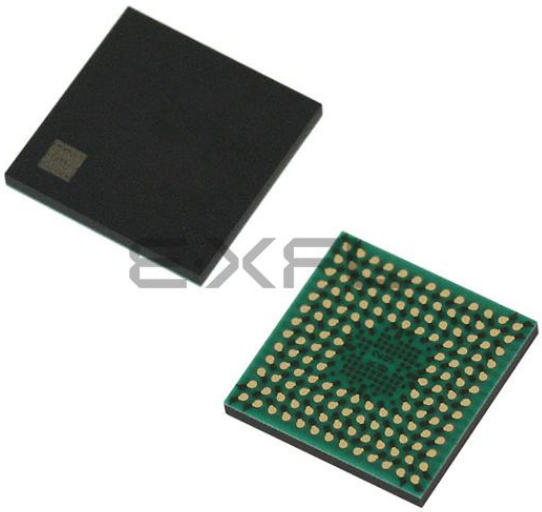
# Renesas Electronics America Inc - R5F56217BDLE#U0 Datasheet



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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | RX |
| Core Size | 32-Bit Single-Core |
| Speed | 100MHz |
| Connectivity | CANbus, EBI/EMI, I²C, SCI, SPI, USB |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 103 |
| Program Memory Size | 384KB (384K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 64K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | A/D 8x10/12b; D/A 2x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 145-TFLGA |
| Supplier Device Package | 145-TFLGA (9x9) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f56217bdle-u0 |

# 1. Overview

## 1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 lists the functions of products.

**Table 1.1 Outline of Specifications (1 / 4)**

| Classification | Module/Function | Description |
|---|---|---|
| CPU | CPU | ・ Maximum operating frequency: 100 MHz<br>・ 32-bit RX CPU<br>・ Minimum instruction execution time: One instruction per state (cycle of the system clock)<br>・ Address space: 4-Gbyte linear<br>・ Register set of the CPU<br>General purpose: Sixteen 32-bit registers<br>Control: Nine 32-bit registers<br>Accumulator: One 64-bit register<br>・ Basic instructions: 73<br>・ Floating-point instructions: 8<br>・ DSP instructions: 9<br>・ Addressing modes: 10<br>・ Data arrangement<br>Instructions: Little endian<br>Data: Selectable as little endian or big endian<br>・ On-chip 32-bit multiplier: 32 x 32 → 64 bits<br>・ On-chip divider: 32 / 32 → 32 bits<br>・ Barrel shifter: 32 bits<br>・ Memory-protection unit (MPU) |
| | FPU | ・ Single precision (32-bit) floating point<br>・ Data types and floating-point exceptions in conformance with the IEEE754 standard |
| Memory | ROM | ・ ROM capacity: 512 Kbytes (max.)<br>・ Two on-board programming modes<br>Boot mode (The user MAT is programmable via the SCI and USB.)<br>User program mode<br>・ Parallel programmer mode (for off-board programming) |
| | RAM | RAM capacity: 96 Kbytes (max.) |
| | Data flash | Data flash capacity: 32 Kbytes |
| MCU operating modes | | ・ Single-chip mode, on-chip ROM enabled expansion mode, and on-chip ROM disabled expansion mode (software switching) |
| Clock | Clock generation circuit | ・ Two circuits: Main clock oscillator and subclock oscillator<br>・ Internal oscillator: Low-speed on-chip oscillator<br>・ Structure of a PLL frequency synthesizer and frequency divider for selectable operating frequency<br>・ Oscillation stoppage detection<br>・ Independent frequency-division and multiplication settings for the system clock (ICLK), peripheral module clock (PCLK), and external bus clock (BCLK)<br>The CPU and other bus masters run in synchronization with the system clock (ICLK): 8 to 100 MHz<br>Peripheral modules run in synchronization with the peripheral module clock (PCLK): 8 to 50 MHz<br>・ Devices connected to the external bus run in synchronization with the external bus clock (BCLK pin): 8 to 50 MHz*1 |
| Reset | | ・ Pin reset, power-on reset, voltage-monitoring reset, watchdog timer reset, independent watchdog timer reset, and deep software standby reset |
| Voltage detection circuit | | ・ When the voltage on VCC falls below the voltage detection level (Vdet), an internal reset or internal interrupt is generated. |
| Low power consumption | Low power consumption facilities | ・ Module stop function<br>・ Four low power consumption modes<br>Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode |

**Table 1.2 Functions of RX62N Group and RX621 Group Products**

| Functions | | RX62N Group | | | | | | | | RX621 Group | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | R5F562NxBxxx* | | | | R5F562NxAxxx* | | | | R5F5621xBxxx* | | | | |
| Package | | 176-pin LFBGA | 145-pin TFLGA | 144-pin LQFP | 100-pin LQFP | 176-pin LFBGA | 145-pin TFLGA | 144-pin LQFP | 100-pin LQFP | 176-pin LFBGA | 145-pin TFLGA | 144-pin LQFP | 100-pin LQFP | 85-pin TFLGA |
| External bus | SDRAM area controller | O | | | — | O | | | — | O | | | — | |
| DMA | DMA controller | O | | | | O | | | | O | | | | |
| | EXDMA controller | O | | | — | O | | | — | O | | | — | |
| | Data transfer controller | O | | | | O | | | | O | | | | |
| Timers | Multi-function timer pulse unit | O | | | | O | | | | O | | | | |
| | Port output enable | O | | | | O | | | | O | | | | — |
| | Programmable pulse generator | O | | | | O | | | | O | | | | |
| | 8-bit timers | O | | | | O | | | | O | | | | |
| | Compare match timer | O | | | | O | | | | O | | | | |
| | Realtime clock | O | | | | O | | | | O | | | | |
| | Watchdog timer | O | | | | O | | | | O | | | | |
| | Independent watchdog timer | O | | | | O | | | | O | | | | |
| Communication function | Ethernet controller/ DMA controller for Ethernet controller | O | | | | O | | | | — | | | | |
| | USB 2.0 host/function module | O | | | | O | | | | O | | | | |
| | Serial communications interfaces | O | | | | O | | | | O | | | | |
| | $I^2C$ bus interfaces | O | | | | O | | | | O | | | | |
| | CAN module | O | | | | — | | | | O | | | | |
| | Serial peripheral interfaces | O | | | | O | | | | O | | | | |
| A/D converter | | O | | | | O | | | | O | | | | |
| D/A converter | | O | | | | O | | | | O | | | | |
| CRC calculator | | O | | | | O | | | | O | | | | |

[Legend]
O: Supported, —: Not supported
Note: * For details on part numbers, see Table 1.3.

**Table 1.7 List of Pins and Pin Functions (100-Pin LQFP) (4 / 4)**

| Pin No. 100-Pin LQFP | Power Supply Clock System Control | I/O Port | External Bus | ETHERC EDMAC | USB | Timers (MTU, TMR, PPG, POE) | Communi-cation (SCI, CAN, RSPI, RIIC) | Others |
|---|---|---|---|---|---|---|---|---|
| 80 | | PD6 | D6 | | | MTIC5V/ POE1# | | |
| 81 | | PD5 | D5 | | | MTIC5W/ POE2# | | |
| 82 | | PD4 | D4 | | | MTIC11U-B/ POE3# | | |
| 83 | | PD3 | D3 | | | MTIC11V-B/ POE4# | | |
| 84 | | PD2 | D2 | | | MTIC11W-B/ POE5# | | |
| 85 | | PD1 | D1 | | | POE6# | | |
| 86 | | PD0 | D0 | | | POE7# | | |
| 87 | | P47 | | | | | | IRQ15-B/AN7 |
| 88 | | P46 | | | | | | IRQ14/AN6 |
| 89 | | P45 | | | | | | IRQ13-B/AN5 |
| 90 | | P44 | | | | | | IRQ12/AN4 |
| 91 | | P43 | | | | | | IRQ11/AN3 |
| 92 | | P42 | | | | | | IRQ10/AN2 |
| 93 | | P41 | | | | | | IRQ9/AN1 |
| 94 | VREFL | | | | | | | |
| 95 | | P40 | | | | | | IRQ8/AN0 |
| 96 | VREFH | | | | | | | |
| 97 | AVCC | | | | | | | |
| 98 | | P07 | | | | | | IRQ15-A/ ADTRG0#-A |
| 99 | AVSS | | | | | | | |
| 100 | | P05 | | | | | | DA1/IRQ13-A |

## 1.5 Pin Functions

Table 1.8 lists the pin functions.

**Table 1.9 Pin Functions (1 / 7)**

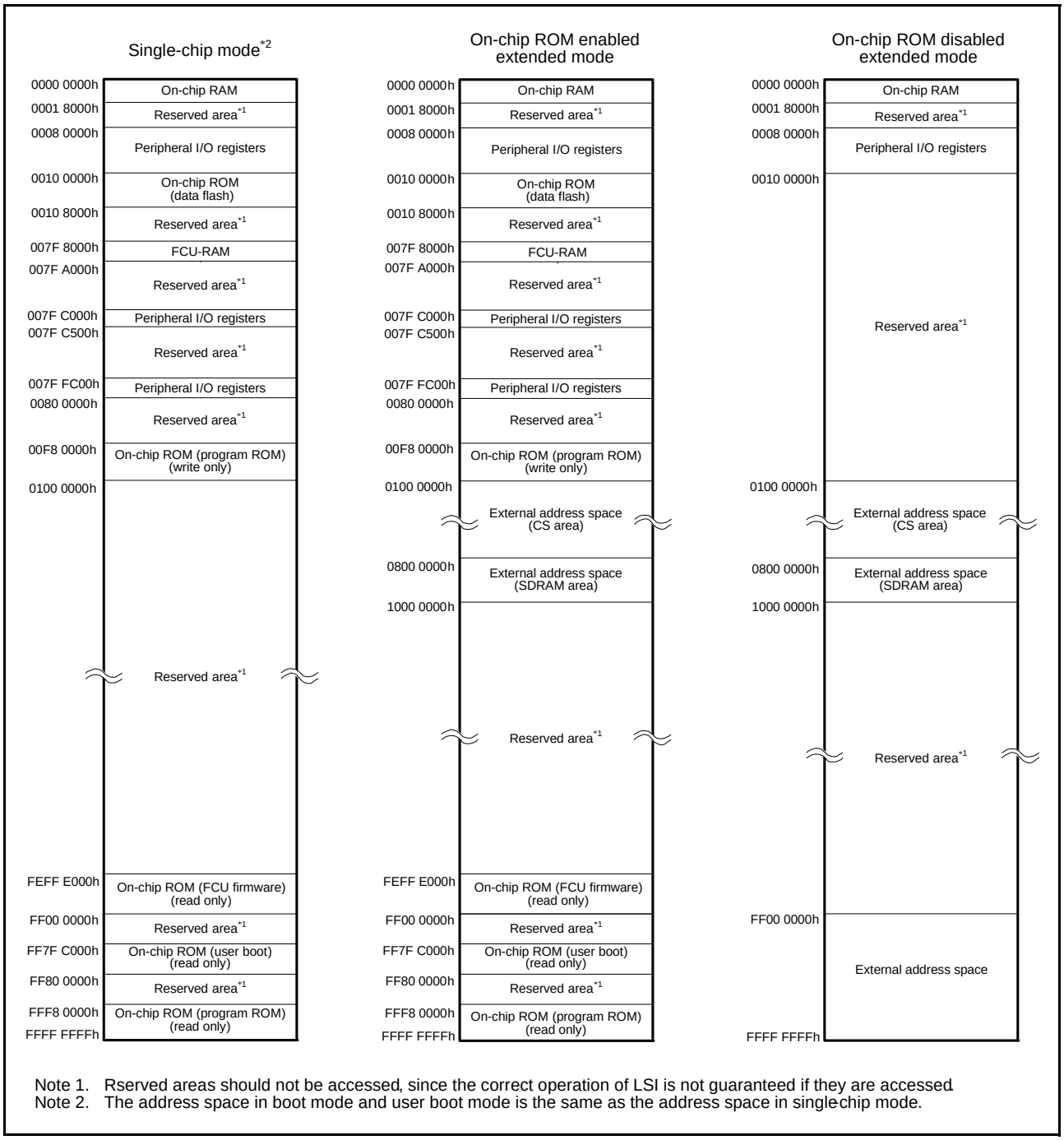
| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| Power supply | VCC | Input | Power supply pin. Connect it to the system power supply. |
| | VCL | Input | Connect this pin to VSS via a 0.1-μF capacitor. The capacitor should be placed close to the pin. |
| | VSS | Input | Ground pin. Connect it to the system power supply (0 V). |
| | PLLVCC | Input | Power supply pin for the PLL circuit. Connect it to the system power supply. |
| | PLLVSS | Input | Ground pin for the PLL circuit. |
| Clock | XTAL | Output | Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin. |
| | EXTAL | Input | |
| | BCLK | Output | Outputs the external bus clock for external devices. |
| | SDCLK | Output | Outputs the clock dedicated for the SDRAM. |
| | XCOUT | Output | Input/output pins for the subclock generation circuit. Connect a crystal resonator between XCOUT and XCIN. |
| | XCIN | Input | |
| Operating mode control | MD0, MD1, MDE | Input | Pins for setting the operating mode. The signal levels on these pins must not be changed during operation. |
| System control | RES# | Input | Reset signal input pin. This LSI enters the reset state when this signal goes low. |
| | EMLE | Input | Input pin to enable the connection of the on-chip emulator signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low. |
| | BSCANP | Input | Boundary scan pin. Boundary scan is enabled when this pin goes high. When not used, it should be driven low. |
| CNVSS | CNVSS | Input | Connect this pin to VSS via pull-down resister. |
| On-chip emulator | TRST# | Input | On-chip emulator pins or boundary scan pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator. |
| | TMS | Input | |
| | TDI | Input | |
| | TCK | Input | |
| | TDO | Output | |
| | TRCLK | Output | This pin outputs the clock for synchronization with the trace data. |
| | TRSYNC | Output | This pin indicates that output from the TRDATA0 to TRDATA3 pins is valid. |
| | TRDATA0-A/TRDATA3-B | Output | These pins output the trace information. |
| Address bus | A0 to A15<br>A16-A/A16-B to<br>A23-A/A23-B | Output | Output pins for the address. |
| Data bus | D0 to D31 | I/O | Input and output pins for the bidirectional data bus. |

# 3. Address Space

## 3.1 Address Space

This LSI has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.

Figure 3.1 shows the memory maps in the respective operating modes. Accessible areas will differ according to the operating mode and states of control bits.




Note 1. Rserved areas should not be accessed, since the correct operation of LSI is not guaranteed if they are accessed.
Note 2. The address space in boot mode and user boot mode is the same as the address space in single-chip mode.

**Figure 3.1 Memory Map in Each Operating Mode**

**Table 4.1 List of I/O Registers (Address Order) (2 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 208Ch | DMAC2 | DMA block transfer count register | DMCRB | 16 | 16 | 2 ICLK |
| 0008 2090h | DMAC2 | DMA transfer mode register | DMTMD | 16 | 16 | 2 ICLK |
| 0008 2093h | DMAC2 | DMA interrupt setting register | DMINT | 8 | 8 | 2 ICLK |
| 0008 2094h | DMAC2 | DMA address mode register | DMAMD | 16 | 16 | 2 ICLK |
| 0008 209Ch | DMAC2 | DMA transfer enable register | DMCNT | 8 | 8 | 2 ICLK |
| 0008 209Dh | DMAC2 | DMA software start register | DMREQ | 8 | 8 | 2 ICLK |
| 0008 209Eh | DMAC2 | DMA status register | DMSTS | 8 | 8 | 2 ICLK |
| 0008 209Fh | DMAC2 | DMA activation source flag control register | DMCSL | 8 | 8 | 2 ICLK |
| 0008 20C0h | DMAC3 | DMA source address register | DMSAR | 32 | 32 | 2 ICLK |
| 0008 20C4h | DMAC3 | DMA destination address register | DMDAR | 32 | 32 | 2 ICLK |
| 0008 20C8h | DMAC3 | DMA transfer count register | DMCRA | 32 | 32 | 2 ICLK |
| 0008 20CCh | DMAC3 | DMA block transfer count register | DMCRB | 16 | 16 | 2 ICLK |
| 0008 20D0h | DMAC3 | DMA transfer mode register | DMTMD | 16 | 16 | 2 ICLK |
| 0008 20D3h | DMAC3 | DMA interrupt setting register | DMINT | 8 | 8 | 2 ICLK |
| 0008 20D4h | DMAC3 | DMA address mode register | DMAMD | 16 | 16 | 2 ICLK |
| 0008 20DCh | DMAC3 | DMA transfer enable register | DMCNT | 8 | 8 | 2 ICLK |
| 0008 20DDh | DMAC3 | DMA software start register | DMREQ | 8 | 8 | 2 ICLK |
| 0008 20DEh | DMAC3 | DMA status register | DMSTS | 8 | 8 | 2 ICLK |
| 0008 20DFh | DMAC3 | DMA activation source flag control register | DMCSL | 8 | 8 | 2 ICLK |
| 0008 2200h | DMAC | DMACA start register | DMAST | 8 | 8 | 2 ICLK |
| 0008 2400h | DTC | DTC control register | DTCCR | 8 | 8 | 2 ICLK |
| 0008 2404h | DTC | DTC vector base register | DTCVBR | 32 | 32 | 2 ICLK |
| 0008 2408h | DTC | DTC address mode register | DTCADMOD | 8 | 8 | 2 ICLK |
| 0008 240Ch | DTC | DTC module start register | DTCST | 8 | 8 | 2 ICLK |
| 0008 240Eh | DTC | DTC status register | DTCSTS | 16 | 16 | 2 ICLK |
| 0008 2800h | EXDMAC0 | EXDMA source address register | EDMSAR | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 2804h | EXDMAC0 | EXDMA destination address register | EDMDAR | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 2808h | EXDMAC0 | EXDMA transfer count register | EDMCRA | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 280Ch | EXDMAC0 | EXDMA block transfer count register | EDMCRB | 16 | 16 | 1 to 2 BCLK*8 |
| 0008 2810h | EXDMAC0 | EXDMA transfer mode register | EDMTMD | 16 | 16 | 1 to 2 BCLK*8 |
| 0008 2812h | EXDMAC0 | EXDMA output setting register | EDMOMD | 8 | 8 | 1 to 2 BCLK*8 |
| 0008 2813h | EXDMAC0 | EXDMA interrupt setting register | EDMINT | 8 | 8 | 1 to 2 BCLK*8 |
| 0008 2814h | EXDMAC0 | EXDMA address mode register | EDMAMD | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 2818h | EXDMAC0 | EXDMA output setting register | EDMOFR | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 281Ch | EXDMAC0 | EXDMA transfer enable register | EDMCNT | 8 | 8 | 1 to 2 BCLK*8 |
| 0008 281Dh | EXDMAC0 | EXDMA software start register | EDMREQ | 8 | 8 | 1 to 2 BCLK*8 |
| 0008 281Eh | EXDMAC0 | EXDMA status register | EDMSTS | 8 | 8 | 1 to 2 BCLK*8 |
| 0008 2820h | EXDMAC0 | EXDMA external request sense mode register | EDMRMD | 8 | 8 | 1 to 2 BCLK*8 |
| 0008 2821h | EXDMAC0 | EXDMA external request flag register | EDMERF | 8 | 8 | 1 to 2 BCLK*8 |
| 0008 2822h | EXDMAC0 | EXDMA peripheral request flag register | EDMPRF | 8 | 8 | 1 to 2 BCLK*8 |
| 0008 2840h | EXDMAC1 | EXDMA source address register | EDMSAR | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 2844h | EXDMAC1 | EXDMA destination address register | EDMDAR | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 2848h | EXDMAC1 | EXDMA transfer count register | EDMCRA | 32 | 32 | 1 to 2 BCLK*8 |

**Table 4.1 List of I/O Registers (Address Order) (6 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 7044h | ICU | Interrupt request register 068 | IR068 | 8 | 8 | 2 ICLK |
| 0008 7045h | ICU | Interrupt request register 069 | IR069 | 8 | 8 | 2 ICLK |
| 0008 7046h | ICU | Interrupt request register 070 | IR070 | 8 | 8 | 2 ICLK |
| 0008 7047h | ICU | Interrupt request register 071 | IR071 | 8 | 8 | 2 ICLK |
| 0008 7048h | ICU | Interrupt request register 072 | IR072 | 8 | 8 | 2 ICLK |
| 0008 7049h | ICU | Interrupt request register 073 | IR073 | 8 | 8 | 2 ICLK |
| 0008 704Ah | ICU | Interrupt request register 074 | IR074 | 8 | 8 | 2 ICLK |
| 0008 704Bh | ICU | Interrupt request register 075 | IR075 | 8 | 8 | 2 ICLK |
| 0008 704Ch | ICU | Interrupt request register 076 | IR076 | 8 | 8 | 2 ICLK |
| 0008 704Dh | ICU | Interrupt request register 077 | IR077 | 8 | 8 | 2 ICLK |
| 0008 704Eh | ICU | Interrupt request register 078 | IR078 | 8 | 8 | 2 ICLK |
| 0008 704Fh | ICU | Interrupt request register 079 | IR079 | 8 | 8 | 2 ICLK |
| 0008 705Ah | ICU | Interrupt request register 090 | IR090 | 8 | 8 | 2 ICLK |
| 0008 705Bh | ICU | Interrupt request register 091 | IR091 | 8 | 8 | 2 ICLK |
| 0008 705Ch | ICU | Interrupt request register 092 | IR092 | 8 | 8 | 2 ICLK |
| 0008 7060h | ICU | Interrupt request register 096 | IR096 | 8 | 8 | 2 ICLK |
| 0008 7062h | ICU | Interrupt request register 098 | IR098 | 8 | 8 | 2 ICLK |
| 0008 7063h | ICU | Interrupt request register 099 | IR099 | 8 | 8 | 2 ICLK |
| 0008 7066h | ICU | Interrupt request register 102 | IR102 | 8 | 8 | 2 ICLK |
| 0008 7072h | ICU | Interrupt request register 114 | IR114 | 8 | 8 | 2 ICLK |
| 0008 7073h | ICU | Interrupt request register 115 | IR115 | 8 | 8 | 2 ICLK |
| 0008 7074h | ICU | Interrupt request register 116 | IR116 | 8 | 8 | 2 ICLK |
| 0008 7075h | ICU | Interrupt request register 117 | IR117 | 8 | 8 | 2 ICLK |
| 0008 7076h | ICU | Interrupt request register 118 | IR118 | 8 | 8 | 2 ICLK |
| 0008 7077h | ICU | Interrupt request register 119 | IR119 | 8 | 8 | 2 ICLK |
| 0008 7078h | ICU | Interrupt request register 120 | IR120 | 8 | 8 | 2 ICLK |
| 0008 7079h | ICU | Interrupt request register 121 | IR121 | 8 | 8 | 2 ICLK |
| 0008 707Ah | ICU | Interrupt request register 122 | IR122 | 8 | 8 | 2 ICLK |
| 0008 707Bh | ICU | Interrupt request register 123 | IR123 | 8 | 8 | 2 ICLK |
| 0008 707Ch | ICU | Interrupt request register 124 | IR124 | 8 | 8 | 2 ICLK |
| 0008 707Dh | ICU | Interrupt request register 125 | IR125 | 8 | 8 | 2 ICLK |
| 0008 707Eh | ICU | Interrupt request register 126 | IR126 | 8 | 8 | 2 ICLK |
| 0008 707Fh | ICU | Interrupt request register 127 | IR127 | 8 | 8 | 2 ICLK |
| 0008 7080h | ICU | Interrupt request register 128 | IR128 | 8 | 8 | 2 ICLK |
| 0008 7081h | ICU | Interrupt request register 129 | IR129 | 8 | 8 | 2 ICLK |
| 0008 7082h | ICU | Interrupt request register 130 | IR130 | 8 | 8 | 2 ICLK |
| 0008 7083h | ICU | Interrupt request register 131 | IR131 | 8 | 8 | 2 ICLK |
| 0008 7084h | ICU | Interrupt request register 132 | IR132 | 8 | 8 | 2 ICLK |
| 0008 7085h | ICU | Interrupt request register 133 | IR133 | 8 | 8 | 2 ICLK |
| 0008 7086h | ICU | Interrupt request register 134 | IR134 | 8 | 8 | 2 ICLK |
| 0008 7087h | ICU | Interrupt request register 135 | IR135 | 8 | 8 | 2 ICLK |
| 0008 7088h | ICU | Interrupt request register 136 | IR136 | 8 | 8 | 2 ICLK |
| 0008 7089h | ICU | Interrupt request register 137 | IR137 | 8 | 8 | 2 ICLK |
| 0008 708Ah | ICU | Interrupt request register 138 | IR138 | 8 | 8 | 2 ICLK |
| 0008 708Bh | ICU | Interrupt request register 139 | IR139 | 8 | 8 | 2 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (7 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 708Ch | ICU | Interrupt request register 140 | IR140 | 8 | 8 | 2 ICLK |
| 0008 708Dh | ICU | Interrupt request register 141 | IR141 | 8 | 8 | 2 ICLK |
| 0008 708Eh | ICU | Interrupt request register 142 | IR142 | 8 | 8 | 2 ICLK |
| 0008 708Fh | ICU | Interrupt request register 143 | IR143 | 8 | 8 | 2 ICLK |
| 0008 7090h | ICU | Interrupt request register 144 | IR144 | 8 | 8 | 2 ICLK |
| 0008 7091h | ICU | Interrupt request register 145 | IR145 | 8 | 8 | 2 ICLK |
| 0008 7092h | ICU | Interrupt request register 146 | IR146 | 8 | 8 | 2 ICLK |
| 0008 7093h | ICU | Interrupt request register 147 | IR147 | 8 | 8 | 2 ICLK |
| 0008 7094h | ICU | Interrupt request register 148 | IR148 | 8 | 8 | 2 ICLK |
| 0008 7095h | ICU | Interrupt request register 149 | IR149 | 8 | 8 | 2 ICLK |
| 0008 7096h | ICU | Interrupt request register 150 | IR150 | 8 | 8 | 2 ICLK |
| 0008 7097h | ICU | Interrupt request register 151 | IR151 | 8 | 8 | 2 ICLK |
| 0008 7098h | ICU | Interrupt request register 152 | IR152 | 8 | 8 | 2 ICLK |
| 0008 7099h | ICU | Interrupt request register 153 | IR153 | 8 | 8 | 2 ICLK |
| 0008 709Ah | ICU | Interrupt request register 154 | IR154 | 8 | 8 | 2 ICLK |
| 0008 709Bh | ICU | Interrupt request register 155 | IR155 | 8 | 8 | 2 ICLK |
| 0008 709Ch | ICU | Interrupt request register 156 | IR156 | 8 | 8 | 2 ICLK |
| 0008 709Dh | ICU | Interrupt request register 157 | IR157 | 8 | 8 | 2 ICLK |
| 0008 709Eh | ICU | Interrupt request register 158 | IR158 | 8 | 8 | 2 ICLK |
| 0008 709Fh | ICU | Interrupt request register 159 | IR159 | 8 | 8 | 2 ICLK |
| 0008 70A0h | ICU | Interrupt request register 160 | IR160 | 8 | 8 | 2 ICLK |
| 0008 70A1h | ICU | Interrupt request register 161 | IR161 | 8 | 8 | 2 ICLK |
| 0008 70A2h | ICU | Interrupt request register 162 | IR162 | 8 | 8 | 2 ICLK |
| 0008 70A3h | ICU | Interrupt request register 163 | IR163 | 8 | 8 | 2 ICLK |
| 0008 70A4h | ICU | Interrupt request register 164 | IR164 | 8 | 8 | 2 ICLK |
| 0008 70A5h | ICU | Interrupt request register 165 | IR165 | 8 | 8 | 2 ICLK |
| 0008 70A6h | ICU | Interrupt request register 166 | IR166 | 8 | 8 | 2 ICLK |
| 0008 70A7h | ICU | Interrupt request register 167 | IR167 | 8 | 8 | 2 ICLK |
| 0008 70A8h | ICU | Interrupt request register 168 | IR168 | 8 | 8 | 2 ICLK |
| 0008 70A9h | ICU | Interrupt request register 169 | IR169 | 8 | 8 | 2 ICLK |
| 0008 70AAh | ICU | Interrupt request register 170 | IR170 | 8 | 8 | 2 ICLK |
| 0008 70ABh | ICU | Interrupt request register 171 | IR171 | 8 | 8 | 2 ICLK |
| 0008 70ACh | ICU | Interrupt request register 172 | IR172 | 8 | 8 | 2 ICLK |
| 0008 70ADh | ICU | Interrupt request register 173 | IR173 | 8 | 8 | 2 ICLK |
| 0008 70AEh | ICU | Interrupt request register 174 | IR174 | 8 | 8 | 2 ICLK |
| 0008 70AFh | ICU | Interrupt request register 175 | IR175 | 8 | 8 | 2 ICLK |
| 0008 70B0h | ICU | Interrupt request register 176 | IR176 | 8 | 8 | 2 ICLK |
| 0008 70B1h | ICU | Interrupt request register 177 | IR177 | 8 | 8 | 2 ICLK |
| 0008 70B2h | ICU | Interrupt request register 178 | IR178 | 8 | 8 | 2 ICLK |
| 0008 70B3h | ICU | Interrupt request register 179 | IR179 | 8 | 8 | 2 ICLK |
| 0008 70B4h | ICU | Interrupt request register 180 | IR180 | 8 | 8 | 2 ICLK |
| 0008 70B5h | ICU | Interrupt request register 181 | IR181 | 8 | 8 | 2 ICLK |
| 0008 70B6h | ICU | Interrupt request register 182 | IR182 | 8 | 8 | 2 ICLK |
| 0008 70B7h | ICU | Interrupt request register 183 | IR183 | 8 | 8 | 2 ICLK |
| 0008 70B8h | ICU | Interrupt request register 184 | IR184 | 8 | 8 | 2 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (14 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 7505h | ICU | IRQ control register 5 | IRQCR5 | 8 | 8 | 2 ICLK |
| 0008 7506h | ICU | IRQ control register 6 | IRQCR6 | 8 | 8 | 2 ICLK |
| 0008 7507h | ICU | IRQ control register 7 | IRQCR7 | 8 | 8 | 2 ICLK |
| 0008 7508h | ICU | IRQ control register 8 | IRQCR8 | 8 | 8 | 2 ICLK |
| 0008 7509h | ICU | IRQ control register 9 | IRQCR9 | 8 | 8 | 2 ICLK |
| 0008 750Ah | ICU | IRQ control register 10 | IRQCR10 | 8 | 8 | 2 ICLK |
| 0008 750Bh | ICU | IRQ control register 11 | IRQCR11 | 8 | 8 | 2 ICLK |
| 0008 750Ch | ICU | IRQ control register 12 | IRQCR12 | 8 | 8 | 2 ICLK |
| 0008 750Dh | ICU | IRQ control register 13 | IRQCR13 | 8 | 8 | 2 ICLK |
| 0008 750Eh | ICU | IRQ control register 14 | IRQCR14 | 8 | 8 | 2 ICLK |
| 0008 750Fh | ICU | IRQ control register 15 | IRQCR15 | 8 | 8 | 2 ICLK |
| 0008 7580h | ICU | Non-maskable interrupt status register | NMISR | 8 | 8 | 2 ICLK |
| 0008 7581h | ICU | Non-maskable interrupt enable register | NMIER | 8 | 8 | 2 ICLK |
| 0008 7582h | ICU | Non-maskable interrupt clear register | NMICLR | 8 | 8 | 2 ICLK |
| 0008 7583h | ICU | NMI pin interrupt control register | NMICR | 8 | 8 | 2 ICLK |
| 0008 8000h | CMT | Compare match timer start register 0 | CMSTR0 | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8002h | CMT0 | Compare match timer control register | CMCR | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8004h | CMT0 | Compare match timer counter | CMCNT | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8006h | CMT0 | Compare match timer constant register | CMCOR | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8008h | CMT1 | Compare match timer control register | CMCR | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 800Ah | CMT1 | Compare match timer counter | CMCNT | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 800Ch | CMT1 | Compare match timer constant register | CMCOR | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8010h | CMT | Compare match timer start register 1 | CMSTR1 | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8012h | CMT2 | Compare match timer control register | CMCR | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8014h | CMT2 | Compare match timer counter | CMCNT | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8016h | CMT2 | Compare match timer constant register | CMCOR | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8018h | CMT3 | Compare match timer control register | CMCR | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 801Ah | CMT3 | Compare match timer counter | CMCNT | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 801Ch | CMT3 | Compare match timer constant register | CMCOR | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8028h | WDT | Timer control/status register | READ.TCSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8028h | WDT | Write window A register | WRITE.WINA | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8029h | WDT | Timer counter | READ.TCNT | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 802Ah | WDT | Write window B register | WRITE.WINB | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 802Bh | WDT | Reset control/status register | READ.RSTCSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8030h | IWDT | IWDT refresh register | IWDTRR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8032h | IWDT | IWDT control register | IWDTCR | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8034h | IWDT | IWDT status register | IWDTSR | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8040h | AD0 | A/D data register A | ADDRA | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8042h | AD0 | A/D data register B | ADDRB | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8044h | AD0 | A/D data register C | ADDRC | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8046h | AD0 | A/D data register D | ADDRD | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8050h | AD0 | A/D control/status register | ADCSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8051h | AD0 | A/D control register | ADCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8052h | AD0 | ADDRn format select register | ADDPR | 8 | 8 | 2 to 3 PCLK*8 |

**Table 4.1 List of I/O Registers (Address Order) (18 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 826Fh | SCI5 | Serial extended mode register | SEMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8268h | SMCI5 | Serial mode register | SMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8269h | SMCI5 | Bit rate register | BRR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 826Ah | SMCI5 | Serial control register | SCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 826Bh | SMCI5 | Transmit data register | TDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 826Ch | SMCI5 | Serial status register | SSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 826Dh | SMCI5 | Receive data register | RDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 826Eh | SMCI5 | Smart card mode register | SCMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8270h | SCI6 | Serial mode register | SMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8271h | SCI6 | Bit rate register | BRR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8272h | SCI6 | Serial control register | SCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8273h | SCI6 | Transmit data register | TDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8274h | SCI6 | Serial status register | SSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8275h | SCI6 | Receive data register | RDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8276h | SCI6 | Smart card mode register | SCMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8277h | SCI6 | Serial extended mode register | SEMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8270h | SMCI6 | Serial mode register | SMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8271h | SMCI6 | Bit rate register | BRR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8272h | SMCI6 | Serial control register | SCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8273h | SMCI6 | Transmit data register | TDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8274h | SMCI6 | Serial status register | SSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8275h | SMCI6 | Receive data register | RDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8276h | SMCI6 | Smart card mode register | SCMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8280h | CRC | CRC control register | CRCCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8281h | CRC | CRC data input register | CRCDIR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8282h | CRC | CRC data output register | CRCDOR | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8300h | RIIC0 | I2C bus control register 1 | ICCR1 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8301h | RIIC0 | I2C bus control register 2 | ICCR2 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8302h | RIIC0 | I2C bus mode register 1 | ICMR1 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8303h | RIIC0 | I2C bus mode register 2 | ICMR2 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8304h | RIIC0 | I2C bus mode register 3 | ICMR3 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8305h | RIIC0 | I2C bus function enable register | ICFER | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8306h | RIIC0 | I2C bus status enable register | ICSER | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8307h | RIIC0 | I2C bus interrupt enable register | ICIER | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8308h | RIIC0 | I2C bus status register 1 | ICSR1 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8309h | RIIC0 | I2C bus status register 2 | ICSR2 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 830Ah | RIIC0 | Slave address register L0 | SARL0 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 830Ah | RIIC0 | Timeout internal counter | TMOCNT | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 830Ah | RIIC0 | Timeout internal counter L | TMOCNTL | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 830Bh | RIIC0 | Slave address register U0 | SARU0 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 830Bh | RIIC0 | Timeout internal counter U | TMOCNTU | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 830Ch | RIIC0 | Slave address register L1 | SARL1 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 830Dh | RIIC0 | Slave address register U1 | SARU1 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 830Eh | RIIC0 | Slave address register L2 | SARL2 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 830Fh | RIIC0 | Slave address register U2 | SARU2 | 8 | 8 | 2 to 3 PCLK*8 |

**Table 4.1 List of I/O Registers (Address Order) (23 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 8A01h | MTU10 | Timer control register | TCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A02h | MTU9 | Timer mode register | TMDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A03h | MTU10 | Timer mode register | TMDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A04h | MTU9 | Timer I/O control register H | TIORH | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A05h | MTU9 | Timer I/O control register L | TIORL | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A06h | MTU10 | Timer I/O control register H | TIORH | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A07h | MTU10 | Timer I/O control register L | TIORL | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A08h | MTU9 | Timer interrupt enable register | TIER | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A09h | MTU10 | Timer interrupt enable register | TIER | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A0Ah | MTUB | Timer output master enable register | TOER | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A0Dh | MTUB | Timer gate control register | TGCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A0Eh | MTUB | Timer output control register 1 | TOCR1 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A0Fh | MTUB | Timer output control register 2 | TOCR2 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A10h | MTU9 | Timer counter | TCNT | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8A12h | MTU10 | Timer counter | TCNT | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8A14h | MTUB | Timer cycle data register | TCDR | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8A16h | MTUB | Timer dead time data register | TDDR | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8A18h | MTU9 | Timer general register A | TGRA | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8A1Ah | MTU9 | Timer general register B | TGRB | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8A1Ch | MTU10 | Timer general register A | TGRA | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8A1Eh | MTU10 | Timer general register B | TGRB | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8A20h | MTUB | Timer subcounter | TCNTS | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8A22h | MTUB | MTUB Timer cycle buffer register | TCBR | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8A24h | MTU9 | Timer general register C | TGRC | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8A26h | MTU9 | Timer general register D | TGRD | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8A28h | MTU10 | Timer general register C | TGRC | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8A2Ah | MTU10 | Timer general register D | TGRD | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8A2Ch | MTU9 | Timer status register | TSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A2Dh | MTU10 | Timer status register | TSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A30h | MTUB | Timer interrupt skipping set register | TITCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A31h | MTUB | Timer interrupt skipping counter | TITCNT | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A32h | MTUB | TUB Timer dead time enable register | TBTER | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A34h | MTUB | Timer dead time enable register | TDER | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A36h | MTUB | Timer output level buffer register | TOLBR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A38h | MTU9 | Timer buffer operation transfer mode register | TBTM | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A39h | MTU10 | Timer buffer operation transfer mode register | TBTM | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A40h | MTU10 | Timer A/D converter start request control register | TADCR | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8A44h | MTU10 | Timer A/D converter start request cycle set register A | TADCORA | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8A46h | MTU10 | Timer A/D converter start request cycle set register B | TADCORB | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8A48h | MTU10 | Timer A/D converter start request cycle set buffer register A | TADCOBRA | 16 | 16 | 2 to 3 PCLK*8 |

**Table 4.1 List of I/O Registers (Address Order) (28 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 C28Ah | SYSTEM | Sub-clock oscillator control register | SUBOSCCR | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C28Ch | SYSTEM | Key code register for voltage detection control register | LVDKEYR | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C28Dh | SYSTEM | Voltage detection control register | LVDCR | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C290h | SYSTEM | Deep standby backup register 0 | DPSBKR0 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C291h | SYSTEM | Deep standby backup register 1 | DPSBKR1 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C292h | SYSTEM | Deep standby backup register 2 | DPSBKR2 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C293h | SYSTEM | Deep standby backup register 3 | DPSBKR3 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C294h | SYSTEM | Deep standby backup register 4 | DPSBKR4 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C295h | SYSTEM | Deep standby backup register 5 | DPSBKR5 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C296h | SYSTEM | Deep standby backup register 6 | DPSBKR6 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C297h | SYSTEM | Deep standby backup register 7 | DPSBKR7 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C298h | SYSTEM | Deep standby backup register 8 | DPSBKR8 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C299h | SYSTEM | Deep standby backup register 9 | DPSBKR9 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C29Ah | SYSTEM | Deep standby backup register 10 | DPSBKR10 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C29Bh | SYSTEM | Deep standby backup register 11 | DPSBKR11 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C29Ch | SYSTEM | Deep standby backup register 12 | DPSBKR12 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C29Dh | SYSTEM | Deep standby backup register 13 | DPSBKR13 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C29Eh | SYSTEM | Deep standby backup register 14 | DPSBKR14 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C29Fh | SYSTEM | Deep standby backup register 15 | DPSBKR15 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C2A0h | SYSTEM | Deep standby backup register 16 | DPSBKR16 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C2A1h | SYSTEM | Deep standby backup register 17 | DPSBKR17 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C2A2h | SYSTEM | Deep standby backup register 18 | DPSBKR18 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C2A3h | SYSTEM | Deep standby backup register 19 | DPSBKR19 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C2A4h | SYSTEM | Deep standby backup register 20 | DPSBKR20 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C2A5h | SYSTEM | Deep standby backup register 21 | DPSBKR21 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C2A6h | SYSTEM | Deep standby backup register 22 | DPSBKR22 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C2A7h | SYSTEM | Deep standby backup register 23 | DPSBKR23 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C2A8h | SYSTEM | Deep standby backup register 24 | DPSBKR24 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C2A9h | SYSTEM | Deep standby backup register 25 | DPSBKR25 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C2AAh | SYSTEM | Deep standby backup register 26 | DPSBKR26 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C2ABh | SYSTEM | Deep standby backup register 27 | DPSBKR27 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C2ACh | SYSTEM | Deep standby backup register 28 | DPSBKR28 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C2ADh | SYSTEM | Deep standby backup register 29 | DPSBKR29 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C2AEh | SYSTEM | Deep standby backup register 30 | DPSBKR30 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C2AFh | SYSTEM | Deep standby backup register 31 | DPSBKR31 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C400h | RTC | 64-Hz counter | R64CNT | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C402h | RTC | Second counter | RSECCNT | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C404h | RTC | Minute counter | RMINCNT | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C406h | RTC | Hour counter | RHRCNT | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C408h | RTC | Day-of-week counter | RWKCNT | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C40Ah | RTC | Date counter | RDAYCNT | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C40Ch | RTC | Month counter | RMONCNT | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C40Eh | RTC | Year counter | RYRCNT | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 C410h | RTC | Second alarm register | RSECAR | 8 | 8 | 2 to 3 PCLK*8 |

**Table 4.1 List of I/O Registers (Address Order) (30 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 000A 0008h | USB0 | Device state control register 0 | DVSTCTR0 | 16 | 16 | at least 9 PCLK*9 |
| 000A 0014h | USB0 | CFIFO port register | CFIFO | 16 | 8, 16 | 3 to 4 PCLK*8 |
| 000A 0018h | USB0 | D0FIFO port register | D0FIFO | 16 | 8, 16 | 3 to 4 PCLK*8 |
| 000A 001Ch | USB0 | D1FIFO port register | D1FIFO | 16 | 8, 16 | 3 to 4 PCLK*8 |
| 000A 0020h | USB0 | CFIFO port select register | CFIFOSEL | 16 | 16 | 3 to 4 PCLK*8 |
| 000A 0022h | USB0 | CFIFO port control register | CFIFOCTR | 16 | 16 | 3 to 4 PCLK*8 |
| 000A 0028h | USB0 | D0FIFO port select register | D0FIFOSEL | 16 | 16 | 3 to 4 PCLK*8 |
| 000A 002Ah | USB0 | D0FIFO port control register | D0FIFOCTR | 16 | 16 | 3 to 4 PCLK*8 |
| 000A 002Ch | USB0 | D1FIFO port select register | D1FIFOSEL | 16 | 16 | 3 to 4 PCLK*8 |
| 000A 002Eh | USB0 | D1FIFO port control register | D1FIFOCTR | 16 | 16 | 3 to 4 PCLK*8 |
| 000A 0030h | USB0 | Interrupt enable register 0 | INTENB0 | 16 | 16 | at least 9 PCLK*9 |
| 000A 0032h | USB0 | Interrupt enable register 1 | INTENB1 | 16 | 16 | at least 9 PCLK*9 |
| 000A 0036h | USB0 | BRDY interrupt enable register | BRDYENB | 16 | 16 | at least 9 PCLK*9 |
| 000A 0038h | USB0 | NRDY interrupt enable register | NRDYENB | 16 | 16 | at least 9 PCLK*9 |
| 000A 003Ah | USB0 | BEMP interrupt enable register | BEMPENB | 16 | 16 | at least 9 PCLK*9 |
| 000A 003Ch | USB0 | SOF output configuration register | SOFCFG | 16 | 16 | at least 9 PCLK*9 |
| 000A 0040h | USB0 | Interrupt status register 0 | INTSTS0 | 16 | 16 | at least 9 PCLK*9 |
| 000A 0042h | USB0 | Interrupt status register 1 | INTSTS1 | 16 | 16 | at least 9 PCLK*9 |
| 000A 0046h | USB0 | BRDY interrupt enable register | BRDYSTS | 16 | 16 | at least 9 PCLK*9 |
| 000A 0048h | USB0 | NRDY interrupt status register | NRDYSTS | 16 | 16 | at least 9 PCLK*9 |
| 000A 004Ah | USB0 | BEMP interrupt status register | BEMPSTS | 16 | 16 | at least 9 PCLK*9 |
| 000A 004Ch | USB0 | Frame number register | FRMNUM | 16 | 16 | at least 9 PCLK*9 |
| 000A 004Eh | USB0 | Device state change register | DVCHGR | 16 | 16 | at least 9 PCLK*9 |
| 000A 0050h | USB0 | USB address register | USBADDR | 16 | 16 | at least 9 PCLK*9 |
| 000A 0054h | USB0 | USB request type register | USBREQ | 16 | 16 | at least 9 PCLK*9 |
| 000A 0056h | USB0 | USB request value register | USBVAL | 16 | 16 | at least 9 PCLK*9 |
| 000A 0058h | USB0 | USB request index register | USBINDX | 16 | 16 | at least 9 PCLK*9 |
| 000A 005Ah | USB0 | USB request length register | USBLENG | 16 | 16 | at least 9 PCLK*9 |
| 000A 005Ch | USB0 | DCP configuration register | DCPCFG | 16 | 16 | at least 9 PCLK*9 |
| 000A 005Eh | USB0 | DCP maximum packet size register | DCPMAXP | 16 | 16 | at least 9 PCLK*9 |

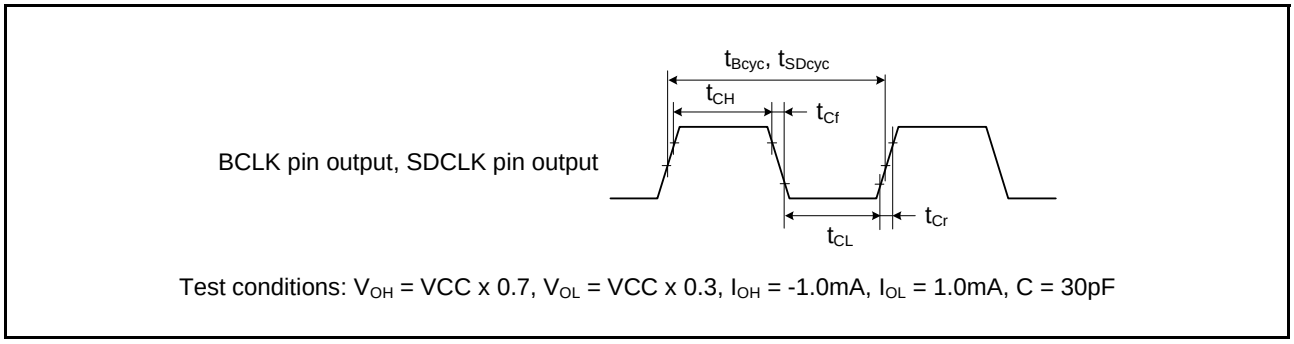



**Figure 5.1 BCLK Pin Output, SDCLK Pin Output Timing**

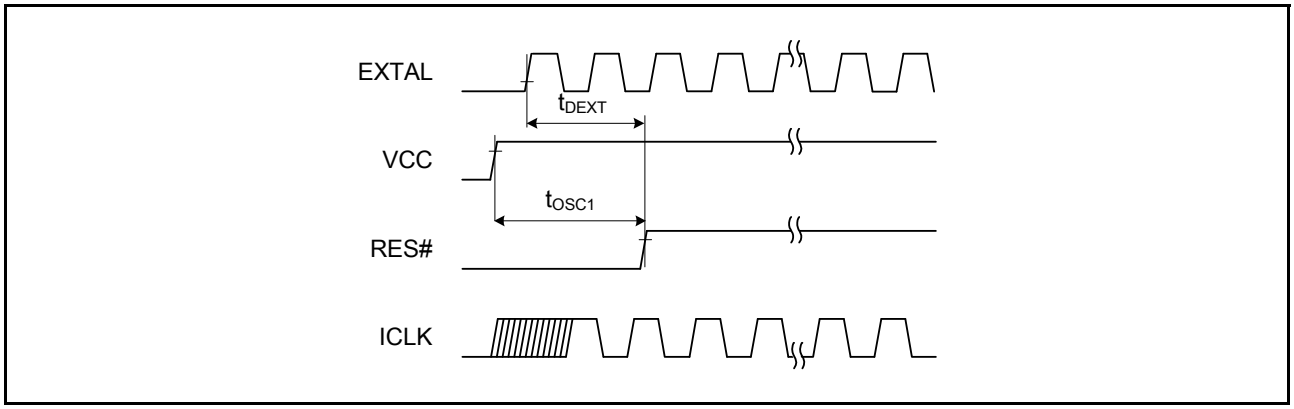



**Figure 5.2 Oscillation Settling Timing**

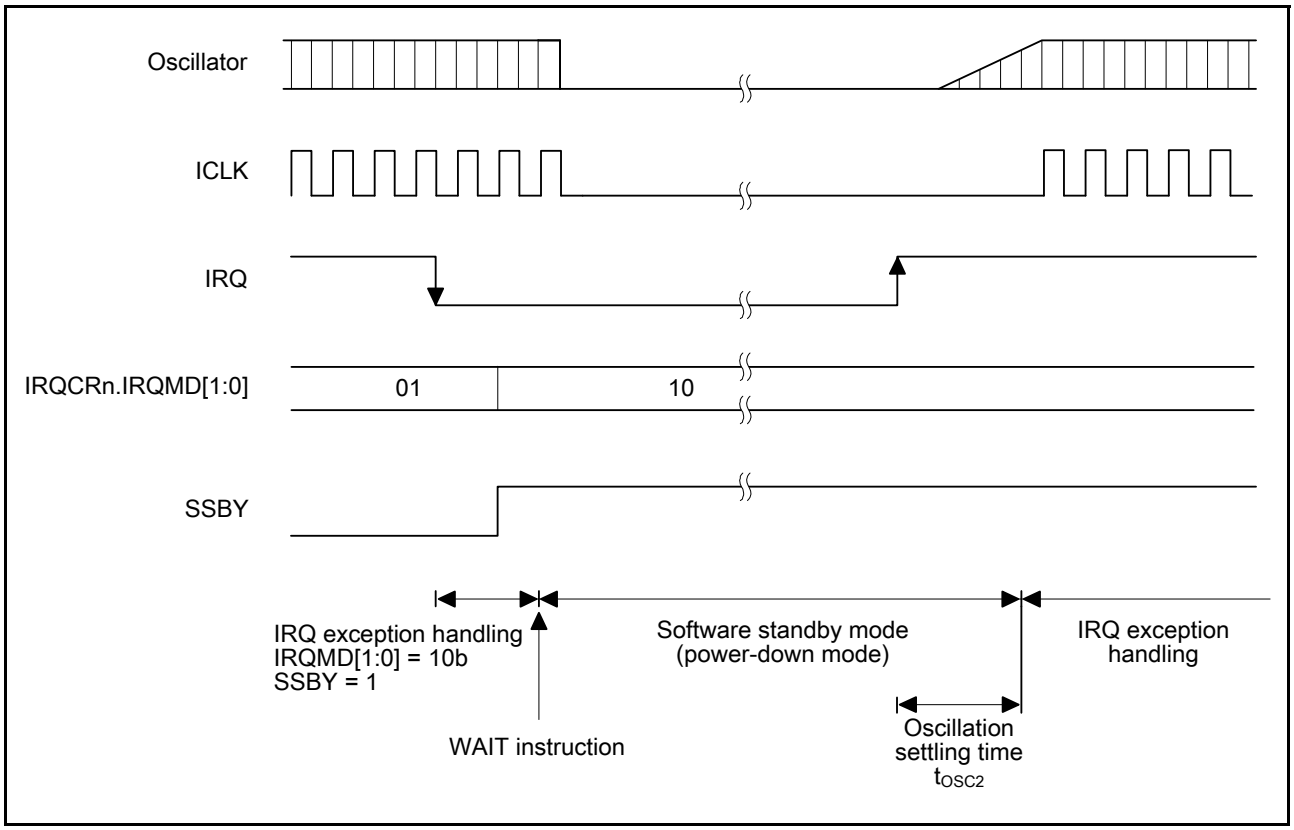



**Figure 5.3 Oscillation Settling Timing after Software Standby Mode**

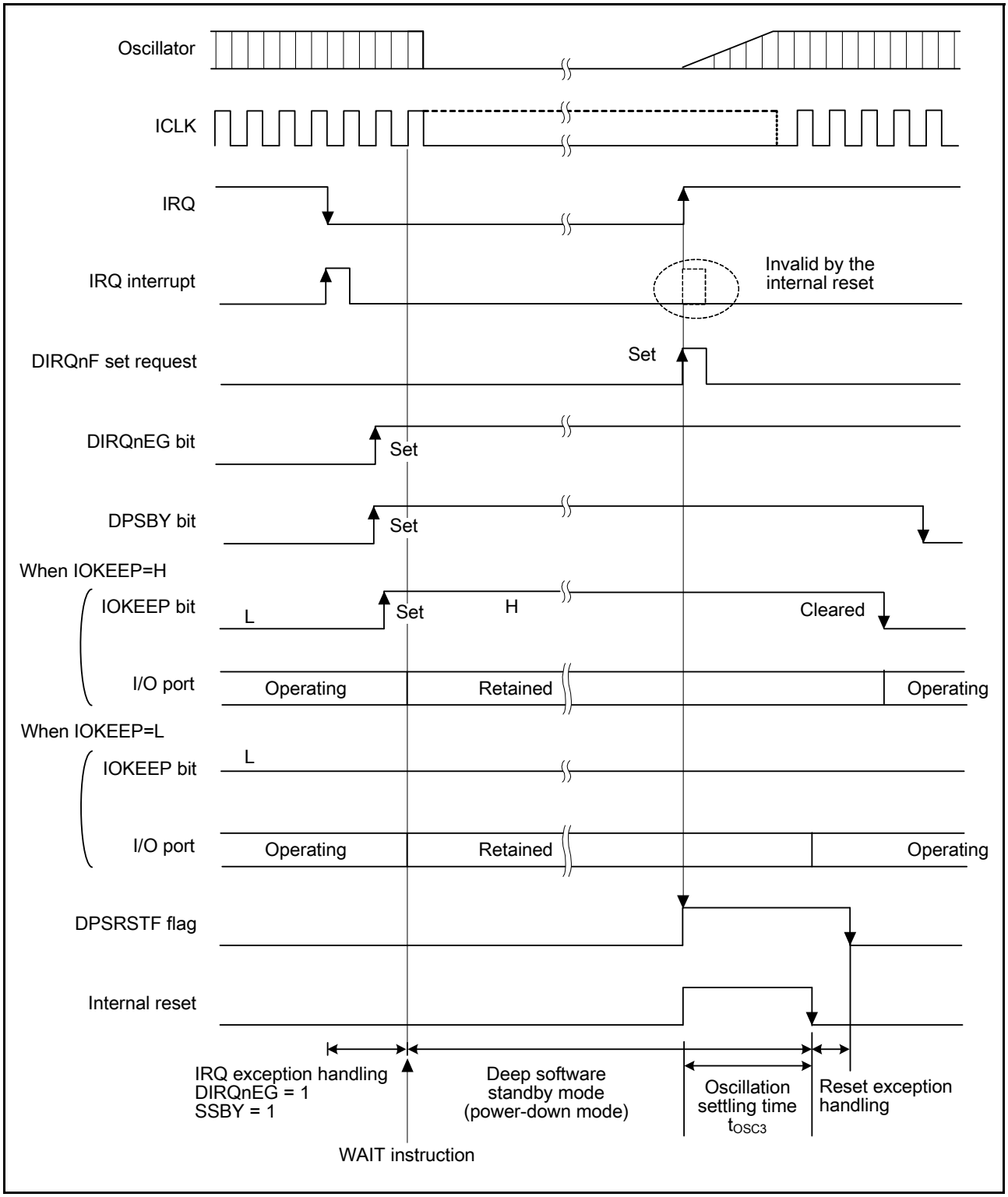



**Figure 5.4 Oscillation Settling Timing after Deep Software Standby Mode**

**Table 5.18 Timing of On-Chip Peripheral Modules (10)**

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
PCLK = 8 to 50 MHz
$T_a$ = -40 to +85°C

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| TCK clock cycle time | $t_{TCKcyc}$ | 100 | — | — | ns | Figure 5.58 |
| TCK clock high pulse width | $t_{TCKH}$ | 45 | — | — | ns | |
| TCK clock low pulse width | $t_{TCKL}$ | 45 | — | — | ns | |
| TCK clock rising time | $t_{TCKr}$ | — | — | 5 | ns | |
| TCK clock falling time | $t_{TCKf}$ | — | — | 5 | ns | |
| TRST# pulse width | $t_{TRSTW}$ | 20 | — | — | $t_{TCKcyc}$ | Figure 5.59 |
| TMS setup time | $t_{TMSS}$ | 20 | — | — | ns | Figure 5.60 |
| TMS hold time | $t_{TMSH}$ | 20 | — | — | ns | |
| TDI setup time | $t_{TDIS}$ | 20 | — | — | ns | |
| TDI hold time | $t_{TDIH}$ | 20 | — | — | ns | |
| TDO data delay time | $t_{TDOD}$ | — | — | 40 | ns | |

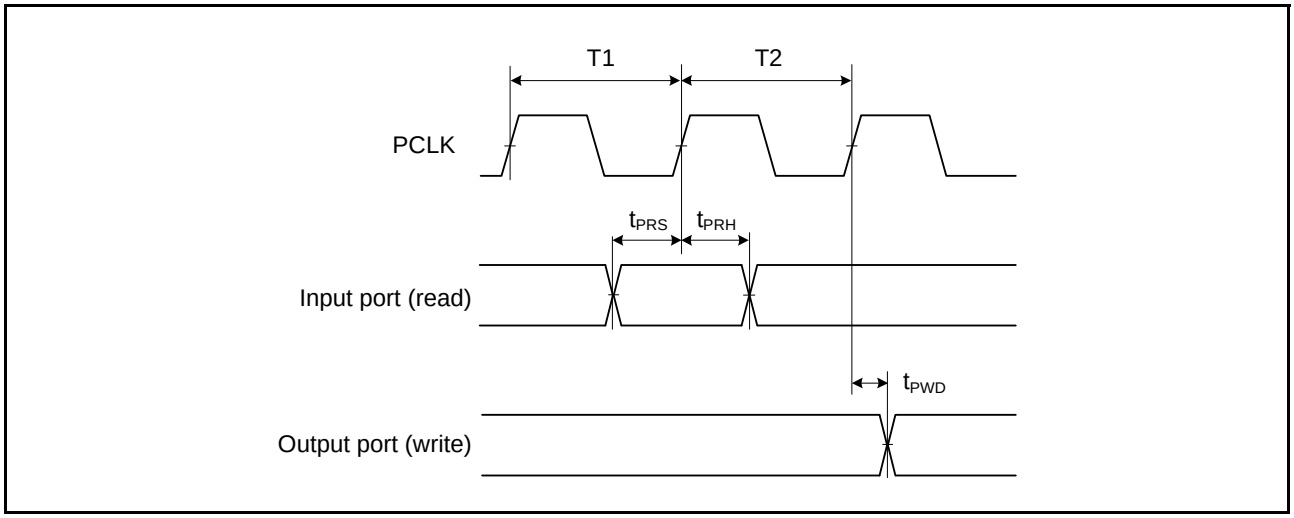



**Figure 5.25 I/O Port Input/Output Timing**

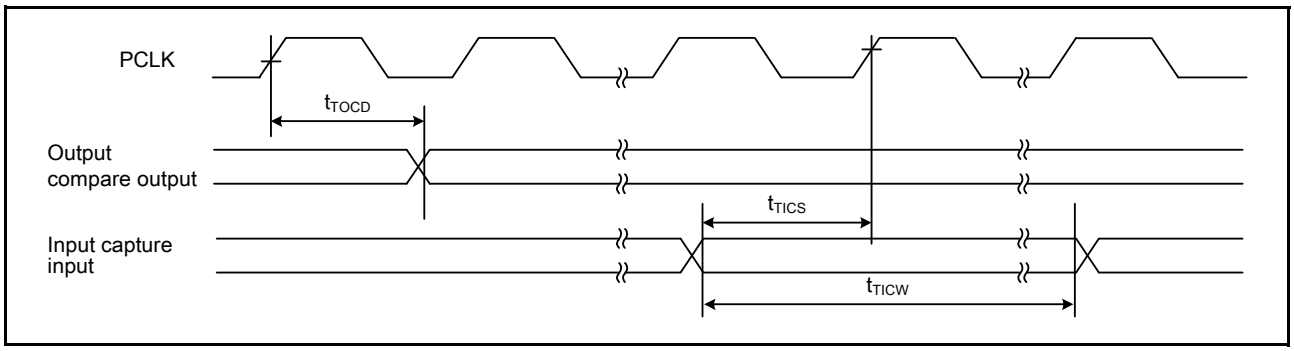



**Figure 5.26 MTU2 Input/Output Timing**

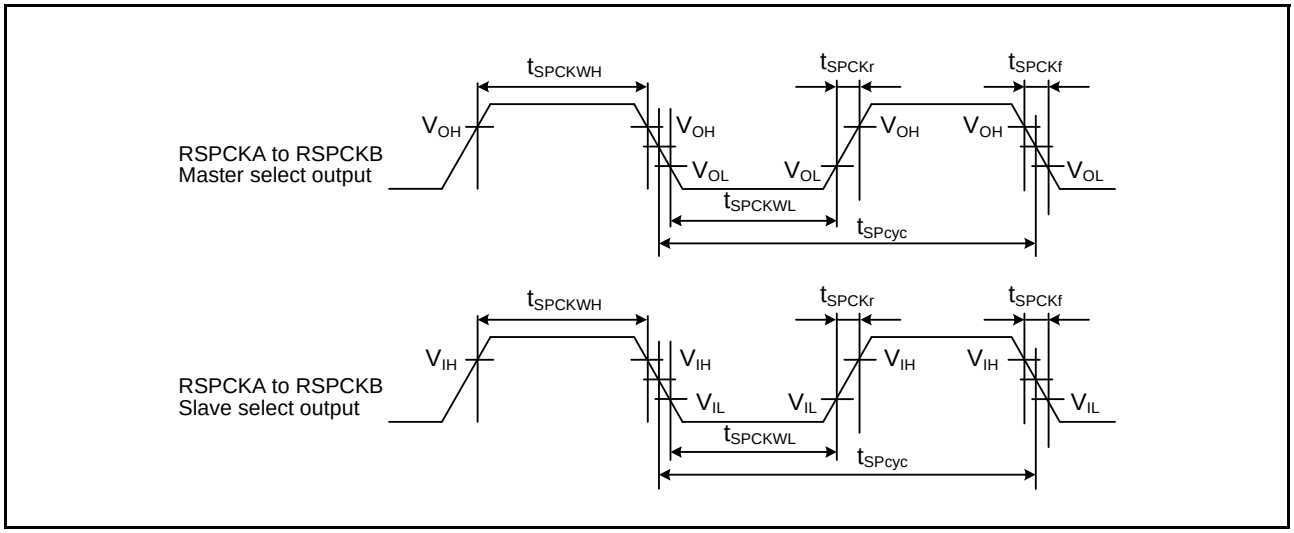



**Figure 5.38 RSPI Clock Timing**

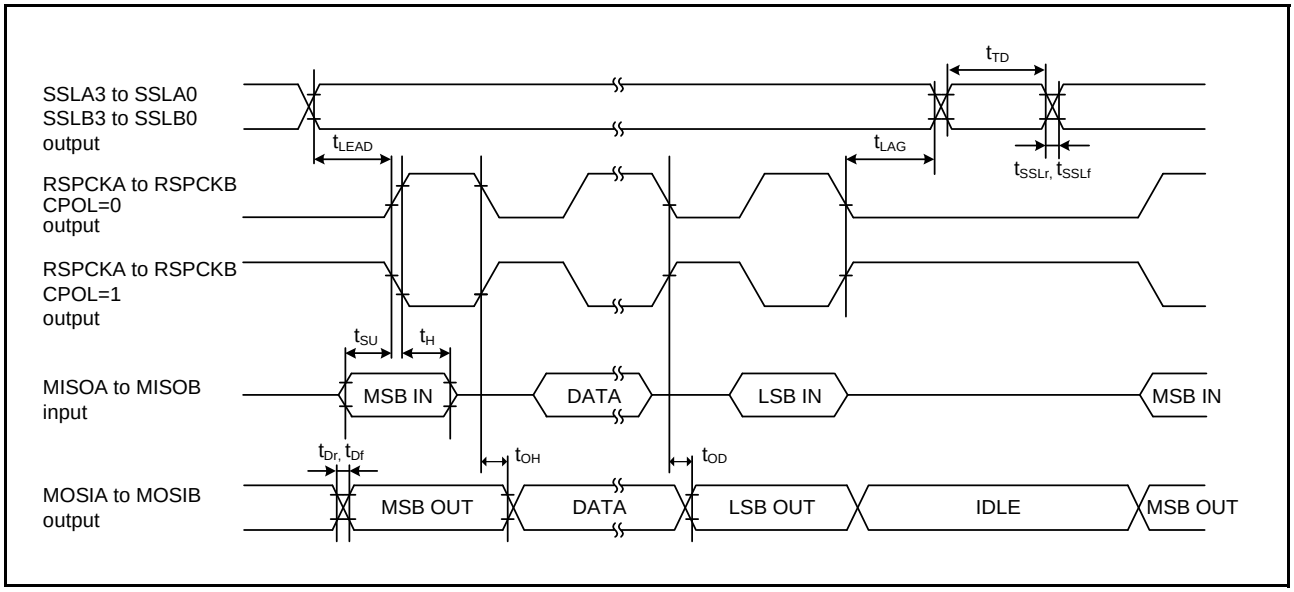



**Figure 5.39 RSPI Timing (Master, CPHA = 0)**

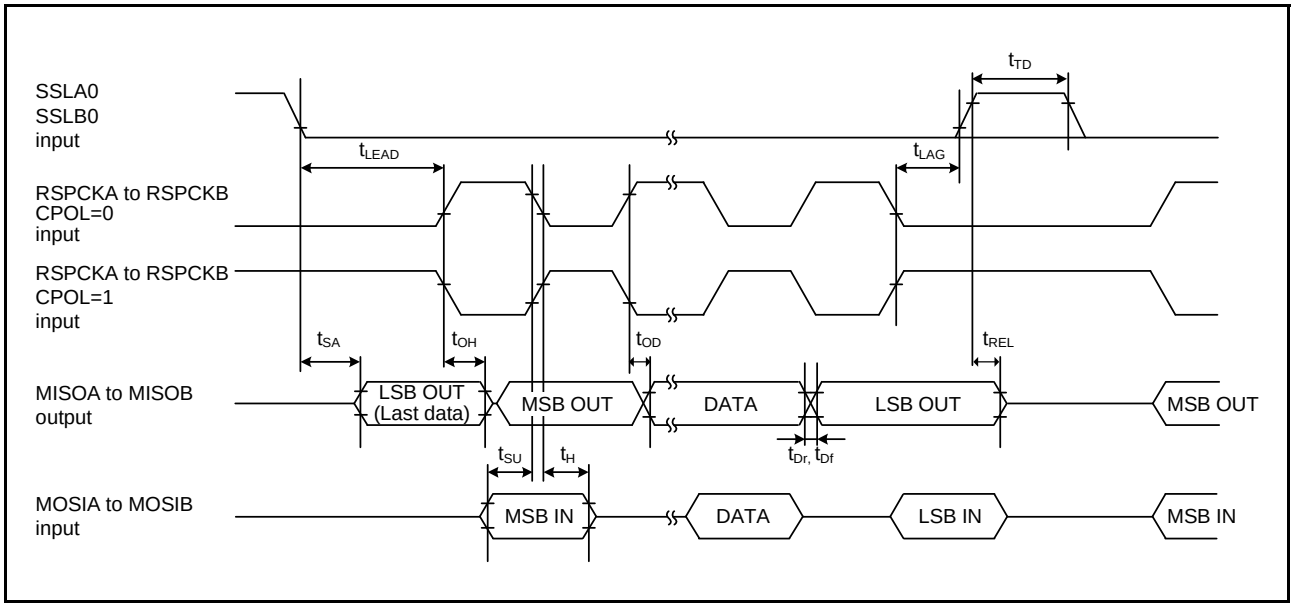



**Figure 5.42 RSPI Timing (Slave, CPHA = 1)**

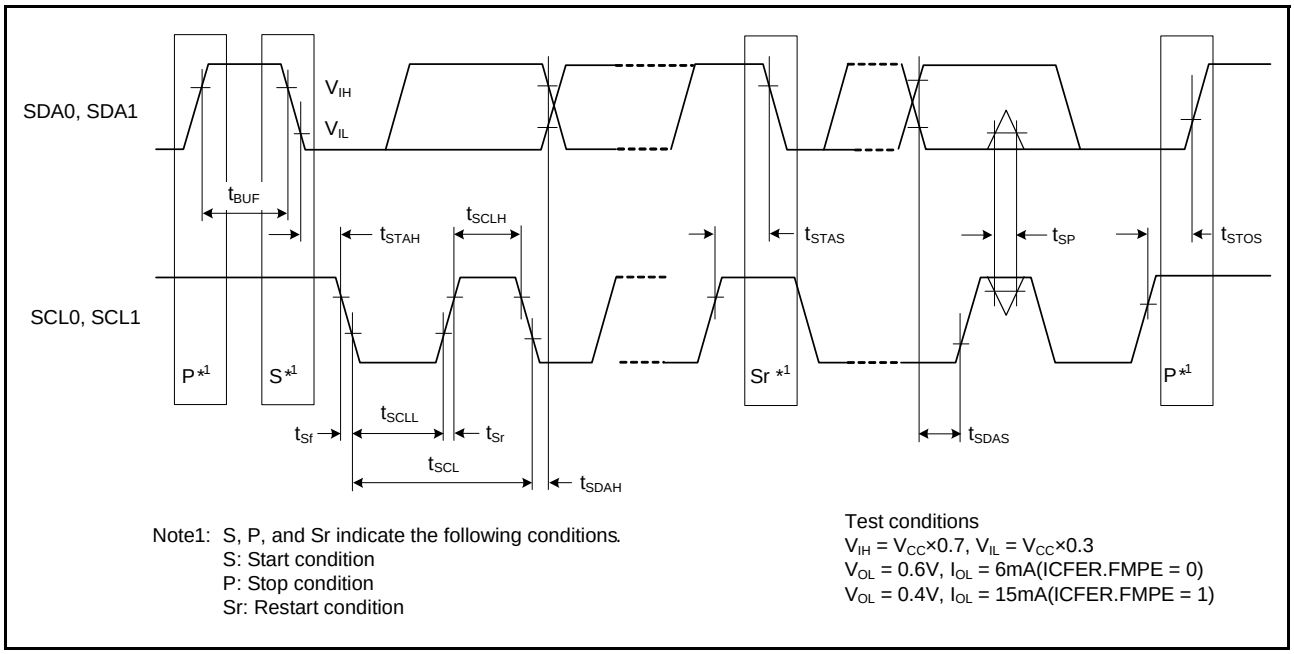



**Figure 5.43 I2C Bus Interface Input/Output Timing**

## 5.4 USB Characteristics

**Table 5.19 Internal USB Full-Speed Characteristics (DP, DM Pin Characteristics)**

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 3.0 to 3.6 V, VREFH = 3.0 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
PCLK = 24 to 50 MHz
$T_a$ = -40 to +85°C

| Item | | Symbol | Min. | Max. | Unit | Test Conditions | |
|---|---|---|---|---|---|---|---|
| Input characteristics | Input high level voltage | $V_{IH}$ | 2.0 | — | V | | Figure 5.61 and Figure 5.62 |
| | Input low level voltage | $V_{IL}$ | — | 0.8 | V | | |
| | Differential input Sensitivity | $V_{DI}$ | 0.2 | — | V | \| DP — DM \| | |
| | Differential commom mode range | $V_{CM}$ | 0.8 | 2.5 | V | | |
| Output characteristics | Output high level voltage | $V_{OH}$ | 2.8 | 3.6 | V | $I_{OH}$ = -200µA | |
| | Output low level voltage | $V_{OL}$ | 0.0 | 0.3 | V | $I_{OL}$ = 2 mA | |
| | Cross over voltage | $V_{CRS}$ | 1.3 | 2.0 | V | | |
| | Rising time | $t_{Lr}$ | 4 | 20 | ns | | |
| | Falling time | $t_{Lf}$ | 4 | 20 | ns | | |
| | Rising/falling time ratio | $t_{Lr}$ / $t_{Lf}$ | 90 | 111.11 | % | $t_{Lr}$ / $t_{Lf}$ | |
| | Output resistance | $Z_{DRV}$ | 28 | 44 | Ω | Rs = 22Ω included | |

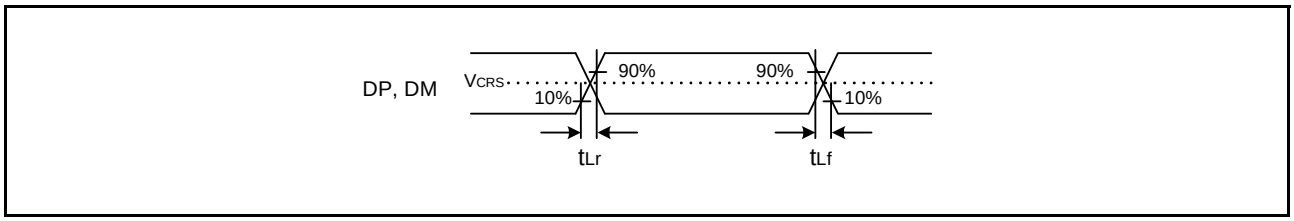



**Figure 5.61 DP, DM Output Timing (Full-Speed)**

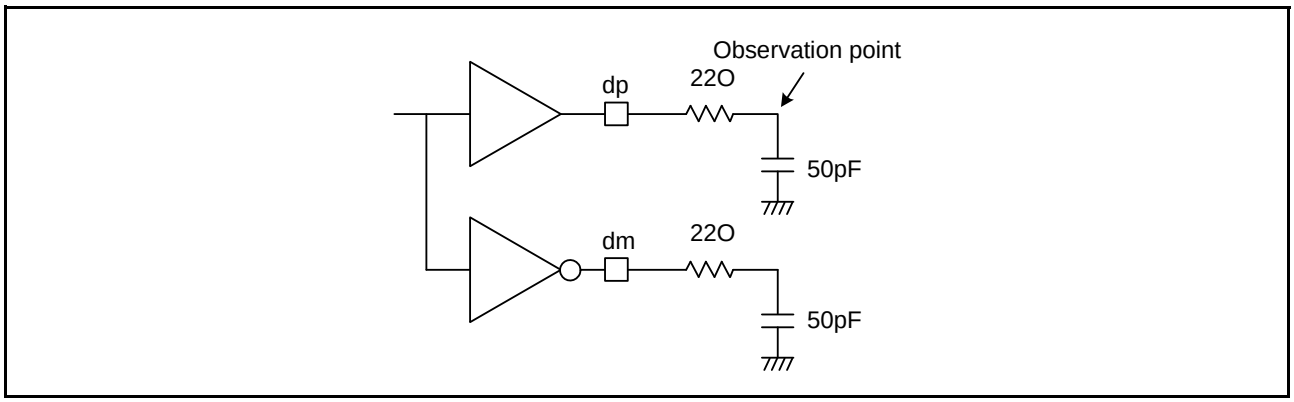



**Figure 5.62 Test Circuit (Full-Speed)**

## 5.5 A/D Conversion Characteristics

**Table 5.20 10-Bit A/D Conversion Characteristics**

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
PCLK = 8 to 50 MHz
$T_a$ = -40 to +85°C

| Item | | | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Resolution | | | 10 | 10 | 10 | bits | |
| Conversion time*1 (PCLK = 50-MHz operation) | With 0.1-µF external capacitor | When the capacitor is charged enough*2 | 0.8 (0.3)*3 | — | — | µs | Sampling 15 states |
| | Without external capacitor | Permissible signal source impedance (max.) = 1.0 kΩ | 1.0 (0.5)*3 | — | — | | Sampling 25 states |
| | | Permissible signal source impedance (max.) = 5.0 kΩ | 2.6 (2.1)*3 | — | — | | Sampling 105 states |
| Analog input capacitance | | | — | — | 6.0 | pF | |
| INL integral nonlinearity error | | | — | ±1.5 | ±3.0 | LSB | |
| Offset error | | | — | ±1.5 | ±3.0 | LSB | |
| Full-scale error | | | — | ±1.5 | ±3.0 | LSB | |
| Quantization error | | | — | ±0.5 | — | LSB | |
| Absolute accuracy | | | — | ±1.5 | ±3.0 | LSB | |
| DNL differential nonlinearity error | | | — | ±0.5 | ±1.0 | LSB | |

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.
Note 2. The scanning is not supported.
Note 3. The value in parentheses indicates the sampling time.

**Table 5.21 12-Bit A/D Conversion Characteristics**

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
PCLK = 8 to 50 MHz
$T_a$ = -40 to +85°C

| Item | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| Resolution | 12 | 12 | 12 | bits | |
| Conversion time*1 | 1.0 | — | — | µs | AVCC ≥ 3.0 |
| | 2.0 | — | — | µs | AVCC ≥ 2.7 |
| Analog input capacitance | — | — | 30 | pF | |
| Offset error | — | ±2.0 | ±7.5 | LSB | |
| Full-scale error | — | ±2.0 | ±7.5 | LSB | |
| Quantization error | — | ±0.5 | — | LSB | |
| Absolute accuracy | — | ±2.5 | ±8.0 | LSB | |
| Nonlinearity error | — | ±2.0 | ±4.0 | LSB | |

Note 1. The time conversion takes is the sum of the sampling interval and the time comparison takes (permissible signal-source impedance is up to 1.0 kΩ)