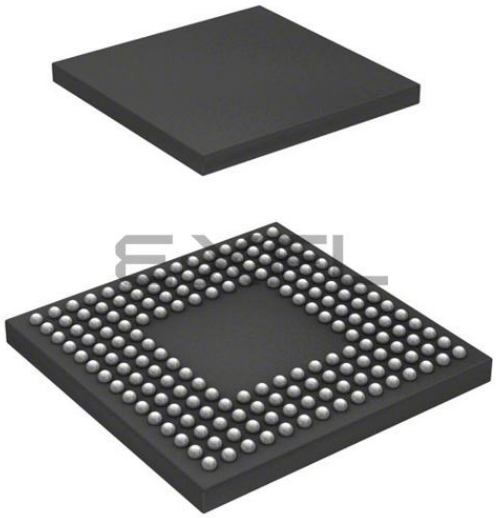
Renesas Electronics America Inc - R5F56218BDBG#U0 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	126
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10/12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LFBGA
Supplier Device Package	176-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f56218bdbg-u0

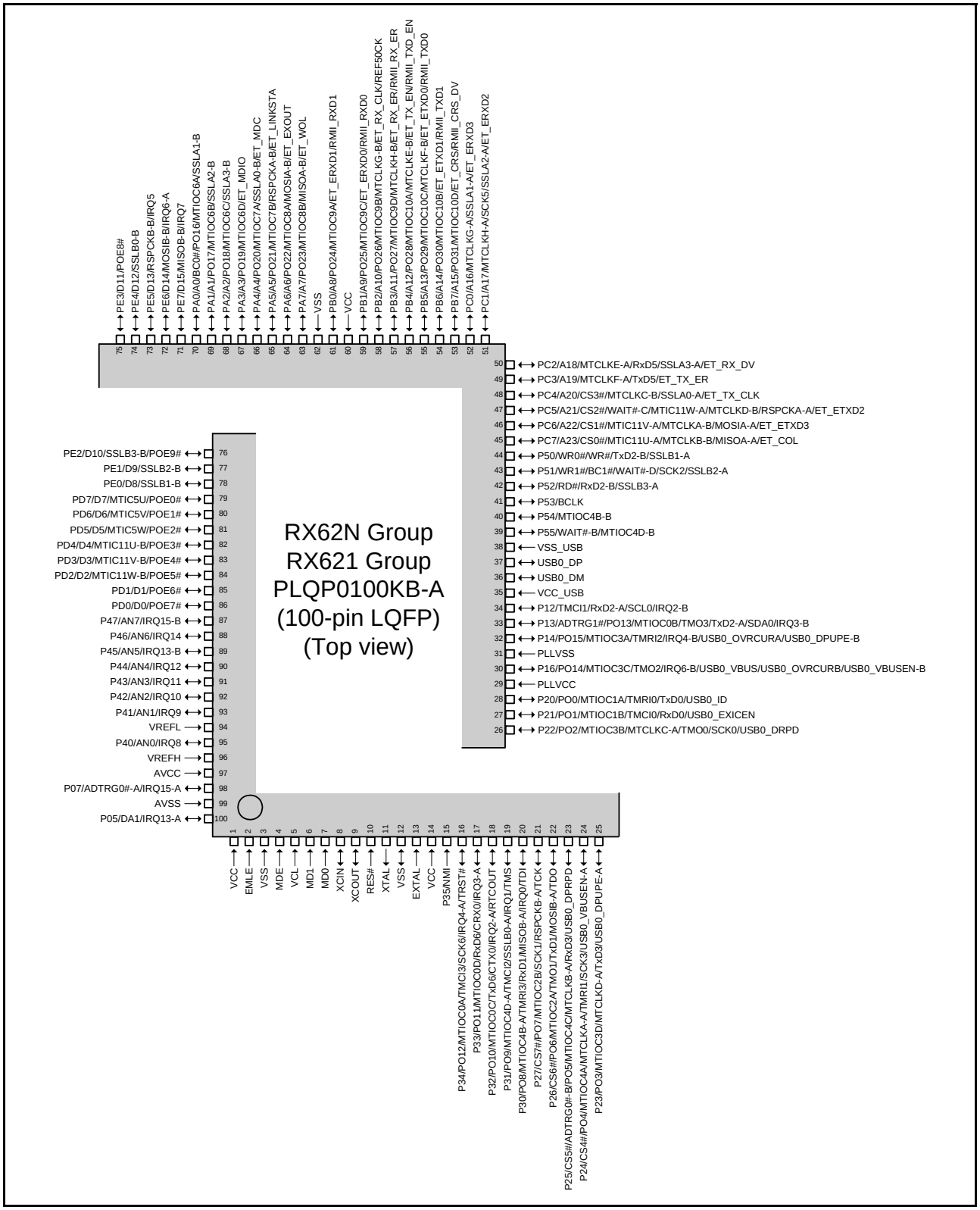

Figure 1.8 Pin Assignment of the 100-Pin LQFP (Assistance Diagram)

Table 1.4 List of Pins and Pin Functions (176-Pin LFBGA) (1 / 6)

Pin No. 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	External Bus EXDMAC	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE, WDT)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
A1	AVSS							
A2	AVCC							
A3		P42						IRQ10-B/AN2
A4		P45						IRQ13-B/AN5
A5		P46						IRQ14/AN6
A6		P90	D16/A16-B					
A7		PD0	D0			POE7#		
A8		PD2	D2			MTIC11W-B/ POE5#		
A9		PD3	D3			MTIC11V-B/ POE4#		
A10		PD4	D4			MTIC11U-B/ POE3#		
A11		PG0	D24					
A12		PD7	D7			MTIC5U-B/ POE0#		
A13		P61	CS1#-A/ SDCS#					
A14		P63	CS3#-A/ CAS#					
A15		PE1	D9				SSLB2-B	
B1		P02				TMCI1-A	SCK6-A	IRQ10-A
B2	VREFH							
B3	VREFL							
B4		P44						IRQ12/AN4
B5		P47						IRQ15-B/AN7
B6		P91	D17/A17-B					
B7		PD1	D1			POE6#		
B8		P96	D22/A22-B					
B9		P97	D23/A23-B					
B10		PD6	D6			MTIC5V-B/ POE1#		
B11		P60	CS0#-A					
B12		P62	CS2#-A/ RAS#					
B13		P64	CS4#-A/ WE#					
B14		PE2	D10			POE9#	SSLB3-B	
B15	SDCLK	P70						
C1		P00				TMRI0-A	TxD6-A	IRQ8-A
C2		P03						IRQ11-A/DA0
C3		P05						IRQ13-A/DA1
C4		P07						IRQ15-A/ ADTRG0#-A
C5		P40						IRQ8-B/AN0

Table 1.5 List of Pins and Pin Functions (145-Pin TFLGA) (4 / 5)

Pin No. 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	External Bus EXDMAC	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE, WDT)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
K4		P26	CS6#-C			MTIOC2A/ TMO1/ PO6	MOSIB-A/ TxD1	TDO
K5	BCLK	P53						
K6	VSS							
K7		PC7	A23/ CS0#-B	ET_COL		MTIC11U-A/ MTCLKB-B	MISOA-A	
K8		P82	EDREQ1-A	ET_ETXD1/ RMII_TXD1		MTIOC4A-B		TRSYNC
K9		PC3	A19-A	ET_TX_ER		MTCLKF-A	TxD5	
K10		PB7	A15			MTIOC10D/ PO31		
K11		P73	CS3#-B	ET_WOL				
K12		PC0	A16-A	ET_ERXD3		MTCLKG-A	SSLA1-A	
K13		PB3	A11			MTIOC9D/ MTCLKH-B/ PO27		
L1		P25	CS5#-C/ EDACK1-B		USB0_DPRPD	MTIOC4C-A/ MTCLKB-A/ PO5	RxD3-B	ADTRG0#-B
L2		P22	EDREQ0-B		USB0_DRPD	MTIOC3B-A/ MTCLKC-A/ TMO0/PO2	SCK0	
L3		P17				MTIOC3A/ PO15	TxD3-A	IRQ7-B
L4		P12				TMCI1-B	SCL0/ RxD2-A	IRQ2-B
L5	VCC_USB							
L6		P56	EDACK1-C			MTIOC3C-B		
L7		P52	RD#				SSLB3-A/ RxD2-B	
L8		P83	EDACK1-A	ET_CRS/ RMII_CRS_DV		MTIOC4C-B		TRCLK
L9		P81	EDACK0-A	ET_ETXD0/ RMII_TXD0		MTIOC3D-B		TRDATA1
L10		P77	CS7#-B	ET_RX_ER/ RMII_RX_ER				
L11		P75	CS5#-B	ET_ERXD0/ RMII_RXD0				
L12	VCC							
L13		PB6	A14			MTIOC10B/ PO30		
M1		P23	EDACK0-B		USB0_DPUPE-A	MTIOC3D-A/ MTCLKD-A/ PO3	TxD3-B	
M2		P20			USB0_ID	MTIOC1A/ TMRI0-B/ PO0	SDA1/ TxD0	
M3	PLLVCC							

Table 1.6 List of Pins and Pin Functions (144-Pin LQFP) (4 / 5)

Pin No. 144-Pin LQFP	Power Supply Clock System Control	I/O Port	External Bus EXDMAC	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE, WDT)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
82		PB3	A11			MTIOC9D/ MTCLKH-B/ PO27		
83		PB2	A10			MTIOC9B/ MTCLKG-B/ PO26		
84		PB1	A9			MTIOC9C/ PO25		
85		P72	CS2#-B	ET_MDC				
86		P71	CS1#-B	ET_MDIO				
87		PB0	A8			MTIOC9A/ PO24		
88		PA7	A7			MTIOC8B/ PO23	MISOA-B	
89		PA6	A6			MTIOC8A/ PO22	MOSIA-B	
90		PA5	A5			MTIOC7B/ PO21	RSPCKA-B	
91	VCC							
92		PA4	A4			MTIOC7A/ PO20	SSLA0-B	
93	VSS							
94		PA3	A3			MTIOC6D/ PO19		
95		PA2	A2			MTIOC6C/ PO18	SSLA3-B	
96		PA1	A1			MTIOC6B/ PO17	SSLA2-B	
97		PA0	A0/BC0#/			MTIOC6A/ PO16	SSLA1-B	
98		P67	CS7#-A/ DQM1					
99		P66	CS6#-A/ DQM0					
100		P65	CS5#-A/ CKE					
101		PE7	D15				MISOB-B	IRQ7-A
102		PE6	D14				MOSIB-B	IRQ6-A
103	VCC							
104	SDCLK	P70						
105	VSS							
106		PE5	D13				RSPCKB-B	IRQ5-A
107		PE4	D12				SSLB0-B	
108		PE3	D11			POE8#		
109		PE2	D10			POE9#	SSLB3-B	
110		PE1	D9				SSLB2-B	
111		PE0	D8				SSLB1-B	

Table 1.7 List of Pins and Pin Functions (100-Pin LQFP) (3 / 4)

Pin No. 100-Pin LQFP	Power Supply Clock System Control	I/O Port	External Bus	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
53		PB7	A15	ET_CRS/ RMII_CRS_DV		MTIOC10D/ PO31		
54		PB6	A14	ET_ETXD1/ RMII_TXD1		MTIOC10B/ PO30		
55		PB5	A13	ET_ETXD0/ RMII_TXD0		MTIOC10C/ MTCLKF-B/ PO29		
56		PB4	A12	ET_TX_EN/ RMII_TXD_EN		MTIOC10A/ MTCLKE-B/ PO28		
57		PB3	A11	ET_RX_ER/ RMII_RX_ER		MTIOC9D/ MTCLKH-B/ PO27		
58		PB2	A10	ET_RX_CLK/ REF50CK		MTIOC9B/ MTCLKG-B/ PO26		
59		PB1	A9	ET_ERXD0/ RMII_RXD0		MTIOC9C/ PO25		
60	VCC							
61		PB0	A8	ET_ERXD1/ RMII_RXD1		MTIOC9A/ PO24		
62	VSS							
63		PA7	A7	ET_WOL		MTIOC8B/ PO23	MISOA-B	
64		PA6	A6	ET_EXOUT		MTIOC8A/ PO22	MOSIA-B	
65		PA5	A5	ET_LINKSTA		MTIOC7B/ PO21	RSPCKA-B	
66		PA4	A4	ET_MDC		MTIOC7A/ PO20	SSLA0-B	
67		PA3	A3	ET_MDIO		MTIOC6D/ PO19		
68		PA2	A2			MTIOC6C/ PO18	SSLA3-B	
69		PA1	A1			MTIOC6B/ PO17	SSLA2-B	
70		PA0	A0/BC0#			MTIOC6A/ PO16	SSLA1-B	
71		PE7	D15				MISOB-B	IRQ7
72		PE6	D14				MOSIB-B	IRQ6-A
73		PE5	D13				RSPCKB-B	IRQ5
74		PE4	D12				SSLB0-B	
75		PE3	D11			POE8#		
76		PE2	D10			POE9#	SSLB3-B	
77		PE1	D9				SSLB2-B	
78		PE0	D8				SSLB1-B	
79		PD7	D7			MTIC5U/ POE0#		

2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen general-purpose registers (R0 to R15). R1 to R15 can be used as data registers or address registers.

R0, a general-purpose register, also functions as the stack pointer (SP). The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

(1) Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).

Set the ISP or USP to a multiple of four, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts.

Set INTB to a multiple of four.

(3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(4) Processor Status Word (PSW)

The processor status word (PSW) indicates results of instruction execution or the state of the CPU.

(5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC.

(6) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.

The FINTV register specifies a branch destination address when a fast interrupt has been generated.

(8) Floating-Point Status Word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.

When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the exception cause can be identified by checking the corresponding Cj flag in the exception handling routine. If the exception handling is masked (Ej = 0), the occurrence of exception can be checked by reading the Fj flag at the end of a series of processing. Once the Fj flag has been set to 1, this value is retained until it is cleared to 0 by software (j = X, U, Z, O, or V).

Table 4.1 List of I/O Registers (Address Order) (2 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 208Ch	DMAC2	DMA block transfer count register	DMCRB	16	16	2 ICLK
0008 2090h	DMAC2	DMA transfer mode register	DMTMD	16	16	2 ICLK
0008 2093h	DMAC2	DMA interrupt setting register	DMINT	8	8	2 ICLK
0008 2094h	DMAC2	DMA address mode register	DMAMD	16	16	2 ICLK
0008 209Ch	DMAC2	DMA transfer enable register	DMCNT	8	8	2 ICLK
0008 209Dh	DMAC2	DMA software start register	DMREQ	8	8	2 ICLK
0008 209Eh	DMAC2	DMA status register	DMSTS	8	8	2 ICLK
0008 209Fh	DMAC2	DMA activation source flag control register	DMCSL	8	8	2 ICLK
0008 20C0h	DMAC3	DMA source address register	DMSAR	32	32	2 ICLK
0008 20C4h	DMAC3	DMA destination address register	DMDAR	32	32	2 ICLK
0008 20C8h	DMAC3	DMA transfer count register	DMCRA	32	32	2 ICLK
0008 20CCh	DMAC3	DMA block transfer count register	DMCRB	16	16	2 ICLK
0008 20D0h	DMAC3	DMA transfer mode register	DMTMD	16	16	2 ICLK
0008 20D3h	DMAC3	DMA interrupt setting register	DMINT	8	8	2 ICLK
0008 20D4h	DMAC3	DMA address mode register	DMAMD	16	16	2 ICLK
0008 20DCh	DMAC3	DMA transfer enable register	DMCNT	8	8	2 ICLK
0008 20DDh	DMAC3	DMA software start register	DMREQ	8	8	2 ICLK
0008 20DEh	DMAC3	DMA status register	DMSTS	8	8	2 ICLK
0008 20DFh	DMAC3	DMA activation source flag control register	DMCSL	8	8	2 ICLK
0008 2200h	DMAC	DMACA start register	DMAST	8	8	2 ICLK
0008 2400h	DTC	DTC control register	DTCCR	8	8	2 ICLK
0008 2404h	DTC	DTC vector base register	DTCVBR	32	32	2 ICLK
0008 2408h	DTC	DTC address mode register	DTCADMOD	8	8	2 ICLK
0008 240Ch	DTC	DTC module start register	DTCST	8	8	2 ICLK
0008 240Eh	DTC	DTC status register	DTCSTS	16	16	2 ICLK
0008 2800h	EXDMAC0	EXDMA source address register	EDMSAR	32	32	1 to 2 BCLK*8
0008 2804h	EXDMAC0	EXDMA destination address register	EDMDAR	32	32	1 to 2 BCLK*8
0008 2808h	EXDMAC0	EXDMA transfer count register	EDMCRA	32	32	1 to 2 BCLK*8
0008 280Ch	EXDMAC0	EXDMA block transfer count register	EDMCRB	16	16	1 to 2 BCLK*8
0008 2810h	EXDMAC0	EXDMA transfer mode register	EDMTMD	16	16	1 to 2 BCLK*8
0008 2812h	EXDMAC0	EXDMA output setting register	EDMOMD	8	8	1 to 2 BCLK*8
0008 2813h	EXDMAC0	EXDMA interrupt setting register	EDMINT	8	8	1 to 2 BCLK*8
0008 2814h	EXDMAC0	EXDMA address mode register	EDMAMD	32	32	1 to 2 BCLK*8
0008 2818h	EXDMAC0	EXDMA output setting register	EDMOFR	32	32	1 to 2 BCLK*8
0008 281Ch	EXDMAC0	EXDMA transfer enable register	EDMCNT	8	8	1 to 2 BCLK*8
0008 281Dh	EXDMAC0	EXDMA software start register	EDMREQ	8	8	1 to 2 BCLK*8
0008 281Eh	EXDMAC0	EXDMA status register	EDMSTS	8	8	1 to 2 BCLK*8
0008 2820h	EXDMAC0	EXDMA external request sense mode register	EDMRMD	8	8	1 to 2 BCLK*8
0008 2821h	EXDMAC0	EXDMA external request flag register	EDMERF	8	8	1 to 2 BCLK*8
0008 2822h	EXDMAC0	EXDMA peripheral request flag register	EDMPRF	8	8	1 to 2 BCLK*8
0008 2840h	EXDMAC1	EXDMA source address register	EDMSAR	32	32	1 to 2 BCLK*8
0008 2844h	EXDMAC1	EXDMA destination address register	EDMDAR	32	32	1 to 2 BCLK*8
0008 2848h	EXDMAC1	EXDMA transfer count register	EDMCRA	32	32	1 to 2 BCLK*8

Table 4.1 List of I/O Registers (Address Order) (9 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 7125h	ICU	DTC activation enable register 037	DTCER037	8	8	2 ICLK
0008 7128h	ICU	DTC activation enable register 040	DTCER040	8	8	2 ICLK
0008 7129h	ICU	DTC activation enable register 041	DTCER041	8	8	2 ICLK
0008 712Dh	ICU	DTC activation enable register 045	DTCER045	8	8	2 ICLK
0008 712Eh	ICU	DTC activation enable register 046	DTCER046	8	8	2 ICLK
0008 7131h	ICU	DTC activation enable register 049	DTCER049	8	8	2 ICLK
0008 7132h	ICU	DTC activation enable register 050	DTCER050	8	8	2 ICLK
0008 7140h	ICU	DTC activation enable register 064	DTCER064	8	8	2 ICLK
0008 7141h	ICU	DTC activation enable register 065	DTCER065	8	8	2 ICLK
0008 7142h	ICU	DTC activation enable register 066	DTCER066	8	8	2 ICLK
0008 7143h	ICU	DTC activation enable register 067	DTCER067	8	8	2 ICLK
0008 7144h	ICU	DTC activation enable register 068	DTCER068	8	8	2 ICLK
0008 7145h	ICU	DTC activation enable register 069	DTCER069	8	8	2 ICLK
0008 7146h	ICU	DTC activation enable register 070	DTCER070	8	8	2 ICLK
0008 7147h	ICU	DTC activation enable register 071	DTCER071	8	8	2 ICLK
0008 7148h	ICU	DTC activation enable register 072	DTCER072	8	8	2 ICLK
0008 7149h	ICU	DTC activation enable register 073	DTCER073	8	8	2 ICLK
0008 714Ah	ICU	DTC activation enable register 074	DTCER074	8	8	2 ICLK
0008 714Bh	ICU	DTC activation enable register 075	DTCER075	8	8	2 ICLK
0008 714Ch	ICU	DTC activation enable register 076	DTCER076	8	8	2 ICLK
0008 714Dh	ICU	DTC activation enable register 077	DTCER077	8	8	2 ICLK
0008 714Eh	ICU	DTC activation enable register 078	DTCER078	8	8	2 ICLK
0008 714Fh	ICU	DTC activation enable register 079	DTCER079	8	8	2 ICLK
0008 7162h	ICU	DTC activation enable register 098	DTCER098	8	8	2 ICLK
0008 7163h	ICU	DTC activation enable register 099	DTCER099	8	8	2 ICLK
0008 7166h	ICU	DTC activation enable register 102	DTCER102	8	8	2 ICLK
0008 7172h	ICU	DTC activation enable register 114	DTCER114	8	8	2 ICLK
0008 7173h	ICU	DTC activation enable register 115	DTCER115	8	8	2 ICLK
0008 7174h	ICU	DTC activation enable register 116	DTCER116	8	8	2 ICLK
0008 7175h	ICU	DTC activation enable register 117	DTCER117	8	8	2 ICLK
0008 7179h	ICU	DTC activation enable register 121	DTCER121	8	8	2 ICLK
0008 717Ah	ICU	DTC activation enable register 122	DTCER122	8	8	2 ICLK
0008 717Dh	ICU	DTC activation enable register 125	DTCER125	8	8	2 ICLK
0008 717Eh	ICU	DTC activation enable register 126	DTCER126	8	8	2 ICLK
0008 7181h	ICU	DTC activation enable register 129	DTCER129	8	8	2 ICLK
0008 7182h	ICU	DTC activation enable register 130	DTCER130	8	8	2 ICLK
0008 7183h	ICU	DTC activation enable register 131	DTCER131	8	8	2 ICLK
0008 7184h	ICU	DTC activation enable register 132	DTCER132	8	8	2 ICLK
0008 7186h	ICU	DTC activation enable register 134	DTCER134	8	8	2 ICLK
0008 7187h	ICU	DTC activation enable register 135	DTCER135	8	8	2 ICLK
0008 7188h	ICU	DTC activation enable register 136	DTCER136	8	8	2 ICLK
0008 7189h	ICU	DTC activation enable register 137	DTCER137	8	8	2 ICLK
0008 718Ah	ICU	DTC activation enable register 138	DTCER138	8	8	2 ICLK
0008 718Bh	ICU	DTC activation enable register 139	DTCER139	8	8	2 ICLK
0008 718Ch	ICU	DTC activation enable register 140	DTCER140	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (14 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 7505h	ICU	IRQ control register 5	IRQCR5	8	8	2 ICLK
0008 7506h	ICU	IRQ control register 6	IRQCR6	8	8	2 ICLK
0008 7507h	ICU	IRQ control register 7	IRQCR7	8	8	2 ICLK
0008 7508h	ICU	IRQ control register 8	IRQCR8	8	8	2 ICLK
0008 7509h	ICU	IRQ control register 9	IRQCR9	8	8	2 ICLK
0008 750Ah	ICU	IRQ control register 10	IRQCR10	8	8	2 ICLK
0008 750Bh	ICU	IRQ control register 11	IRQCR11	8	8	2 ICLK
0008 750Ch	ICU	IRQ control register 12	IRQCR12	8	8	2 ICLK
0008 750Dh	ICU	IRQ control register 13	IRQCR13	8	8	2 ICLK
0008 750Eh	ICU	IRQ control register 14	IRQCR14	8	8	2 ICLK
0008 750Fh	ICU	IRQ control register 15	IRQCR15	8	8	2 ICLK
0008 7580h	ICU	Non-maskable interrupt status register	NMISR	8	8	2 ICLK
0008 7581h	ICU	Non-maskable interrupt enable register	NMIER	8	8	2 ICLK
0008 7582h	ICU	Non-maskable interrupt clear register	NMICLR	8	8	2 ICLK
0008 7583h	ICU	NMI pin interrupt control register	NMICR	8	8	2 ICLK
0008 8000h	CMT	Compare match timer start register 0	CMSTR0	16	16	2 to 3 PCLK*8
0008 8002h	CMT0	Compare match timer control register	CMCR	16	16	2 to 3 PCLK*8
0008 8004h	CMT0	Compare match timer counter	CMCNT	16	16	2 to 3 PCLK*8
0008 8006h	CMT0	Compare match timer constant register	CMCOR	16	16	2 to 3 PCLK*8
0008 8008h	CMT1	Compare match timer control register	CMCR	16	16	2 to 3 PCLK*8
0008 800Ah	CMT1	Compare match timer counter	CMCNT	16	16	2 to 3 PCLK*8
0008 800Ch	CMT1	Compare match timer constant register	CMCOR	16	16	2 to 3 PCLK*8
0008 8010h	CMT	Compare match timer start register 1	CMSTR1	16	16	2 to 3 PCLK*8
0008 8012h	CMT2	Compare match timer control register	CMCR	16	16	2 to 3 PCLK*8
0008 8014h	CMT2	Compare match timer counter	CMCNT	16	16	2 to 3 PCLK*8
0008 8016h	CMT2	Compare match timer constant register	CMCOR	16	16	2 to 3 PCLK*8
0008 8018h	CMT3	Compare match timer control register	CMCR	16	16	2 to 3 PCLK*8
0008 801Ah	CMT3	Compare match timer counter	CMCNT	16	16	2 to 3 PCLK*8
0008 801Ch	CMT3	Compare match timer constant register	CMCOR	16	16	2 to 3 PCLK*8
0008 8028h	WDT	Timer control/status register	READ.TCSR	8	8	2 to 3 PCLK*8
0008 8028h	WDT	Write window A register	WRITE.WINA	16	16	2 to 3 PCLK*8
0008 8029h	WDT	Timer counter	READ.TCNT	8	8	2 to 3 PCLK*8
0008 802Ah	WDT	Write window B register	WRITE.WINB	16	16	2 to 3 PCLK*8
0008 802Bh	WDT	Reset control/status register	READ.RSTCSR	8	8	2 to 3 PCLK*8
0008 8030h	IWDT	IWDT refresh register	IWDTRR	8	8	2 to 3 PCLK*8
0008 8032h	IWDT	IWDT control register	IWDTCR	16	16	2 to 3 PCLK*8
0008 8034h	IWDT	IWDT status register	IWDTSR	16	16	2 to 3 PCLK*8
0008 8040h	AD0	A/D data register A	ADDRA	16	16	2 to 3 PCLK*8
0008 8042h	AD0	A/D data register B	ADDRB	16	16	2 to 3 PCLK*8
0008 8044h	AD0	A/D data register C	ADDRC	16	16	2 to 3 PCLK*8
0008 8046h	AD0	A/D data register D	ADDRD	16	16	2 to 3 PCLK*8
0008 8050h	AD0	A/D control/status register	ADCSR	8	8	2 to 3 PCLK*8
0008 8051h	AD0	A/D control register	ADCR	8	8	2 to 3 PCLK*8
0008 8052h	AD0	ADDRn format select register	ADDPR	8	8	2 to 3 PCLK*8

Table 4.1 List of I/O Registers (Address Order) (18 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 826Fh	SCI5	Serial extended mode register	SEMR	8	8	2 to 3 PCLK*8
0008 8268h	SMCI5	Serial mode register	SMR	8	8	2 to 3 PCLK*8
0008 8269h	SMCI5	Bit rate register	BRR	8	8	2 to 3 PCLK*8
0008 826Ah	SMCI5	Serial control register	SCR	8	8	2 to 3 PCLK*8
0008 826Bh	SMCI5	Transmit data register	TDR	8	8	2 to 3 PCLK*8
0008 826Ch	SMCI5	Serial status register	SSR	8	8	2 to 3 PCLK*8
0008 826Dh	SMCI5	Receive data register	RDR	8	8	2 to 3 PCLK*8
0008 826Eh	SMCI5	Smart card mode register	SCMR	8	8	2 to 3 PCLK*8
0008 8270h	SCI6	Serial mode register	SMR	8	8	2 to 3 PCLK*8
0008 8271h	SCI6	Bit rate register	BRR	8	8	2 to 3 PCLK*8
0008 8272h	SCI6	Serial control register	SCR	8	8	2 to 3 PCLK*8
0008 8273h	SCI6	Transmit data register	TDR	8	8	2 to 3 PCLK*8
0008 8274h	SCI6	Serial status register	SSR	8	8	2 to 3 PCLK*8
0008 8275h	SCI6	Receive data register	RDR	8	8	2 to 3 PCLK*8
0008 8276h	SCI6	Smart card mode register	SCMR	8	8	2 to 3 PCLK*8
0008 8277h	SCI6	Serial extended mode register	SEMR	8	8	2 to 3 PCLK*8
0008 8270h	SMCI6	Serial mode register	SMR	8	8	2 to 3 PCLK*8
0008 8271h	SMCI6	Bit rate register	BRR	8	8	2 to 3 PCLK*8
0008 8272h	SMCI6	Serial control register	SCR	8	8	2 to 3 PCLK*8
0008 8273h	SMCI6	Transmit data register	TDR	8	8	2 to 3 PCLK*8
0008 8274h	SMCI6	Serial status register	SSR	8	8	2 to 3 PCLK*8
0008 8275h	SMCI6	Receive data register	RDR	8	8	2 to 3 PCLK*8
0008 8276h	SMCI6	Smart card mode register	SCMR	8	8	2 to 3 PCLK*8
0008 8280h	CRC	CRC control register	CRCCR	8	8	2 to 3 PCLK*8
0008 8281h	CRC	CRC data input register	CRCDIR	8	8	2 to 3 PCLK*8
0008 8282h	CRC	CRC data output register	CRCDOR	16	16	2 to 3 PCLK*8
0008 8300h	RIIC0	I2C bus control register 1	ICCR1	8	8	2 to 3 PCLK*8
0008 8301h	RIIC0	I2C bus control register 2	ICCR2	8	8	2 to 3 PCLK*8
0008 8302h	RIIC0	I2C bus mode register 1	ICMR1	8	8	2 to 3 PCLK*8
0008 8303h	RIIC0	I2C bus mode register 2	ICMR2	8	8	2 to 3 PCLK*8
0008 8304h	RIIC0	I2C bus mode register 3	ICMR3	8	8	2 to 3 PCLK*8
0008 8305h	RIIC0	I2C bus function enable register	ICFER	8	8	2 to 3 PCLK*8
0008 8306h	RIIC0	I2C bus status enable register	ICSER	8	8	2 to 3 PCLK*8
0008 8307h	RIIC0	I2C bus interrupt enable register	ICIER	8	8	2 to 3 PCLK*8
0008 8308h	RIIC0	I2C bus status register 1	ICSR1	8	8	2 to 3 PCLK*8
0008 8309h	RIIC0	I2C bus status register 2	ICSR2	8	8	2 to 3 PCLK*8
0008 830Ah	RIIC0	Slave address register L0	SARL0	8	8	2 to 3 PCLK*8
0008 830Ah	RIIC0	Timeout internal counter	TMOCNT	16	16	2 to 3 PCLK*8
0008 830Ah	RIIC0	Timeout internal counter L	TMOCNTL	8	8	2 to 3 PCLK*8
0008 830Bh	RIIC0	Slave address register U0	SARU0	8	8	2 to 3 PCLK*8
0008 830Bh	RIIC0	Timeout internal counter U	TMOCNTU	8	8	2 to 3 PCLK*8
0008 830Ch	RIIC0	Slave address register L1	SARL1	8	8	2 to 3 PCLK*8
0008 830Dh	RIIC0	Slave address register U1	SARU1	8	8	2 to 3 PCLK*8
0008 830Eh	RIIC0	Slave address register L2	SARL2	8	8	2 to 3 PCLK*8
0008 830Fh	RIIC0	Slave address register U2	SARU2	8	8	2 to 3 PCLK*8

Table 4.1 List of I/O Registers (Address Order) (26 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 C023h	PORT3	Data register	DR	8	8	2 to 3 PCLK*8
0008 C024h	PORT4	Data register	DR	8	8	2 to 3 PCLK*8
0008 C025h	PORT5	Data register	DR	8	8	2 to 3 PCLK*8
0008 C026h	PORT6	Data register	DR*6*7	8	8	2 to 3 PCLK*8
0008 C027h	PORT7	Data register	DR*6*7	8	8	2 to 3 PCLK*8
0008 C028h	PORT8	Data register	DR*6*7	8	8	2 to 3 PCLK*8
0008 C029h	PORT9	Data register	DR*6*7	8	8	2 to 3 PCLK*8
0008 C02Ah	PORTA	Data register	DR	8	8	2 to 3 PCLK*8
0008 C02Bh	PORTB	Data register	DR	8	8	2 to 3 PCLK*8
0008 C02Ch	PORTC	Data register	DR	8	8	2 to 3 PCLK*8
0008 C02Dh	PORTD	Data register	DR	8	8	2 to 3 PCLK*8
0008 C02Eh	PORTE	Data register	DR*7	8	8	2 to 3 PCLK*8
0008 C02Fh	PORTF	Data register	DR*5*6*7	8	8	2 to 3 PCLK*8
0008 C030h	PORTG	Data register	DR**5*6*7	8	8	2 to 3 PCLK*8
0008 C040h	PORT0	Port register	PORT	8	8	2 to 3 PCLK*8
0008 C041h	PORT1	Port register	PORT	8	8	2 to 3 PCLK*8
0008 C042h	PORT2	Port register	PORT	8	8	2 to 3 PCLK*8
0008 C043h	PORT3	Port register	PORT	8	8	2 to 3 PCLK*8
0008 C044h	PORT4	Port register	PORT	8	8	2 to 3 PCLK*8
0008 C045h	PORT5	Port register	PORT	8	8	2 to 3 PCLK*8
0008 C046h	PORT6	Port register	PORT*6*7	8	8	2 to 3 PCLK*8
0008 C047h	PORT7	Port register	PORT*6*7	8	8	2 to 3 PCLK*8
0008 C048h	PORT8	Port register	PORT*6*7	8	8	2 to 3 PCLK*8
0008 C049h	PORT9	Port register	PORT*6*7	8	8	2 to 3 PCLK*8
0008 C04Ah	PORTA	Port register	PORT	8	8	2 to 3 PCLK*8
0008 C04Bh	PORTB	Port register	PORT	8	8	2 to 3 PCLK*8
0008 C04Ch	PORTC	Port register	PORT	8	8	2 to 3 PCLK*8
0008 C04Dh	PORTD	Port register	PORT	8	8	2 to 3 PCLK*8
0008 C04Eh	PORTE	Port register	PORT*7	8	8	2 to 3 PCLK*8
0008 C04Fh	PORTF	Port register	PORT*5*6*7	8	8	2 to 3 PCLK*8
0008 C050h	PORTG	Port register	PORT*5*6*7	8	8	2 to 3 PCLK*8
0008 C060h	PORT0	Input buffer control register	ICR	8	8	2 to 3 PCLK*8
0008 C061h	PORT1	Input buffer control register	ICR	8	8	2 to 3 PCLK*8
0008 C062h	PORT2	Input buffer control register	ICR	8	8	2 to 3 PCLK*8
0008 C063h	PORT3	Input buffer control register	ICR	8	8	2 to 3 PCLK*8
0008 C064h	PORT4	Input buffer control register	ICR	8	8	2 to 3 PCLK*8
0008 C065h	PORT5	Input buffer control register	ICR	8	8	2 to 3 PCLK*8
0008 C066h	PORT6	Input buffer control register	ICR*6*7	8	8	2 to 3 PCLK*8
0008 C067h	PORT7	Input buffer control register	ICR*6*7	8	8	2 to 3 PCLK*8
0008 C068h	PORT8	Input buffer control register	ICR*6*7	8	8	2 to 3 PCLK*8
0008 C069h	PORT9	Input buffer control register	ICR*6*7	8	8	2 to 3 PCLK*8
0008 C06Ah	PORTA	Input buffer control register	ICR	8	8	2 to 3 PCLK*8
0008 C06Bh	PORTB	Input buffer control register	ICR	8	8	2 to 3 PCLK*8
0008 C06Ch	PORTC	Input buffer control register	ICR	8	8	2 to 3 PCLK*8
0008 C06Dh	PORTD	Input buffer control register	ICR	8	8	2 to 3 PCLK*8

Table 5.3 DC Characteristics (2)

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
T_a = -40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	All output pins	V_{OH}	VCC-0.5	—	—	V	I_{OH} = -1 mA
Output low voltage	All output pins (except for RIIC pins)	V_{OL}	—	—	0.5	V	I_{OL} = 1.0 mA
	RIIC pins		—	—	0.4	V	I_{OL} = 3.0 mA
			—	—	0.6		I_{OL} = 6.0 mA
	RIIC pins (only P12 and P13 in channel 0)	V_{OL}	—	—	0.4	V	I_{OL} = 15.0 mA (ICFER.FMPE = 1)
			—	0.4	—		I_{OL} = 20.0 mA (ICFER.FMPE = 1)
Input leakage current	RES#, MD pin, EMLE, NMI	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	Ports 03, 05, 10, 11, 14, 15 ports 22 to 27 ports 30 to 32, 34, 35 ports 4 to G	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0 V V_{in} = VCC
	Ports 00 to 02, 07, 12, 13 Ports 16, 17, 20, 21, 33		—	—	5.0		
Input pull-up MOS current	Ports 9 to E, G	$-I_p$	10	—	300	µA	VCC = 2.7 to 3.6 V V_{in} = 0 V
Input capacitance	All input pins (except for ports 12, 13, 20, 21 ports 40 to 47, and EMLE)	C_{in}	—	—	15	pF	V_{in} = 0 V f = 1 MHz T_a = 25°C
	Ports 12, 13, 20, 21, Ports 40 to 47, EMLE		—	—	30		

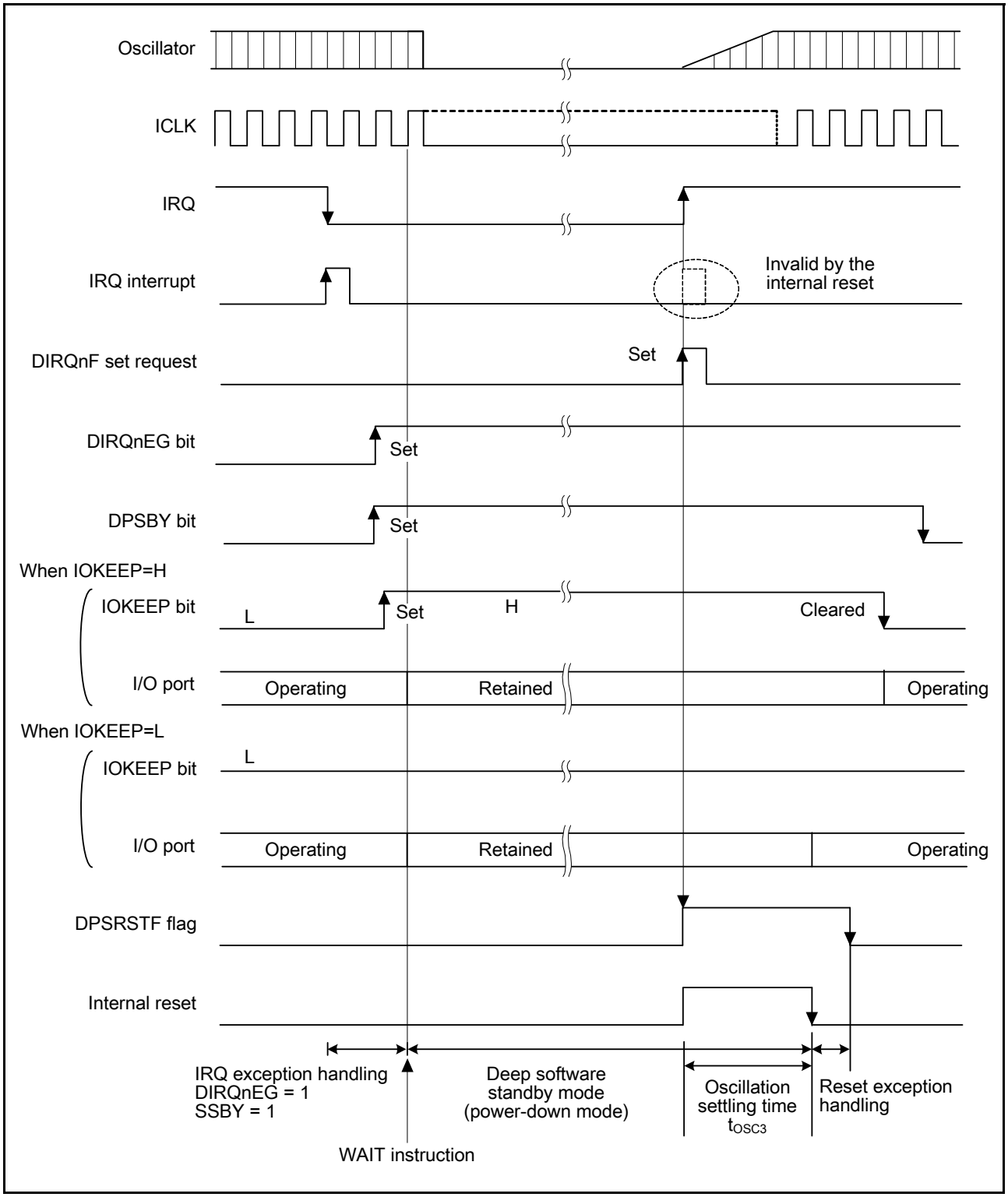

Figure 5.4 Oscillation Settling Timing after Deep Software Standby Mode

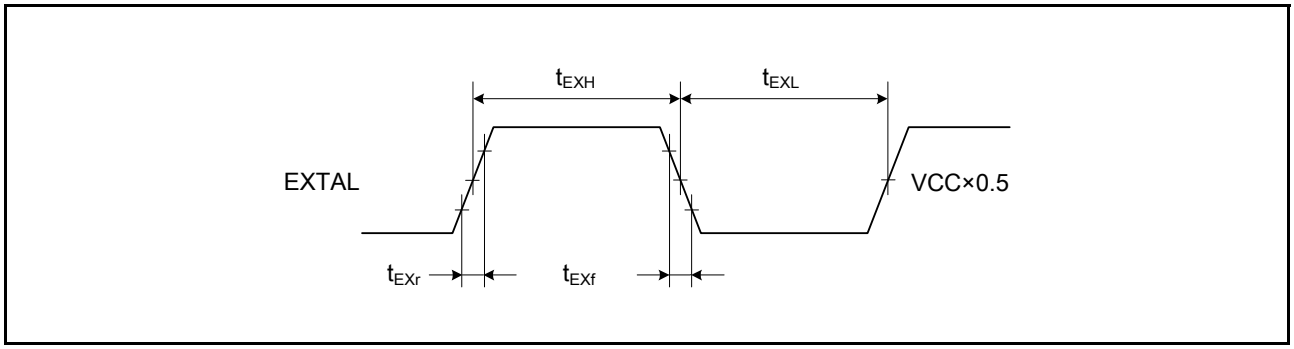

Figure 5.5 EXTAL External Input Clock Timing

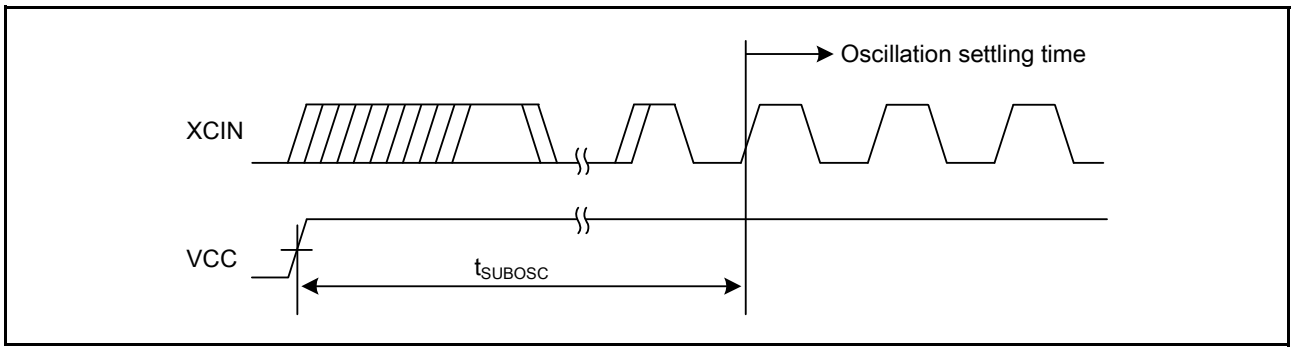

Figure 5.6 XCIN Sub-Clock Oscillation Settling Time

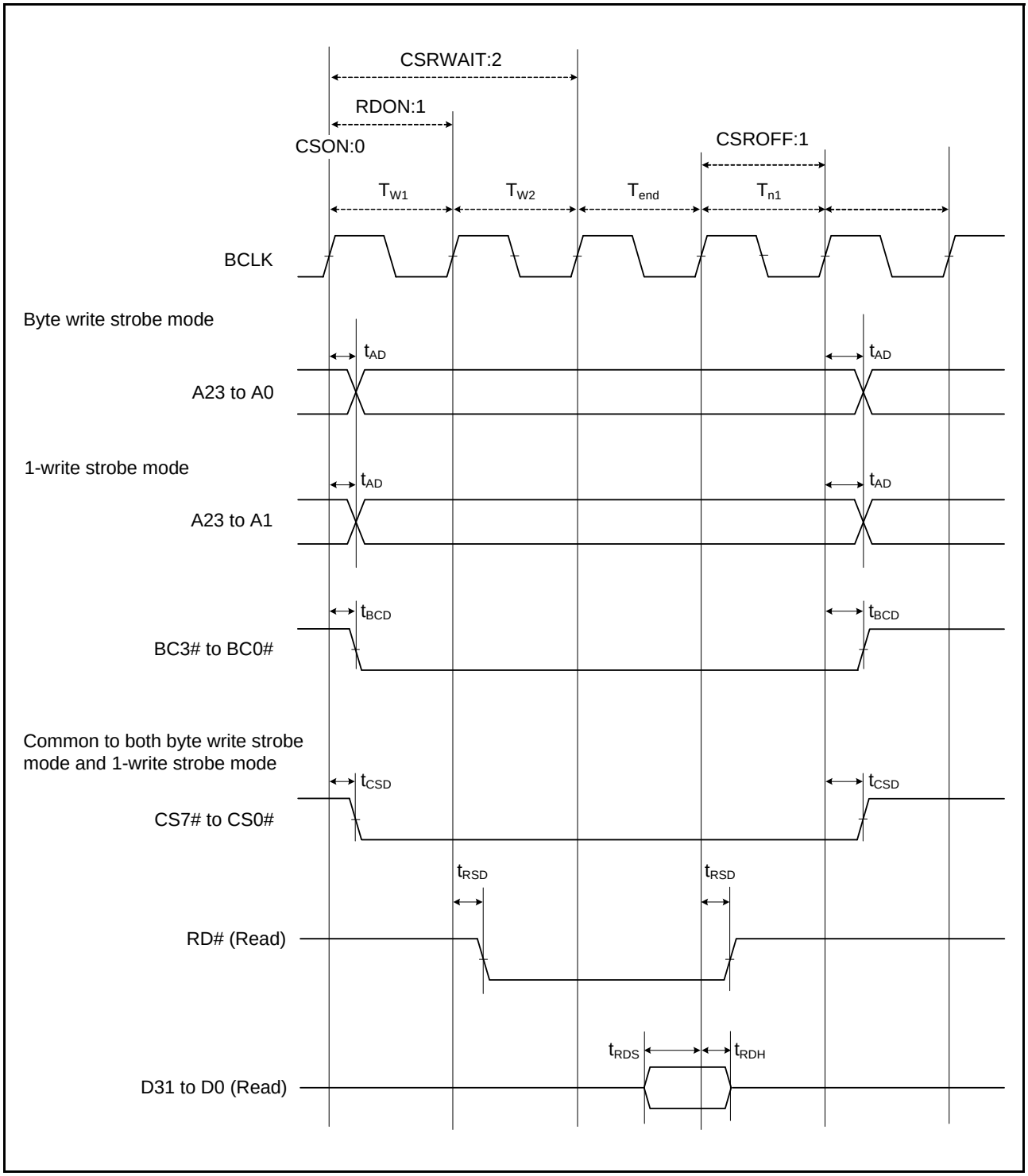

Figure 5.10 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)

Table 5.14 Timing of On-Chip Peripheral Modules (4)

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
PCLK = 8 to 50 MHz
T_a = -40 to +85°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
RSPI	Data input setup time	Master [176-pin LFBGA/ 145-pin TFLGA/ 144-pin LQFP]	t_{SU}	16	—	ns	Figure 5.39 to Figure 5.42
		Master [100-pin LQFP/ 85-pin TFLGA]		30	—		
		Slave		20-2 × t_{Pcyc}	—		
	Data input hold time	Master	t_H	0	—	ns	
		Slave		20+2 × t_{Pcyc}	—		
	SSL setup time	Master	t_{LEAD}	1	8	t_{SPcyc}	
		Slave		4	—	t_{Pcyc}	
	SSL hold time	Master	t_{LAG}	1	8	t_{SPcyc}	
		Slave		4	—	t_{Pcyc}	
	Data output delay time	Master [176-pin LFBGA/ 145-pin TFLGA/ 144-pin LQFP]	t_{OD}	—	20	ns	
		Master [100-pin LQFP/ 85-pin TFLGA]		—	30		
		Slave [176-pin LFBGA/ 145-pin TFLGA/ 144-pin LQFP]		—	3 × t_{Pcyc}+40		
		Slave [100-pin LQFP/ 85-pin TFLGA]		—	3 × t_{Pcyc}+50		

Note 1. tPcyc: PCLK cycle

Table 5.16 Timing of On-Chip Peripheral Modules (6)

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
PCLK = 8 to 50 MHz
T_a = -40 to +85°C

Item		Symbol	Min.*1*2	Max.	Unit	Test Conditions
RIIC (Standard-mode, SMBus) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 1300	—	ns	Figure 5.43
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rising time	t_{Sr}	—	1000	ns	
	SCL, SDA input falling time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Re-start condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast-mode)	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 600	—	ns	
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rising time	t_{Sr}	20+0.1C_b	300	ns	
	SCL, SDA input falling time	t_{Sf}	20+0.1C_b	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Re-start condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc}: RIIC internal reference clock (IICφ) cycles
Note 1. The value in parentheses is used when ICMR3.NF[1:0] are set to 11b while a digital filter is enabled with ICFER.NFE = 1.
Note 2. C_b indicates the total capacity of the bus line.

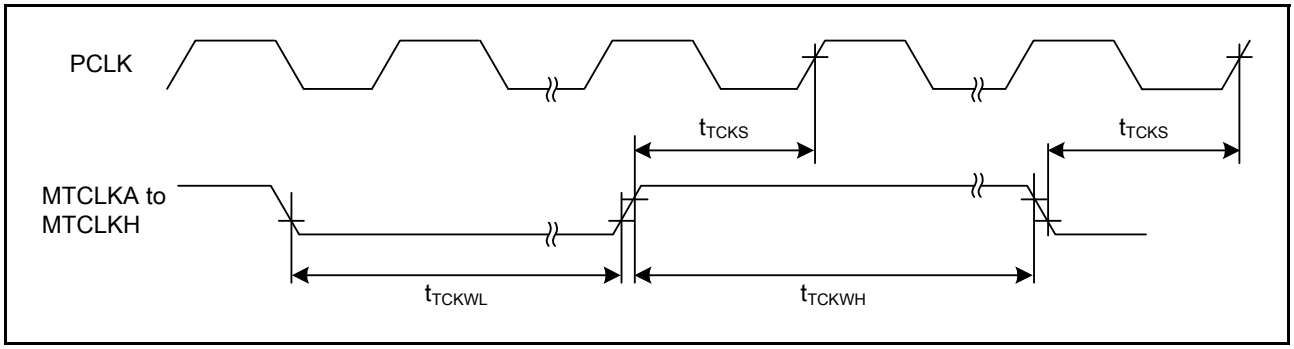

Figure 5.27 MTU2 Clock Input Timing

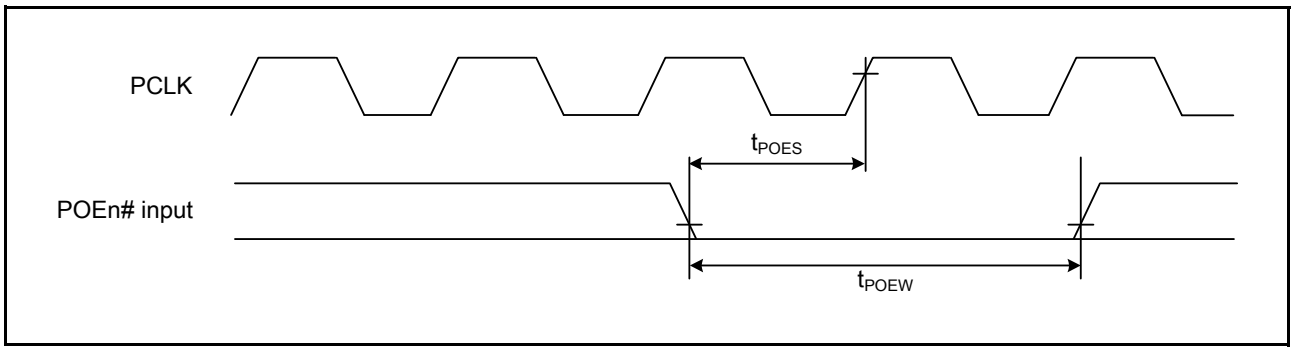

Figure 5.28 POE# Input Timing

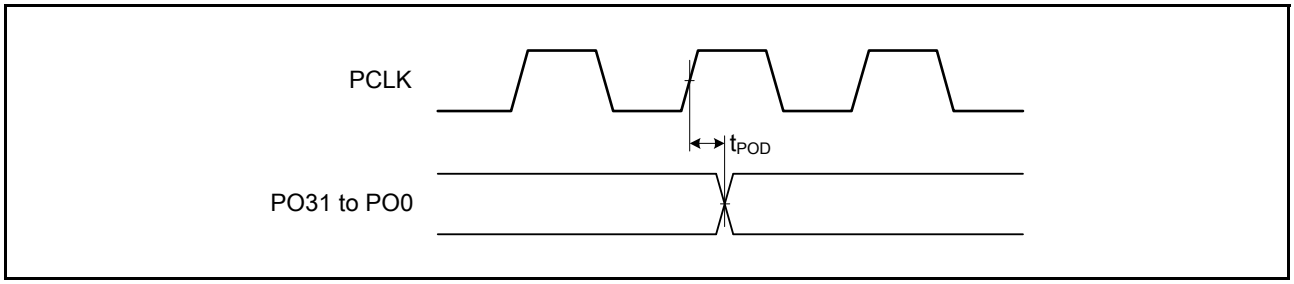

Figure 5.29 PPG Output Timing

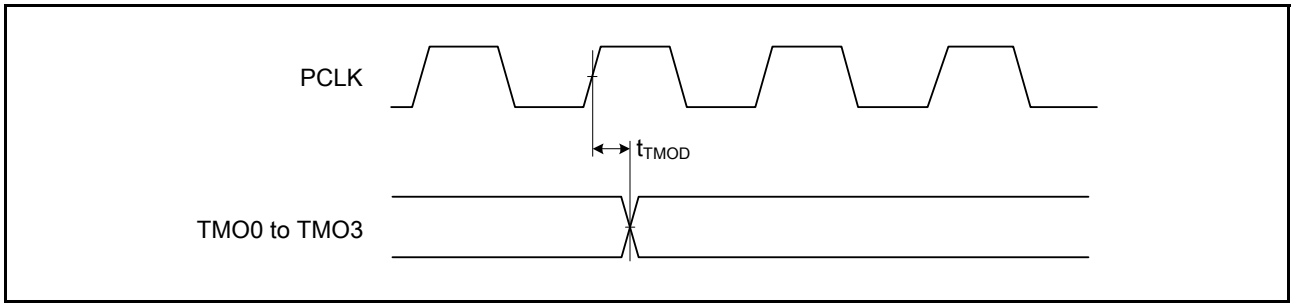

Figure 5.30 8-Bit Timer Output Timing

5.4 USB Characteristics

Table 5.19 Internal USB Full-Speed Characteristics (DP, DM Pin Characteristics)

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 3.0 to 3.6 V, VREFH = 3.0 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
PCLK = 24 to 50 MHz
T_a = -40 to +85°C

Item		Symbol	Min.	Max.	Unit	Test Conditions	
Input characteristics	Input high level voltage	V_{IH}	2.0	—	V		Figure 5.61 and Figure 5.62
	Input low level voltage	V_{IL}	—	0.8	V		
	Differential input Sensitivity	V_{DI}	0.2	—	V	| DP — DM |	
	Differential commom mode range	V_{CM}	0.8	2.5	V		
Output characteristics	Output high level voltage	V_{OH}	2.8	3.6	V	I_{OH} = -200µA	
	Output low level voltage	V_{OL}	0.0	0.3	V	I_{OL} = 2 mA	
	Cross over voltage	V_{CRS}	1.3	2.0	V		
	Rising time	t_{Lr}	4	20	ns		
	Falling time	t_{Lf}	4	20	ns		
	Rising/falling time ratio	t_{Lr} / t_{Lf}	90	111.11	%	t_{Lr} / t_{Lf}	
	Output resistance	Z_{DRV}	28	44	Ω	Rs = 22Ω included	

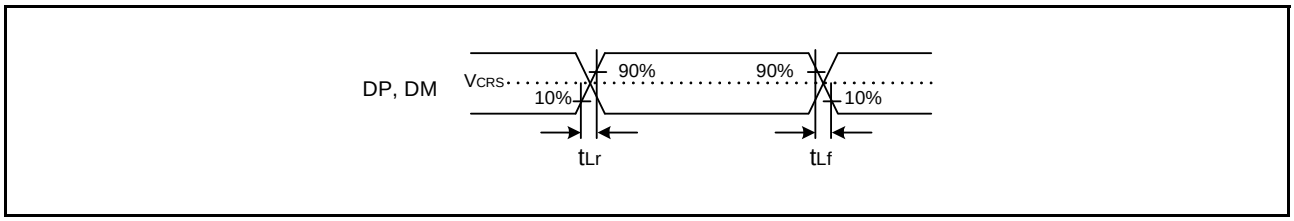

Figure 5.61 DP, DM Output Timing (Full-Speed)

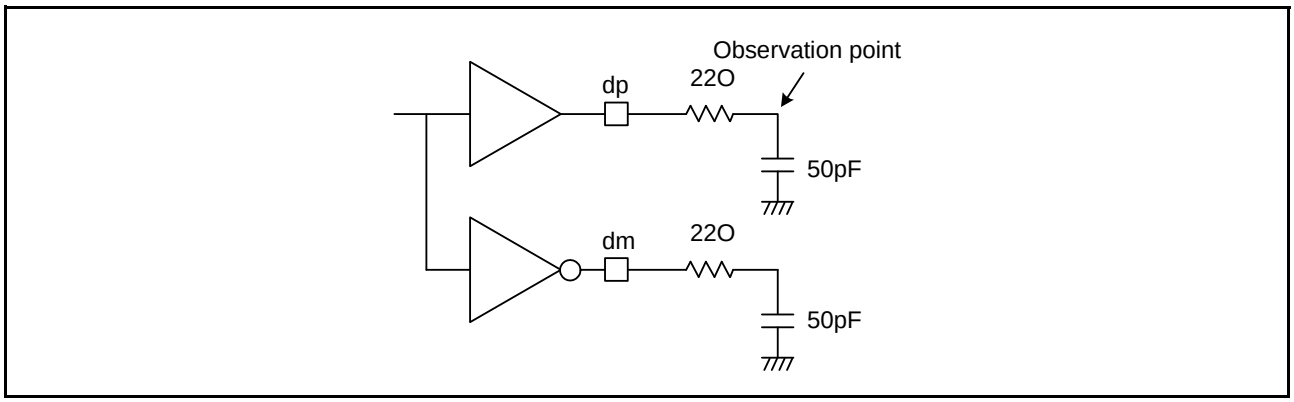

Figure 5.62 Test Circuit (Full-Speed)

5.5 A/D Conversion Characteristics

Table 5.20 10-Bit A/D Conversion Characteristics

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
PCLK = 8 to 50 MHz
T_a = -40 to +85°C

Item			Min.	Typ.	Max.	Unit	Test Conditions
Resolution			10	10	10	bits	
Conversion time*1 (PCLK = 50-MHz operation)	With 0.1-µF external capacitor	When the capacitor is charged enough*2	0.8 (0.3)*3	—	—	µs	Sampling 15 states
	Without external capacitor	Permissible signal source impedance (max.) = 1.0 kΩ	1.0 (0.5)*3	—	—		Sampling 25 states
		Permissible signal source impedance (max.) = 5.0 kΩ	2.6 (2.1)*3	—	—		Sampling 105 states
Analog input capacitance			—	—	6.0	pF	
INL integral nonlinearity error			—	±1.5	±3.0	LSB	
Offset error			—	±1.5	±3.0	LSB	
Full-scale error			—	±1.5	±3.0	LSB	
Quantization error			—	±0.5	—	LSB	
Absolute accuracy			—	±1.5	±3.0	LSB	
DNL differential nonlinearity error			—	±0.5	±1.0	LSB	

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.
Note 2. The scanning is not supported.
Note 3. The value in parentheses indicates the sampling time.

Table 5.21 12-Bit A/D Conversion Characteristics

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
PCLK = 8 to 50 MHz
T_a = -40 to +85°C

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	12	12	12	bits	
Conversion time*1	1.0	—	—	µs	AVCC ≥ 3.0
	2.0	—	—	µs	AVCC ≥ 2.7
Analog input capacitance	—	—	30	pF	
Offset error	—	±2.0	±7.5	LSB	
Full-scale error	—	±2.0	±7.5	LSB	
Quantization error	—	±0.5	—	LSB	
Absolute accuracy	—	±2.5	±8.0	LSB	
Nonlinearity error	—	±2.0	±4.0	LSB	

Note 1. The time conversion takes is the sum of the sampling interval and the time comparison takes (permissible signal-source impedance is up to 1.0 kΩ)