Renesas Electronics America Inc - R5F56218BDFB#V0 Datasheet

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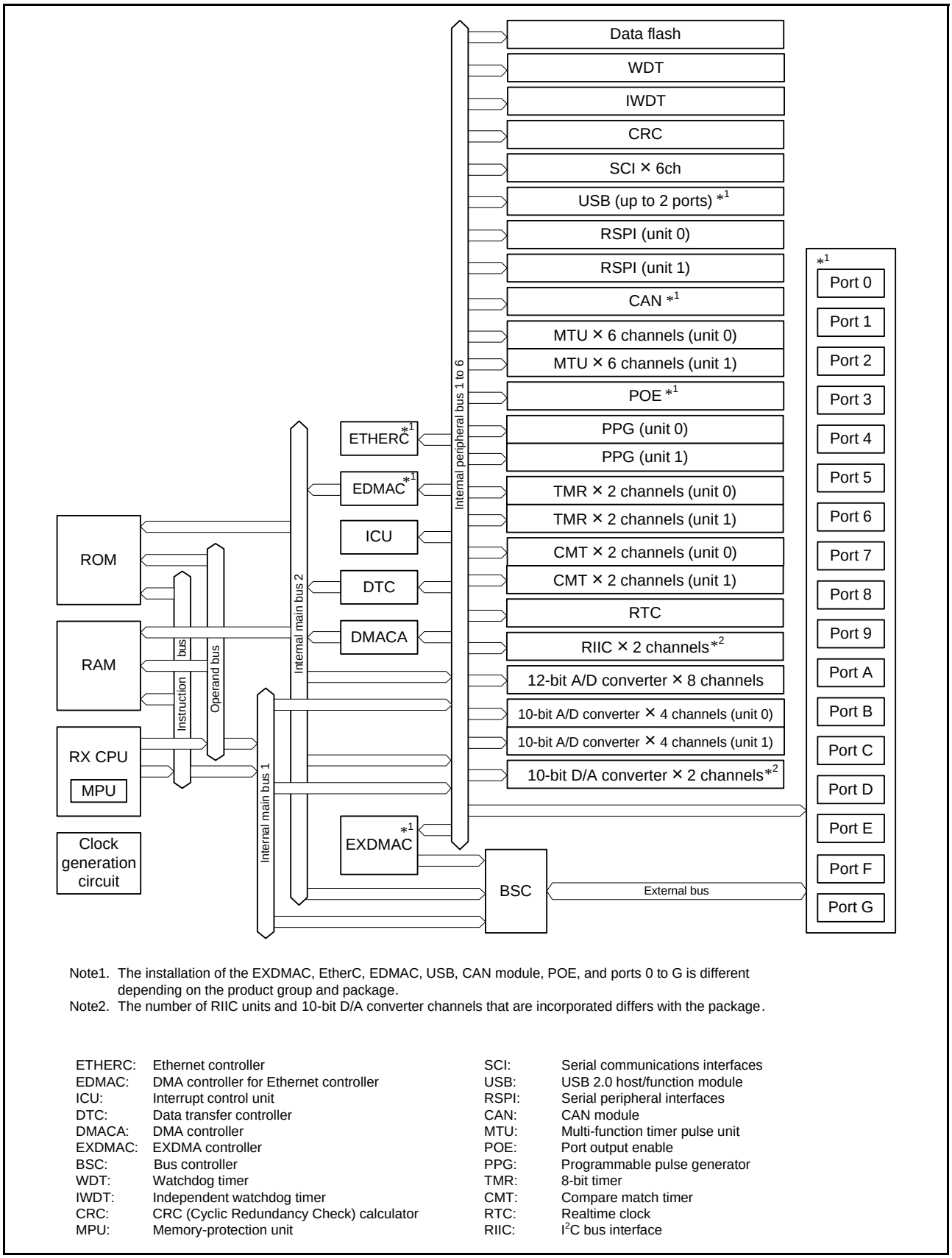
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	103
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10/12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f56218bdfb-v0

1.3 Block Diagram

Figure 1.2 shows a block diagram.



Note1. The installation of the EXDMAC, EtherC, EDMAC, USB, CAN module, POE, and ports 0 to G is different depending on the product group and package.
Note2. The number of RIIC units and 10-bit D/A converter channels that are incorporated differs with the package.

ETHERC:	Ethernet controller	SCI:	Serial communications interfaces
EDMAC:	DMA controller for Ethernet controller	USB:	USB 2.0 host/function module
ICU:	Interrupt control unit	RSPI:	Serial peripheral interfaces
DTC:	Data transfer controller	CAN:	CAN module
DMACA:	DMA controller	MTU:	Multi-function timer pulse unit
EXDMAC:	EXDMA controller	POE:	Port output enable
BSC:	Bus controller	PPG:	Programmable pulse generator
WDT:	Watchdog timer	TMR:	8-bit timer
IWDT:	Independent watchdog timer	CMT:	Compare match timer
CRC:	CRC (Cyclic Redundancy Check) calculator	RTC:	Realtime clock
MPU:	Memory-protection unit	RIIC:	I^2C bus interface

Figure 1.2 Block Diagram

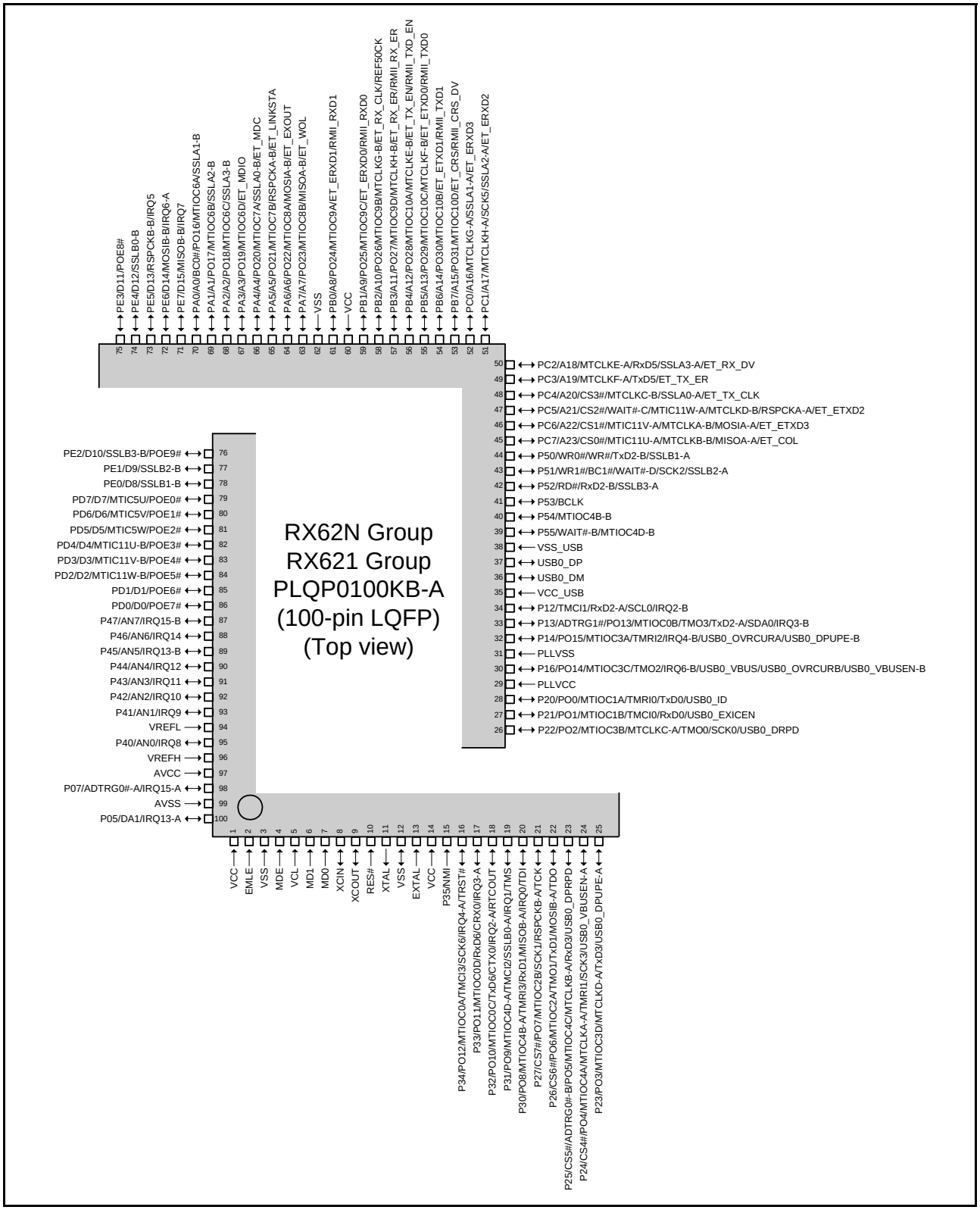


Figure 1.8 Pin Assignment of the 100-Pin LQFP (Assistance Diagram)

Table 1.7 List of Pins and Pin Functions (100-Pin LQFP) (2 / 4)

Pin No. 100-Pin LQFP	Power Supply Clock System Control	I/O Port	External Bus	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
27		P21			USB0_EXICEN	MTIOC1B/ TMCI0/ PO1	RxD0	
28		P20			USB0_ID	MTIOC1A/ TMRI0/ PO0	TxD0	
29	PLLVCC							
30		P16			USB0_VBUS/ USB0_OVRCURB/ USB0_VBUSEN-B	MTIOC3C/ TMO2/ PO14		IRQ6-B
31	PLLVSS							
32		P14			USB0_OVRCURA/ USB0_DPUPE-B	MTIOC3A/ TMRI2/ PO15		IRQ4-B
33		P13				MTIOC0B/ TMO3/ PO13	SDA0/ TxD2-A	IRQ3-B/ ADTRG1#
34		P12				TMCI1	SCL0/ RxD2-A	IRQ2-B
35	VCC_USB							
36					USB0_DM			
37					USB0_DP			
38	VSS_USB							
39		P55	WAIT#-B			MTIOC4D-B		
40		P54				MTIOC4B-B		
41	BCLK	P53						
42		P52	RD#				SSLB3-A/ RxD2-B	
43		P51	WR1#/BC1#/ WAIT#-D				SSLB2-A/ SCK2	
44		P50	WR0#/ WR#				SSLB1-A/ TxD2-B	
45		PC7	A23/ CS0#	ET_COL		MTIC11U-A/ MTCLKB-B	MISOA-A	
46		PC6	A22/ CS1#	ET_ETXD3		MTIC11V-A/ MTCLKA-B	MOSIA-A	
47		PC5	A21/CS2#/ WAIT#-C	ET_ETXD2		MTIC11W-A/ MTCLKD-B	RSPCKA-A	
48		PC4	A20/CS3#	ET_TX_CLK		MTCLKC-B	SSLA0-A	
49		PC3	A19	ET_TX_ER		MTCLKF-A	TxD5	
50		PC2	A18	ET_RX_DV		MTCLKE-A	SSLA3-A/ RxD5	
51		PC1	A17	ET_ERXD2		MTCLKH-A	SSLA2-A/ SCK5	
52		PC0	A16	ET_ERXD3		MTCLKG-A	SSLA1-A	

Table 1.9 Pin Functions (6 / 7)

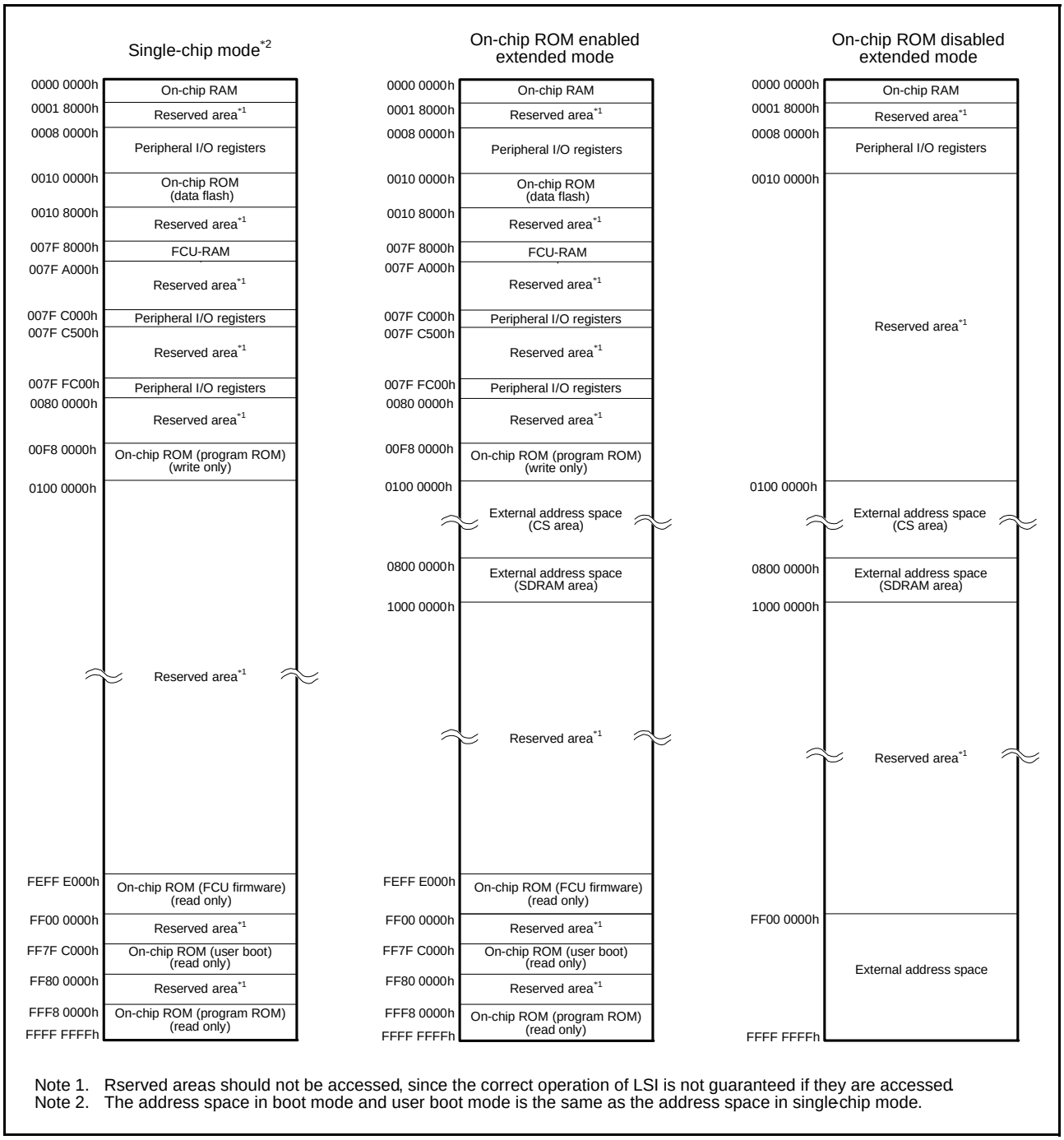
Classifications	Pin Name	I/O	Description
USB 2.0 host/function module	VCC_USB	Input	Power-supply pin for the USB. Connect this pin to the system power supply even when the USB is not to be used.
	VSS_USB	Input	Ground pin for the USB. Connect this pin to the system power supply (0 V) even when the USB is not to be used.
	USB0_DP USB1_DP	I/O	Inputs or outputs D+ data for the USB bus.
	USB0_DM USB1_DM	I/O	Inputs or outputs D- data for the USB bus.
	USB0_DPRPD USB1_DPRPD	Output	Enable D+ pull-down.
	USB0_DRPD USB1_DRPD	Output	Enable D- pull-down.
	USB0_EXICEN USB1_EXICEN	Output	Connect these pins to the OTG power supply IC.
	USB0_ID USB1_ID	Input	Connect these pins to the OTG power supply IC.
	USB0_VBUSEN-A/ USB0_VBUSEN-B USB1_VBUSEN-A/ USB1_VBUSEN-B	Output	VBUS power enable pins for the USB.
	USB0_DPUPE-A/ USB0_DPUPE-B USB1_DPUPE-A/ USB1_DPUPE-B	Output	Pull-up pins for the USB.
	USB0_OVRCURA/ USB0_OVRCURB USB1_OVRCURA/ USB1_OVRCURB	Input	Over current pins for the USB.
	USB0_VBUS USB1_VBUS	Input	Input pins for detection of connection and disconnection of the USB cable.
CAN module	CRX0	Input	Input pins for the CAN.
	CTX0	Output	Output pins for the CAN.
Serial peripheral interfaces	RSPCKA-A/ RSPCKA-B	I/O	Clock input/output pins for the RSPI.
	RSPCKB-A/ RSPCKB-B	I/O	Clock input/output pins for the RSPI
	MOSIA-A/MOSIA-B MOSIB-A/MOSIB-B	I/O	Input or output data output from the master for the RSPI.
	MISOA-A/MISOA-B MISOB-A/MISOB-B	I/O	Input or output data output from the slave for the RSPI.
	SSLA0-A/SSLA0-B	I/O	Select the slave for the RSPI.
	SSLA1-A/SSLA1-B SSLA2-A/SSLA2-B SSLA3-A/SSLA3-B	Output	
	SSLB0-A/SSLB0-B	I/O	
	SSLB1-A/SSLB1-B SSLB2-A/SSLB2-B SSLB3-A/SSLB3-B	Output	
Realtime clock	RTCOUT	Output	Output pin for 1-Hz clock.
A/D converter	AN0 to AN7	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRG0#-A/ADTRG0#-B ADTRG1#	Input	Input pins for the external trigger signals that start the A/D conversion.
D/A converter	DA0, DA1	Output	Output pins for the analog signals from the D/A converter.

3. Address Space

3.1 Address Space

This LSI has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.

Figure 3.1 shows the memory maps in the respective operating modes. Accessible areas will differ according to the operating mode and states of control bits.



Note 1. Rserved areas should not be accessed, since the correct operation of LSI is not guaranteed if they are accessed.
Note 2. The address space in boot mode and user boot mode is the same as the address space in single-chip mode.

Figure 3.1 Memory Map in Each Operating Mode

4. I/O Registers

Table 4.1 List of I/O Registers (Address Order) (1 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 0000h	SYSTEM	Mode monitor register	MDMONR	16	16	3 ICLK
0008 0002h	SYSTEM	Mode status register	MDSR	16	16	3 ICLK
0008 0006h	SYSTEM	System control register 0	SYSCR0	16	16	3 ICLK
0008 0008h	SYSTEM	System control register 1	SYSCR1	16	16	3 ICLK
0008 000Ch	SYSTEM	Standby control register	SBYCR	16	16	3 ICLK
0008 0010h	SYSTEM	Module stop control register A	MSTPCRA	32	32	3 ICLK
0008 0014h	SYSTEM	Module stop control register B	MSTPCRB	32	32	3 ICLK
0008 0018h	SYSTEM	Module stop control register C	MSTPCRC	32	32	3 ICLK
0008 0020h	SYSTEM	System clock control register	SCKCR	32	32	3 ICLK
0008 0030h	SYSTEM	External bus clock control register	BCKCR	8	8	3 ICLK
0008 0040h	SYSTEM	Oscillation stop detection control register	OSTDCR	16	16	3 ICLK
0008 1300h	BSC	Bus error status clear register	BERCLR	8	8	2 ICLK
0008 1304h	BSC	Bus error monitoring enable register	BEREN	8	8	2 ICLK
0008 1308h	BSC	Bus error status register 1	BERSR1	8	8	2 ICLK
0008 130Ah	BSC	Bus error status register 2	BERSR2	16	16	2 ICLK
0008 2000h	DMAC0	DMA source address register	DMSAR	32	32	2 ICLK
0008 2004h	DMAC0	DMA destination address register	DMDAR	32	32	2 ICLK
0008 2008h	DMAC0	DMA transfer count register	DMCRA	32	32	2 ICLK
0008 200Ch	DMAC0	DMA block transfer count register	DMCRB	16	16	2 ICLK
0008 2010h	DMAC0	DMA transfer mode register	DMTMD	16	16	2 ICLK
0008 2013h	DMAC0	DMA interrupt setting register	DMINT	8	8	2 ICLK
0008 2014h	DMAC0	DMA address mode register	DMAMD	16	16	2 ICLK
0008 2018h	DMAC0	DMA offset register	DMOFR	32	32	2 ICLK
0008 201Ch	DMAC0	MA transfer enable register	DMCNT	8	8	2 ICLK
0008 201Dh	DMAC0	DMA software start register	DMREQ	8	8	2 ICLK
0008 201Eh	DMAC0	DMA status register	DMSTS	8	8	2 ICLK
0008 201Fh	DMAC0	DMA activation source flag control register	DMCSL	8	8	2 ICLK
0008 2040h	DMAC1	DMA source address register	DMSAR	32	32	2 ICLK
0008 2044h	DMAC1	DMA destination address register	DMDAR	32	32	2 ICLK
0008 2048h	DMAC1	DMA transfer count register	DMCRA	32	32	2 ICLK
0008 204Ch	DMAC1	DMA block transfer count register	DMCRB	16	16	2 ICLK
0008 2050h	DMAC1	DMA transfer mode register	DMTMD	16	16	2 ICLK
0008 2053h	DMAC1	DMA interrupt setting register	DMINT	8	8	2 ICLK
0008 2054h	DMAC1	DMA address mode register	DMAMD	16	16	2 ICLK
0008 205Ch	DMAC1	MA transfer enable register	DMCNT	8	8	2 ICLK
0008 205Dh	DMAC1	DMA software start register	DMREQ	8	8	2 ICLK
0008 205Eh	DMAC1	DMA status register	DMSTS	8	8	2 ICLK
0008 205Fh	DMAC1	DMA activation source flag control register	DMCSL	8	8	2 ICLK
0008 2080h	DMAC2	DMA source address register	DMSAR	32	32	2 ICLK
0008 2084h	DMAC2	DMA destination address register	DMDAR	32	32	2 ICLK
0008 2088h	DMAC2	DMA transfer count register	DMCRA	32	32	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (7 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 708Ch	ICU	Interrupt request register 140	IR140	8	8	2 ICLK
0008 708Dh	ICU	Interrupt request register 141	IR141	8	8	2 ICLK
0008 708Eh	ICU	Interrupt request register 142	IR142	8	8	2 ICLK
0008 708Fh	ICU	Interrupt request register 143	IR143	8	8	2 ICLK
0008 7090h	ICU	Interrupt request register 144	IR144	8	8	2 ICLK
0008 7091h	ICU	Interrupt request register 145	IR145	8	8	2 ICLK
0008 7092h	ICU	Interrupt request register 146	IR146	8	8	2 ICLK
0008 7093h	ICU	Interrupt request register 147	IR147	8	8	2 ICLK
0008 7094h	ICU	Interrupt request register 148	IR148	8	8	2 ICLK
0008 7095h	ICU	Interrupt request register 149	IR149	8	8	2 ICLK
0008 7096h	ICU	Interrupt request register 150	IR150	8	8	2 ICLK
0008 7097h	ICU	Interrupt request register 151	IR151	8	8	2 ICLK
0008 7098h	ICU	Interrupt request register 152	IR152	8	8	2 ICLK
0008 7099h	ICU	Interrupt request register 153	IR153	8	8	2 ICLK
0008 709Ah	ICU	Interrupt request register 154	IR154	8	8	2 ICLK
0008 709Bh	ICU	Interrupt request register 155	IR155	8	8	2 ICLK
0008 709Ch	ICU	Interrupt request register 156	IR156	8	8	2 ICLK
0008 709Dh	ICU	Interrupt request register 157	IR157	8	8	2 ICLK
0008 709Eh	ICU	Interrupt request register 158	IR158	8	8	2 ICLK
0008 709Fh	ICU	Interrupt request register 159	IR159	8	8	2 ICLK
0008 70A0h	ICU	Interrupt request register 160	IR160	8	8	2 ICLK
0008 70A1h	ICU	Interrupt request register 161	IR161	8	8	2 ICLK
0008 70A2h	ICU	Interrupt request register 162	IR162	8	8	2 ICLK
0008 70A3h	ICU	Interrupt request register 163	IR163	8	8	2 ICLK
0008 70A4h	ICU	Interrupt request register 164	IR164	8	8	2 ICLK
0008 70A5h	ICU	Interrupt request register 165	IR165	8	8	2 ICLK
0008 70A6h	ICU	Interrupt request register 166	IR166	8	8	2 ICLK
0008 70A7h	ICU	Interrupt request register 167	IR167	8	8	2 ICLK
0008 70A8h	ICU	Interrupt request register 168	IR168	8	8	2 ICLK
0008 70A9h	ICU	Interrupt request register 169	IR169	8	8	2 ICLK
0008 70AAh	ICU	Interrupt request register 170	IR170	8	8	2 ICLK
0008 70ABh	ICU	Interrupt request register 171	IR171	8	8	2 ICLK
0008 70ACh	ICU	Interrupt request register 172	IR172	8	8	2 ICLK
0008 70ADh	ICU	Interrupt request register 173	IR173	8	8	2 ICLK
0008 70AEh	ICU	Interrupt request register 174	IR174	8	8	2 ICLK
0008 70AFh	ICU	Interrupt request register 175	IR175	8	8	2 ICLK
0008 70B0h	ICU	Interrupt request register 176	IR176	8	8	2 ICLK
0008 70B1h	ICU	Interrupt request register 177	IR177	8	8	2 ICLK
0008 70B2h	ICU	Interrupt request register 178	IR178	8	8	2 ICLK
0008 70B3h	ICU	Interrupt request register 179	IR179	8	8	2 ICLK
0008 70B4h	ICU	Interrupt request register 180	IR180	8	8	2 ICLK
0008 70B5h	ICU	Interrupt request register 181	IR181	8	8	2 ICLK
0008 70B6h	ICU	Interrupt request register 182	IR182	8	8	2 ICLK
0008 70B7h	ICU	Interrupt request register 183	IR183	8	8	2 ICLK
0008 70B8h	ICU	Interrupt request register 184	IR184	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (11 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 71EFh	ICU	DTC activation enable register 239	DTCER239	8	8	2 ICLK
0008 71F0h	ICU	DTC activation enable register 240	DTCER240	8	8	2 ICLK
0008 71F7h	ICU	DTC activation enable register 247	DTCER247	8	8	2 ICLK
0008 71F8h	ICU	DTC activation enable register 248	DTCER248	8	8	2 ICLK
0008 71FBh	ICU	DTC activation enable register 251	DTCER251	8	8	2 ICLK
0008 71FCh	ICU	DTC activation enable register 252	DTCER252	8	8	2 ICLK
0008 7202h	ICU	Interrupt request enable register 02	IER02	8	8	2 ICLK
0008 7203h	ICU	Interrupt request enable register 03	IER03	8	8	2 ICLK
0008 7204h	ICU	Interrupt request enable register 04	IER04	8	8	2 ICLK
0008 7205h	ICU	Interrupt request enable register 05	IER05	8	8	2 ICLK
0008 7206h	ICU	Interrupt request enable register 06	IER06	8	8	2 ICLK
0008 7207h	ICU	Interrupt request enable register 07	IER07	8	8	2 ICLK
0008 7208h	ICU	Interrupt request enable register 08	IER08	8	8	2 ICLK
0008 7209h	ICU	Interrupt request enable register 09	IER09	8	8	2 ICLK
0008 720Bh	ICU	Interrupt request enable register 0B	IER0B	8	8	2 ICLK
0008 720Ch	ICU	Interrupt request enable register 0C	IER0C	8	8	2 ICLK
0008 720Eh	ICU	Interrupt request enable register 0E	IER0E	8	8	2 ICLK
0008 720Fh	ICU	Interrupt request enable register 0F	IER0F	8	8	2 ICLK
0008 7210h	ICU	Interrupt request enable register 10	IER10	8	8	2 ICLK
0008 7211h	ICU	Interrupt request enable register 11	IER11	8	8	2 ICLK
0008 7212h	ICU	Interrupt request enable register 12	IER12	8	8	2 ICLK
0008 7213h	ICU	Interrupt request enable register 13	IER13	8	8	2 ICLK
0008 7214h	ICU	Interrupt request enable register 14	IER14	8	8	2 ICLK
0008 7215h	ICU	Interrupt request enable register 15	IER15	8	8	2 ICLK
0008 7216h	ICU	Interrupt request enable register 16	IER16	8	8	2 ICLK
0008 7217h	ICU	Interrupt request enable register 17	IER17	8	8	2 ICLK
0008 7218h	ICU	Interrupt request enable register 18	IER18	8	8	2 ICLK
0008 7219h	ICU	Interrupt request enable register 19	IER19	8	8	2 ICLK
0008 721Ah	ICU	Interrupt request enable register 1A	IER1A	8	8	2 ICLK
0008 721Bh	ICU	Interrupt request enable register 1B	IER1B	8	8	2 ICLK
0008 721Ch	ICU	Interrupt request enable register 1C	IER1C	8	8	2 ICLK
0008 721Dh	ICU	Interrupt request enable register 1D	IER1D	8	8	2 ICLK
0008 721Eh	ICU	Interrupt request enable register 1E	IER1E	8	8	2 ICLK
0008 721Fh	ICU	Interrupt request enable register 1F	IER1F	8	8	2 ICLK
0008 72E0h	ICU	Software interrupt activation register	SWINTR	8	8	2 ICLK
0008 72F0h	ICU	Fast interrupt set register	FIR	16	16	2 ICLK
0008 7300h	ICU	Interrupt source priority register 00	IPR00	8	8	2 ICLK
0008 7301h	ICU	Interrupt source priority register 01	IPR01	8	8	2 ICLK
0008 7302h	ICU	Interrupt source priority register 02	IPR02	8	8	2 ICLK
0008 7303h	ICU	Interrupt source priority register 03	IPR03	8	8	2 ICLK
0008 7304h	ICU	Interrupt source priority register 04	IPR04	8	8	2 ICLK
0008 7305h	ICU	Interrupt source priority register 05	IPR05	8	8	2 ICLK
0008 7306h	ICU	Interrupt source priority register 06	IPR06	8	8	2 ICLK
0008 7307h	ICU	Interrupt source priority register 07	IPR07	8	8	2 ICLK
0008 7308h	ICU	Interrupt source priority register 08	IPR08	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (13 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 735Ch	ICU	Interrupt source priority register 5C	IPR5C	8	8	2 ICLK
0008 735Dh	ICU	Interrupt source priority register 5D	IPR5D	8	8	2 ICLK
0008 735Eh	ICU	Interrupt source priority register 5E	IPR5E	8	8	2 ICLK
0008 735Fh	ICU	Interrupt source priority register 5F	IPR5F	8	8	2 ICLK
0008 7360h	ICU	Interrupt source priority register 60	IPR60	8	8	2 ICLK
0008 7361h	ICU	Interrupt source priority register 61	IPR61	8	8	2 ICLK
0008 7362h	ICU	Interrupt source priority register 62	IPR62	8	8	2 ICLK
0008 7363h	ICU	Interrupt source priority register 63	IPR63	8	8	2 ICLK
0008 7364h	ICU	Interrupt source priority register 64	IPR64	8	8	2 ICLK
0008 7365h	ICU	Interrupt source priority register 65	IPR65	8	8	2 ICLK
0008 7366h	ICU	Interrupt source priority register 66	IPR66	8	8	2 ICLK
0008 7367h	ICU	Interrupt source priority register 67	IPR67	8	8	2 ICLK
0008 7368h	ICU	Interrupt source priority register 68	IPR68	8	8	2 ICLK
0008 7369h	ICU	Interrupt source priority register 69	IPR69	8	8	2 ICLK
0008 736Ah	ICU	Interrupt source priority register 6A	IPR6A	8	8	2 ICLK
0008 736Bh	ICU	Interrupt source priority register 6B	IPR6B	8	8	2 ICLK
0008 7370h	ICU	Interrupt source priority register 70	IPR70	8	8	2 ICLK
0008 7371h	ICU	Interrupt source priority register 71	IPR71	8	8	2 ICLK
0008 7372h	ICU	Interrupt source priority register 72	IPR72	8	8	2 ICLK
0008 7373h	ICU	Interrupt source priority register 73	IPR73	8	8	2 ICLK
0008 7374h	ICU	Interrupt source priority register 74	IPR74	8	8	2 ICLK
0008 7375h	ICU	Interrupt source priority register 75	IPR75	8	8	2 ICLK
0008 7380h	ICU	Interrupt source priority register 80	IPR80	8	8	2 ICLK
0008 7381h	ICU	Interrupt source priority register 81	IPR81	8	8	2 ICLK
0008 7382h	ICU	Interrupt source priority register 82	IPR82	8	8	2 ICLK
0008 7383h	ICU	Interrupt source priority register 83	IPR83	8	8	2 ICLK
0008 7385h	ICU	Interrupt source priority register 85	IPR85	8	8	2 ICLK
0008 7386h	ICU	Interrupt source priority register 86	IPR86	8	8	2 ICLK
0008 7388h	ICU	Interrupt source priority register 88	IPR88	8	8	2 ICLK
0008 7389h	ICU	Interrupt source priority register 89	IPR89	8	8	2 ICLK
0008 738Ah	ICU	Interrupt source priority register 8A	IPR8A	8	8	2 ICLK
0008 738Bh	ICU	Interrupt source priority register 8B	IPR8B	8	8	2 ICLK
0008 738Ch	ICU	Interrupt source priority register 8C	IPR8C	8	8	2 ICLK
0008 738Dh	ICU	Interrupt source priority register 8D	IPR8D	8	8	2 ICLK
0008 738Eh	ICU	Interrupt source priority register 8E	IPR8E	8	8	2 ICLK
0008 738Fh	ICU	Interrupt source priority register 8F	IPR8F	8	8	2 ICLK
0008 7400h	ICU	DMACA activation source select register 0	DMRSR0	8	8	2 ICLK
0008 7404h	ICU	DMACA activation source select register 1	DMRSR1	8	8	2 ICLK
0008 7408h	ICU	DMACA activation source select register 2	DMRSR2	8	8	2 ICLK
0008 740Ch	ICU	DMACA activation source select register 3	DMRSR3	8	8	2 ICLK
0008 7500h	ICU	IRQ control register 0	IRQCR0	8	8	2 ICLK
0008 7501h	ICU	IRQ control register 1	IRQCR1	8	8	2 ICLK
0008 7502h	ICU	IRQ control register 2	IRQCR2	8	8	2 ICLK
0008 7503h	ICU	IRQ control register 3	IRQCR3	8	8	2 ICLK
0008 7504h	ICU	IRQ control register 4	IRQCR4	8	8	2 ICLK

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Item	Symbol	Value	Unit
Power supply voltage	VCC PLLVCC VCC_USB	-0.3 to +4.6	V
Input voltage (except for ports 00 to 02, 07, ports 12, 13, 16, 17, ports 20, 21, port 33)	V_{IN}	-0.3 to VCC+0.3	V
Input voltage (ports 00 to 02, 07, ports 12, 13, 16, 17, ports 20, 21, port 33*1)	V_{IN}	-0.3 to +5.8	V
Reference power supply voltage	V_{REF}	-0.3 to VCC+0.3	V
Analog power supply voltage	AVCC*2	-0.3 to +4.6	V
Analog input voltage	V_{AN}	-0.3 to VCC+0.3	V
Operating temperature	T_{opr}	-40 to +85	°C
Storage temperature	T_{stg}	-55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. Ports 00 to 02, 07, ports 12, 13, 16, 17, ports 20, 21, and port 33 are 5 V tolerant.

Note 2. Connect AVCC to VCC. When neither the A/D converter nor the D/A converter is in use, do not leave the AVCC, VREFH, AVSS, and VREFL pins open. Connect the AVCC and VREFH pins to VCC, and the AVSS and VREFL pins to VSS, respectively.

Table 5.5 Permissible Output Currents

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
T_a = -40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (average value per pin)	All output pins except for RIIC pins	I_{OL}	—	—	2.0	mA
	RIIC pins (ICFER.FMPE = 0)	I_{OL}	—	—	6.0	mA
	RIIC pins (ICFER.FMPE = 1)	I_{OL}	—	—	20.0	mA
Permissible output low current (max. value per pin)	All output pins except for RIIC pins	I_{OL}	—	—	4.0	mA
	RIIC pins (ICFER.FMPE = 0)	I_{OL}	—	—	6.0	mA
	RIIC pins (ICFER.FMPE = 1)	I_{OL}	—	—	20.0	mA
Permissible output low current (total)	Total of all output pins	ΣI_{OL}	—	—	80	mA
Permissible output high current (average value per pin)	All output pins (except for USB_DPUPE pin)	$-I_{OH}$	—	—	2.0	mA
	USB_DPUPE pin	$-I_{OH}$	—	—	3.0	mA
Permissible output high current (max. value per pin)	All output pins	$-I_{OH}$	—	—	4.0	mA
Permissible output high current (total)	Total of all output pins	$\Sigma-I_{OH}$	—	—	80	mA

Caution: To protect the LSI's reliability, the output current values should not exceed the permissible output current.

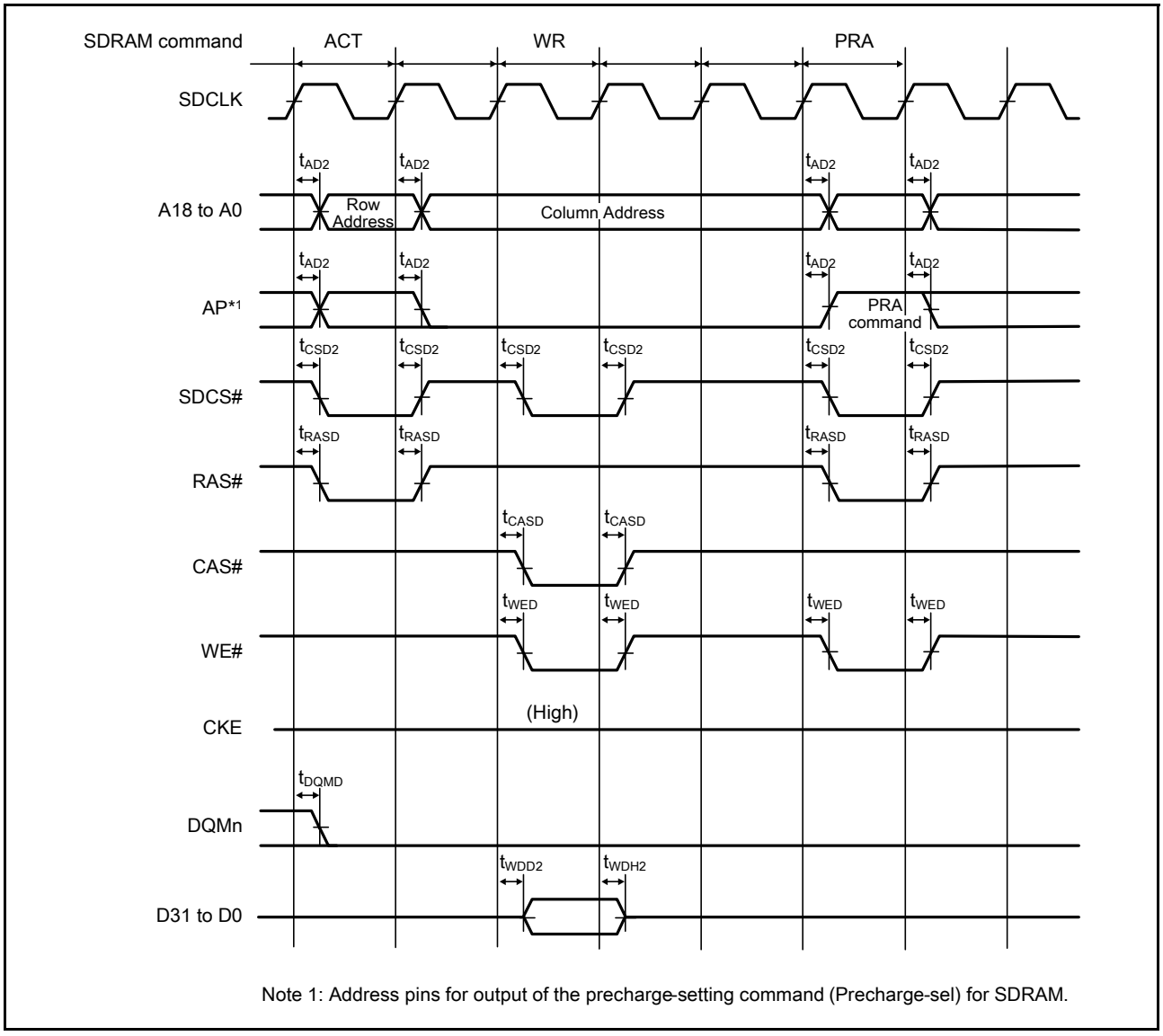
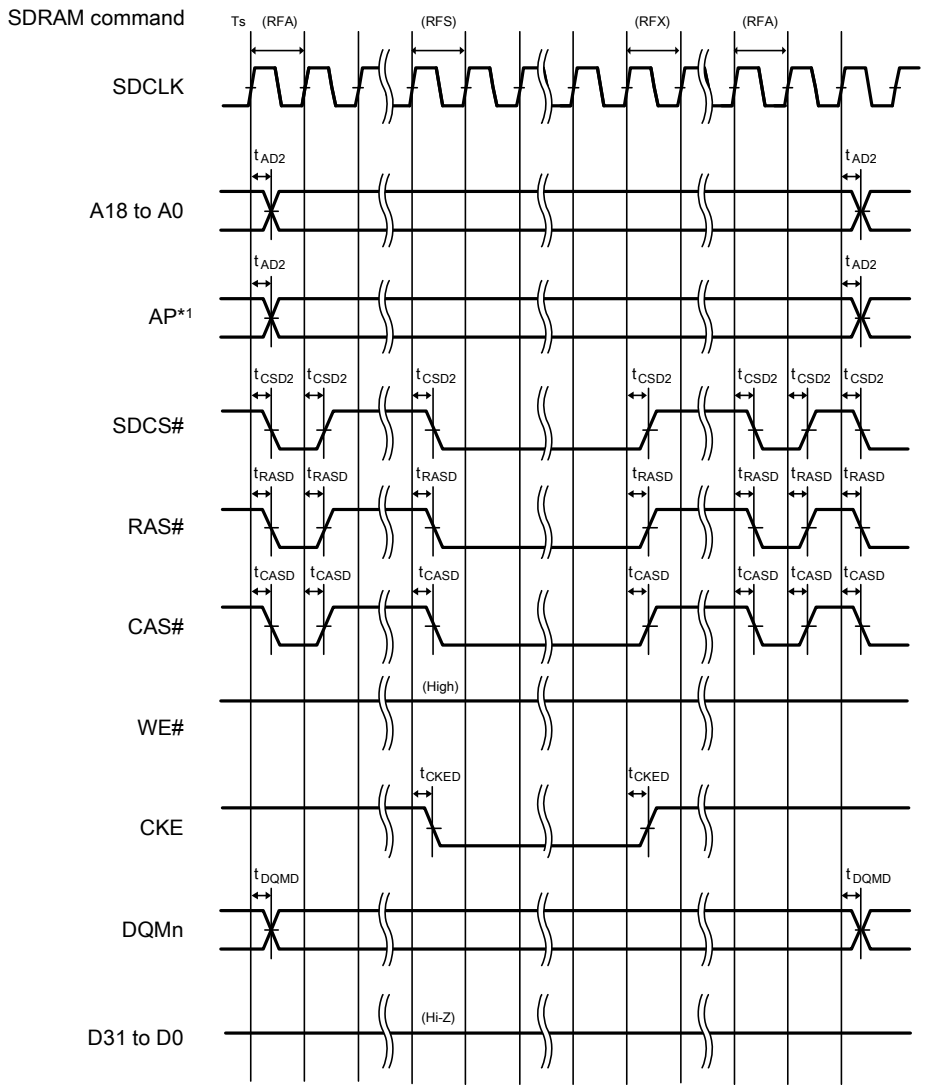


Figure 5.16 SDRAM Space Single Write Bus Timing



Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.21 SDRAM Space Self-Refresh Bus Timing

Table 5.13 Timing of On-Chip Peripheral Modules (2)

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
PCLK = 8 to 50 MHz
T_a = -40 to +85°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4 × t_{Pcyc}	—	ns	Figure 5.34 and Figure 5.35
		Clock synchronous		6 × t_{Pcyc}	—		
	Input clock pulse width		t_{SCKW}	0.4 × t_{Scyc}	0.6 × t_{Scyc}	ns	
	Input clock rise time		t_{SCKr}	—	20	ns	
	Input clock fall time		t_{SCKf}	—	20	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	16 × t_{Pcyc}	—	ns	
		Clock synchronous		4 × t_{Pcyc}	—		
	Output clock pulse width		t_{SCKW}	0.4 × t_{Scyc}	0.6 × t_{Scyc}	ns	
	Output clock rise time		t_{SCKr}	—	20	ns	
	Output clock fall time		t_{SCKf}	—	20	ns	
	Transmit data delay time (clock synchronous)		t_{TXD}	—	40	ns	
	Receive data setup time (clock synchronous)		t_{RXS}	40	—	ns	
	Receive data hold time (clock synchronous)		t_{RXH}	40	—	ns	
A/D converter	10-bit A/D converter trigger input setup time		t_{TRGS}	25	—	ns	Figure 5.36
	12-bit A/D converter trigger input setup time		t_{TRGS}	25	—	ns	

Table 5.14 Timing of On-Chip Peripheral Modules (3)

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
PCLK = 8 to 50 MHz
T_a = -40 to +85°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
CAN	Transmit data delay time		t_{CTXD}	—	40.0	ns	Figure 5.37
	Receive data setup time		t_{CRXS}	40.0	—	ns	
	Receive data hold time		t_{CRXH}	40.0	—	ns	
RSPI	RSPCK clock cycle	Master	t_{SPcyc}	2	4096	t_{Pcyc} *1	Figure 5.38
		Slave		8	4096		
	RSPCK clock high pulse width	Master	t_{SPCKWH}	$(t_{SPcyc}-t_{SPCKR}-t_{SPCKF})$ / 2-3	—	ns	
		Slave		$(t_{SPcyc}-t_{SPCKR}-t_{SPCKF})$ / 2	—		
	RSPCK clock low pulse width	Master	t_{SPCKWL}	$(t_{SPcyc}-t_{SPCKR}-t_{SPCKF})$ / 2-3	—	ns	
		Slave		$(t_{SPcyc}-t_{SPCKR}-t_{SPCKF})$ / 2	—		
	RSPCK clock rise/fall time	Output [176-pin LFBGA/ 145-pin TFLGA/ 144-pin LQFP]	t_{SPCKr}, t_{SPCKf}	—	5	ns	
		Output [100-pin LQFP/ 85-pin TFLGA]		—	10		
		Input		—	1	µs	

Note 1. tPcyc: PCLK cycle

Table 5.17 Timing of On-Chip Peripheral Modules (9)

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
ICLK = 12.5 to 100 MHz
T_a = -40 to +85°C

Item		Symbol	Min.	Max.	Unit	Test Conditions
ETHERC(MII)	ET_TX_CLK cycle time	t_{Tcyc}	40	—	ns	—
	ET_TX_EN output delay time	t_{TENd}	1	20	ns	Figure 5.51
	ET_ETXD0 to ET_ETXD3 output delay time	t_{MTDd}	1	20	ns	
	ET_CRS setup time	t_{CRSs}	10	—	ns	
	ET_CRS hold time	t_{CRSh}	10	—	ns	
	ET_COL setup time	t_{COLs}	10	—	ns	Figure 5.52
	ET_COL hold time	t_{COLh}	10	—	ns	
	ET_RX_CLK cycle time	t_{TRcyc}	40	—	ns	—
	ET_RX_DV setup time	t_{RDVs}	10		ns	Figure 5.53
	ET_RX_DV hold time	t_{RDVh}	10	—	ns	
	ET_ERXD0 to ET_ERXD3 setup time	t_{MRDs}	10	—	ns	
	ET_ERXD0 to ET_ERXD3 hold time	t_{MRDh}	10	—	ns	
	ET_RX_ER setup time	t_{RERs}	10	—	ns	Figure 5.54
	ET_RX_ER hold time	t_{RESh}	10	—	ns	
	ET_MDIO setup time	t_{MDIOs}	10	—	ns	Figure 5.55
	ET_MDIO hold time	t_{MDIOh}	10	—	ns	
	ET_MDIO utput hold time	t_{MDIOdh}	5	—	ns	Figure 5.56
	ET_WOL output delay time	t_{WOLd}	1	20	ns	Figure 5.57

Note 1. RMII_TXD_EN, RMII_TXD1, RMII_TXD0
Note 2. RMII_CRS_DV, RMII_RXD1, RMII_RXD0, RMII_RX_ER
Note 3. The user program must make settings so that this stipulation is satisfied.

5.7 Power-on Reset Circuit, Voltage Detection Circuit Characteristics

Table 5.23 Power-on Reset Circuit, Voltage Detection Circuit Characteristics

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
T_a = -40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	2.48	2.58	2.68	V	Figure 5.63
	Voltage detection circuit (LVD)	Vdet1	2.75	2.85	2.95		Figure 5.64 and Figure 5.65
		Vdet2	3.05	3.15	3.25		
Internal reset time		t_{POR}	20	35	50	ms	
Min. VCC down time*1		t_{VOFF}	200	—	—	µs	Figure 5.64 and Figure 5.65
Reply delay time		tdet	—	—	200	µs	

Note 1. The power-off time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, Vdet1, and Vdet2 for the POR/ LVD.

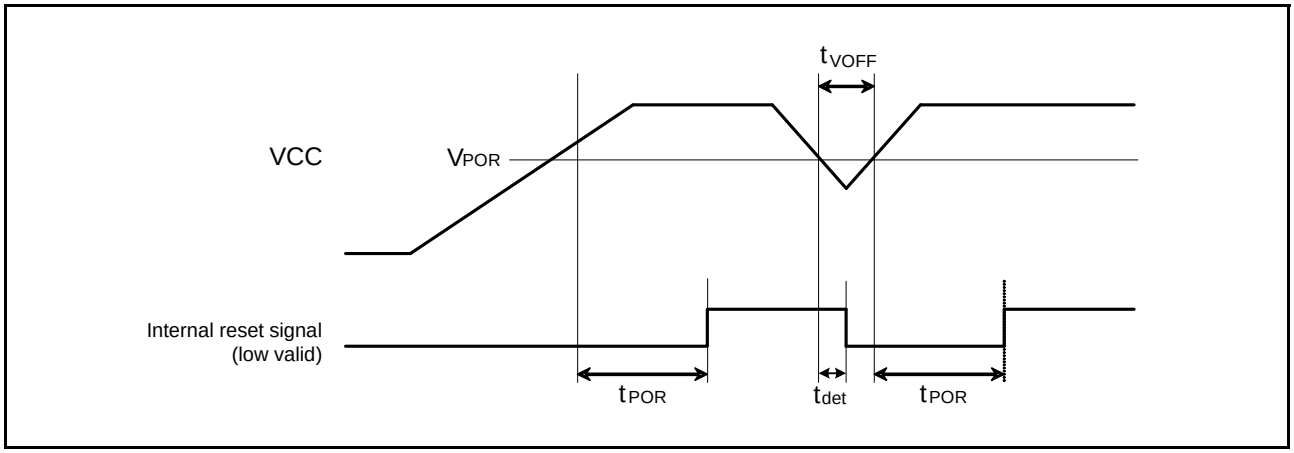


Figure 5.63 Power-on Reset Timing

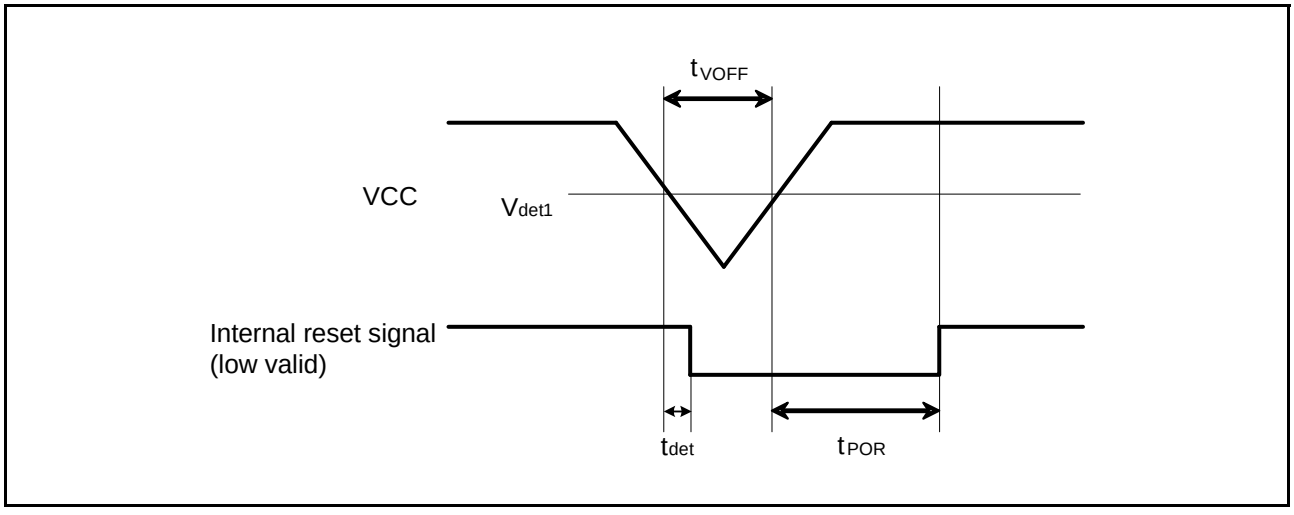


Figure 5.64 Voltage Detection Circuit Timing (Vdet1)

5.10 Data Flash (Flash Memory for Data Storage) Characteristics

Table 5.27 Data Flash (Flash Memory for Data Storage) Characteristics

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
Temperature range for the programming/erasure operation: T_a = -40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Programming time	8 bytes	t_{DP8}	—	0.4	2	ms	PCLK = 50-MHz operation
	128 bytes	t_{DP128}	—	1	5	ms	
Erasure time	2 Kbytes	t_{DE2K}	—	70	250	ms	PCLK = 50-MHz operation
Blank check time	8 bytes	t_{DBC8}	—	—	30	µs	PCLK = 50-MHz operation
	2 Kbytes	t_{DBC2K}	—	—	0.7	ms	
Rewrite/erase cycle*1		N_{DPEC}	30000*2	—	—	Times	
Suspend delay time during writing		t_{DSPD}	—	—	120	µs	Figure 5.67 PCLK = 50-MHz operation
First suspend delay time during erasing (in suspend priority mode)		t_{DSESD1}	—	—	120	µs	
Second suspend delay time during erasing (in suspend priority mode)		t_{DSESD2}	—	—	1.7	ms	
Suspend delay time during erasing (in erasure priority mode)		t_{DSEED}	—	—	1.7	ms	
Data hold time*3		t_{DDRP}	10	—	—	Year	

Note 1. Definition of rewrite/erase cycle:
The rewrite/erase cycle is the number of erasing for each block. When the rewrite/erase cycle is n times (n = 30000), erasing can be performed n times for each block. For instance, when 128-byte writing is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the rewrite/erase cycle is counted as one. However, writing to the same address for several times as one erasing is not enabled (over writing is prohibited).

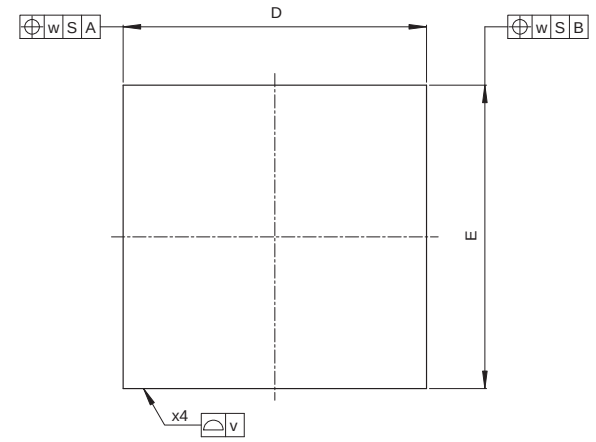
Note 2. This indicates the minimum number that guarantees the characteristics after rewriting. (The guaranteed value is in the range from one to the minimum number.)

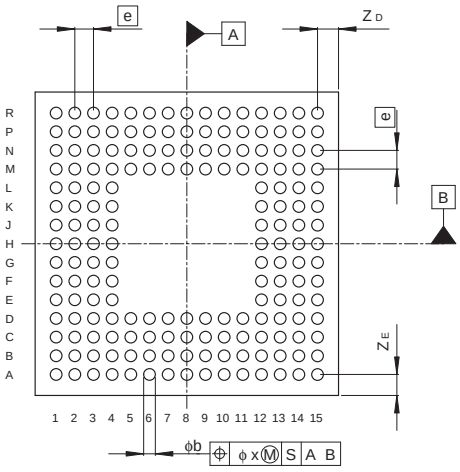
Note 3. This indicates the characteristic when rewrite is performed within the specification range including the minimum number.

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in "Packages" on Renesas Electronics Corp website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFBGA176-13x13-0.80	PLBG0176GA-A	BP-176/BP-176V	0.45g





Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	13.0	—
E	—	13.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.40
A_1	0.35	0.40	0.45
e	—	0.80	—
b	0.45	0.50	0.55
x	—	—	0.08
y	—	—	0.10
y_1	—	—	0.2
S_D	—	—	—
S_E	—	—	—
Z_D	—	0.90	—
Z_E	—	0.90	—

Figure A 176-Pin LFBGA (PLBG0176GA-A) Package Dimensions

REVISION HISTORY — RX62N Group, RX621 Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	2011.02.04	—	First Edition issued
1.10	2011.02.10	—	Features reviewed
1.20	2011.06.10		1. Overview
		2 to 5	Table 1.1 Outline of Specification, Description changed
		40 to 46	Table 1.9 Pin Functions, Description changed
			4. I/O Registers
		52 to 86	Table 4.1 List of I/O Registers (Address Order), Description changed
			5. Electrical Characteristics
		90	Table 5.2 DC Characteristics (3) , changed
		111	Figure 5.23 EDACK0 and EDACK1 Single-Address Transfer Timing (for a CS Area), changed
		111	Figure 5.24 EDACK0 and EDACK1 Single-Address Transfer Timing (for SDRAM), changed
1.30	2012.01.11		1. Overview
		2	Table 1.1 Outline of Specifications (1/4), changed, note 1, note 2 deleted
		13	Figure 1.6 Pin Assignment of the 144-Pin LQFP (Assistance Diagram), changed
		15	Figure 1.8 Pin Assignment of the 100-Pin LQFP (Assistance Diagram), changed
		33	Table 1.7 List of Pins and Pin Functions (100-Pin LQFP) (1/4), changed
		37	Table 1.8 List of Pins and Pin Functions (85-Pin TFLGA) (2/3), changed
			4. I/O Registers
		52 to 87	Table 4.1 List of I/O Registers (Address Order), Description changed
			5. Electrical Characteristics
		91	Table 5.4 DC Characteristics (3), specification added
		98	Table 5.9 Control Signal Timing, note changed
		122	Table 5.18 Timing of On-Chip Peripheral Modules (6), conditions changed