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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I ² C, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	72
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f56218bdfp-v0

Table 1.2 Functions of RX62N Group and RX621 Group Products

Functions		RX62N Group								RX621 Group				
		R5F562NxBxxx*				R5F562NxAxxx*				R5F5621xBxxx*				
Package		176-pin LFBGA	145-pin TFLGA	144-pin LQFP	100-pin LQFP	176-pin LFBGA	145-pin TFLGA	144-pin LQFP	100-pin LQFP	176-pin LFBGA	145-pin TFLGA	144-pin LQFP	100-pin LQFP	85-pin TFLGA
External bus	SDRAM area controller	O			—	O			—	O				—
DMA	DMA controller	O				O				O				
	EXDMA controller	O			—	O			—	O				—
	Data transfer controller	O				O				O				
Timers	Multi-function timer pulse unit	O				O				O				
	Port output enable	O				O				O				—
	Programmable pulse generator	O				O				O				
	8-bit timers	O				O				O				
	Compare match timer	O				O				O				
	Realtime clock	O				O				O				
	Watchdog timer	O				O				O				
	Independent watchdog timer	O				O				O				
Communication function	Ethernet controller/ DMA controller for Ethernet controller	O				O				—				
	USB 2.0 host/function module	O				O				O				
	Serial communications interfaces	O				O				O				
	I ² C bus interfaces	O				O				O				
	CAN module	O				—				O				
	Serial peripheral interfaces	O				O				O				
A/D converter		O				O				O				
D/A converter		O				O				O				
CRC calculator		O				O				O				

[Legend]

O: Supported, —: Not supported

Note: * For details on part numbers, see Table 1.3.

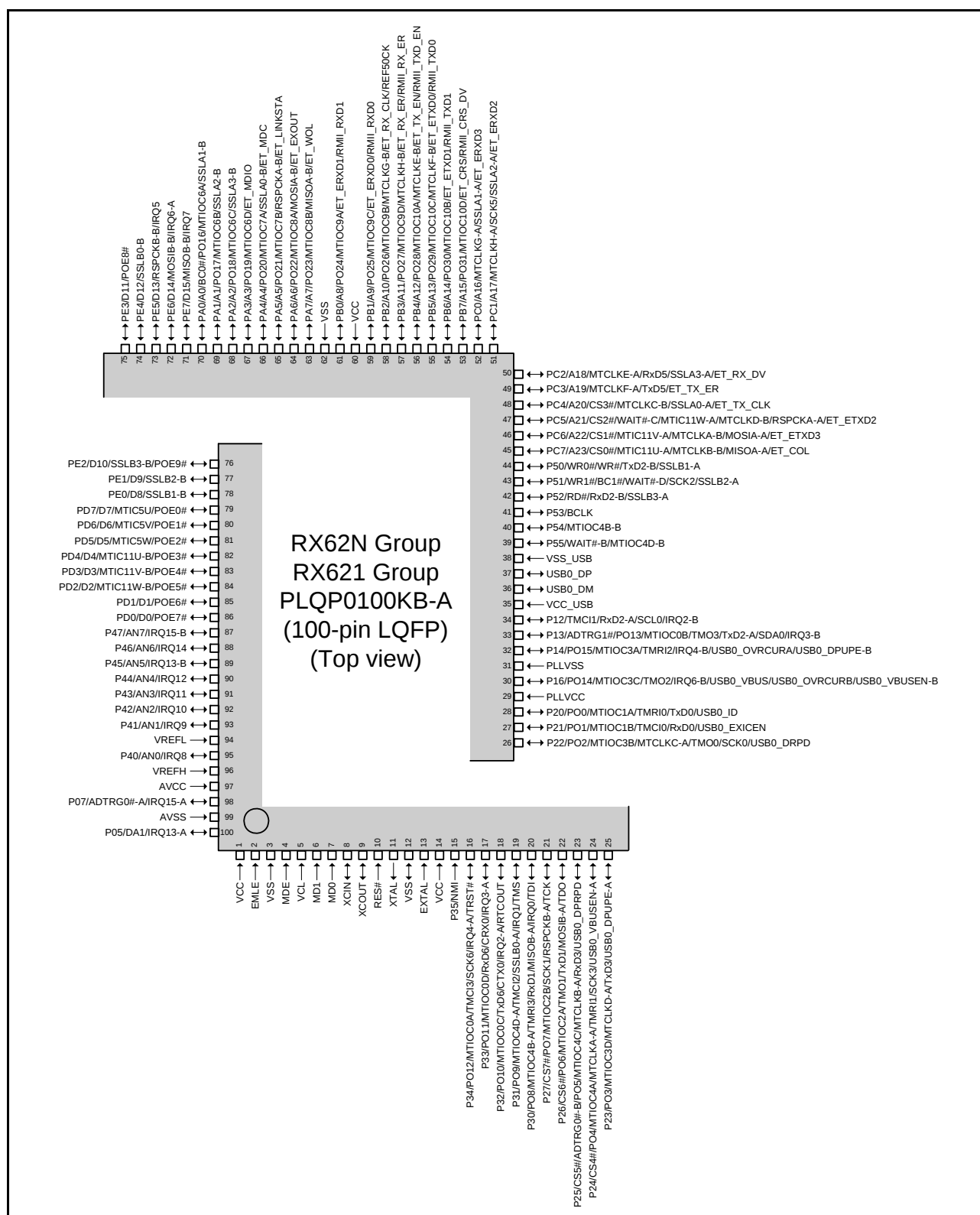


Figure 1.8 Pin Assignment of the 100-Pin LQFP (Assistance Diagram)

Table 1.4 List of Pins and Pin Functions (176-Pin LFBGA) (2 / 6)

Pin No. 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	External Bus EXDMAC	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE, WDT)	Communi- cation (SCI, CAN, RSPI, RIIC)	Others
C6	VCC							
C7		P92	D18/A18-B					
C8		P94	D20/A20-B					
C9	VCC							
C10		PD5	D5			MTIC5W-B/ POE2#		
C11	VCC							
C12		PE0	D8				SSLB1-B	
C13		PE3	D11			POE8#		
C14		PE5	D13				RSPCKB-B	IRQ5-A
C15		PE6	D14				MOSIB-B	IRQ6-A
D1	EMLE							
D2		P01				TMCIO-A	RxD6-A	IRQ9-A
D3	VCC							
D4		P41						IRQ9-B/AN1
D5		P43						IRQ11-B/AN3
D6	VSS							
D7		P93	D19/A19-B					
D8		P95	D21/A21-B					
D9	VSS							
D10		PG1	D25					
D11	VSS							
D12	VSS							
D13		PE4	D12				SSLB0-B	
D14		PE7	D15				MISOB-B	IRQ7-A
D15		P65	CS5#-A/ CKE					
E1	XCIN							
E2	CNVSS							
E3	BSCANP							
E4	VSS							
E12		PG2	D26					TRDATA0
E13	VCC							
E14		P66	CS6#-A/ DQM0					
E15		P67	CS7#-A/ DQM1					
F1	XCOUT							
F2						WDTOVF#		
F3	VCL							
F4	VSS							
F12		PG4	D28					TRSYNC
F13		PG3	D27					TRDATA1
F14		PA0	A0/BC0#/ DQM2			MTIOC6A/ PO16	SSLA1-B	

Table 1.5 List of Pins and Pin Functions (145-Pin TFLGA) (2 / 5)

Pin No.	Power Supply					Timers	Communi-	
145-Pin TFLGA	Clock System Control	I/O Port	External Bus EXDMAC	ETHERC EDMAC	USB	(MTU, TMR, PPG, POE, WDT)	cation (SCI, CAN, RSPI, RIIC)	Others
C10		P63	CS3#-A/ CAS#					
C11		PE5	D13				RSPCKB-B	IRQ5-A
C12		PE3	D11			POE8#		
C13	SDCLK	P70						
D1	EMLE							
D2	VCC							
D3		P02				TMCI1-A	SCK6-A	IRQ10-A
D4		P43						IRQ11-B/AN3
D5	VCC							
D6	VSS							
D7		P93	A19-B					
D8		PD4	D4			MTIC11U-B/ POE3#		
D9	VCC							
D10	VSS							
D11	VCC							
D12		PE7	D15				MISOB-B	IRQ7-A
D13		PE6	D14				MOSIB-B	IRQ6-A
E1	VCL							
E2	VSS							
E3		P00				TMRI0-A	TxD6-A	IRQ8-A
E4	BSCANP							
E5	(N.C)							
E10		P65	CS5#-A/ CKE					
E11		P67	CS7#-A/ DQM1					
E12		PA0	A0/BC0#			MTIOC6A/ PO16	SSLA1-B	
E13		P66	CS6#-A/ DQM0					
F1	XCIN							
F2	XCOUT							
F3						WDTOVF#		
F4	MDE							
F10		PA1	A1			MTIOC6B/ PO17	SSLA2-B	
F11		PA3	A3			MTIOC6D/ PO19		
F12	VCC							
F13		PA2	A2			MTIOC6C/ PO18	SSLA3-B	
G1	XTAL							
G2	VSS							

Table 1.9 Pin Functions (6 / 7)

Classifications	Pin Name	I/O	Description
USB 2.0 host/function module	VCC_USB	Input	Power-supply pin for the USB. Connect this pin to the system power supply even when the USB is not to be used.
	VSS_USB	Input	Ground pin for the USB. Connect this pin to the system power supply (0 V) even when the USB is not to be used.
	USB0_DP USB1_DP	I/O	Inputs or outputs D+ data for the USB bus.
	USB0_DM USB1_DM	I/O	Inputs or outputs D- data for the USB bus.
	USB0_DPRPD USB1_DPRPD	Output	Enable D+ pull-down.
	USB0_DRPD USB1_DRPD	Output	Enable D- pull-down.
	USB0_EXICEN USB1_EXICEN	Output	Connect these pins to the OTG power supply IC.
	USB0_ID USB1_ID	Input	Connect these pins to the OTG power supply IC.
	USB0_VBUSEN-A/ USB0_VBUSEN-B USB1_VBUSEN-A/ USB1_VBUSEN-B	Output	VBUS power enable pins for the USB.
	USB0_DPUPE-A/ USB0_DPUPE-B USB1_DPUPE-A/ USB1_DPUPE-B	Output	Pull-up pins for the USB.
	USB0_OVRCURA/ USB0_OVRCURB USB1_OVRCURA/ USB1_OVRCURB	Input	Over current pins for the USB.
	USB0_VBUS USB1_VBUS	Input	Input pins for detection of connection and disconnection of the USB cable.
CAN module	CRX0	Input	Input pins for the CAN.
	CTX0	Output	Output pins for the CAN.
Serial peripheral interfaces	RSPCKA-A/ RSPCKA-B	I/O	Clock input/output pins for the RSPI.
	RSPCKB-A/ RSPCKB-B	I/O	Clock input/output pins for the RSPI
	MOSIA-A/MOSIA-B MOSIB-A/MOSIB-B	I/O	Input or output data output from the master for the RSPI.
	MISOA-A/MISOA-B MISOB-A/MISOB-B	I/O	Input or output data output from the slave for the RSPI.
	SSLA0-A/SSLA0-B	I/O	Select the slave for the RSPI.
	SSLA1-A/SSLA1-B SSLA2-A/SSLA2-B SSLA3-A/SSLA3-B	Output	
	SSLB0-A/SSLB0-B	I/O	
	SSLB1-A/SSLB1-B SSLB2-A/SSLB2-B SSLB3-A/SSLB3-B	Output	
Realtime clock	RTCOUT	Output	Output pin for 1-Hz clock.
A/D converter	AN0 to AN7	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRG0#-A/ADTRG0#-B ADTRG1#	Input	Input pins for the external trigger signals that start the A/D conversion.
D/A converter	DA0, DA1	Output	Output pins for the analog signals from the D/A converter.

2. CPU

The RX CPU has sixteen general-purpose registers, nine control registers, and one accumulator used for DSP instructions.

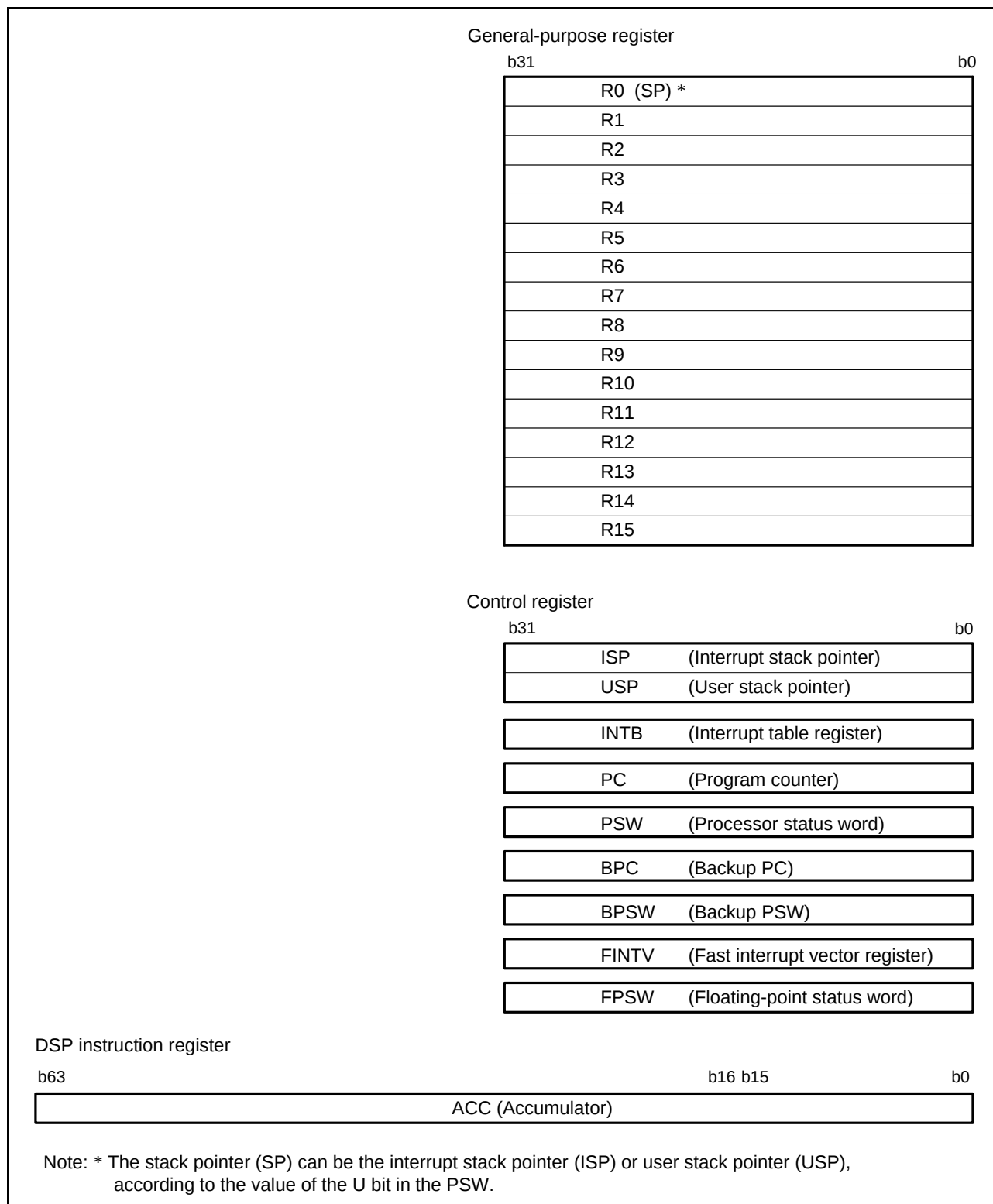


Figure 2.1 Register Set of the CPU

Table 4.1 List of I/O Registers (Address Order) (2 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 208Ch	DMAC2	DMA block transfer count register	DMCRB	16	16	2 ICLK
0008 2090h	DMAC2	DMA transfer mode register	DMTMD	16	16	2 ICLK
0008 2093h	DMAC2	DMA interrupt setting register	DMINT	8	8	2 ICLK
0008 2094h	DMAC2	DMA address mode register	DMAMD	16	16	2 ICLK
0008 209Ch	DMAC2	DMA transfer enable register	DMCNT	8	8	2 ICLK
0008 209Dh	DMAC2	DMA software start register	DMREQ	8	8	2 ICLK
0008 209Eh	DMAC2	DMA status register	DMSTS	8	8	2 ICLK
0008 209Fh	DMAC2	DMA activation source flag control register	DMCSL	8	8	2 ICLK
0008 20C0h	DMAC3	DMA source address register	DMSAR	32	32	2 ICLK
0008 20C4h	DMAC3	DMA destination address register	DMDAR	32	32	2 ICLK
0008 20C8h	DMAC3	DMA transfer count register	DMCRA	32	32	2 ICLK
0008 20CCh	DMAC3	DMA block transfer count register	DMCRB	16	16	2 ICLK
0008 20D0h	DMAC3	DMA transfer mode register	DMTMD	16	16	2 ICLK
0008 20D3h	DMAC3	DMA interrupt setting register	DMINT	8	8	2 ICLK
0008 20D4h	DMAC3	DMA address mode register	DMAMD	16	16	2 ICLK
0008 20DCh	DMAC3	DMA transfer enable register	DMCNT	8	8	2 ICLK
0008 20DDh	DMAC3	DMA software start register	DMREQ	8	8	2 ICLK
0008 20DEh	DMAC3	DMA status register	DMSTS	8	8	2 ICLK
0008 20DFh	DMAC3	DMA activation source flag control register	DMCSL	8	8	2 ICLK
0008 2200h	DMAC	DMACA start register	DMAST	8	8	2 ICLK
0008 2400h	DTC	DTC control register	DTCCR	8	8	2 ICLK
0008 2404h	DTC	DTC vector base register	DTCVBR	32	32	2 ICLK
0008 2408h	DTC	DTC address mode register	DTCADMOD	8	8	2 ICLK
0008 240Ch	DTC	DTC module start register	DTCST	8	8	2 ICLK
0008 240Eh	DTC	DTC status register	DTCSTS	16	16	2 ICLK
0008 2800h	EXDMAC0	EXDMA source address register	EDMSAR	32	32	1 to 2 BCLK*8
0008 2804h	EXDMAC0	EXDMA destination address register	EDMDAR	32	32	1 to 2 BCLK*8
0008 2808h	EXDMAC0	EXDMA transfer count register	EDMCRA	32	32	1 to 2 BCLK*8
0008 280Ch	EXDMAC0	EXDMA block transfer count register	EDMCRB	16	16	1 to 2 BCLK*8
0008 2810h	EXDMAC0	EXDMA transfer mode register	EDMTMD	16	16	1 to 2 BCLK*8
0008 2812h	EXDMAC0	EXDMA output setting register	EDMOMD	8	8	1 to 2 BCLK*8
0008 2813h	EXDMAC0	EXDMA interrupt setting register	EDMINT	8	8	1 to 2 BCLK*8
0008 2814h	EXDMAC0	EXDMA address mode register	EDMAMD	32	32	1 to 2 BCLK*8
0008 2818h	EXDMAC0	EXDMA output setting register	EDMOFR	32	32	1 to 2 BCLK*8
0008 281Ch	EXDMAC0	EXDMA transfer enable register	EDMCNT	8	8	1 to 2 BCLK*8
0008 281Dh	EXDMAC0	EXDMA software start register	EDMREQ	8	8	1 to 2 BCLK*8
0008 281Eh	EXDMAC0	EXDMA status register	EDMSTS	8	8	1 to 2 BCLK*8
0008 2820h	EXDMAC0	EXDMA external request sense mode register	EDMRMD	8	8	1 to 2 BCLK*8
0008 2821h	EXDMAC0	EXDMA external request flag register	EDMERF	8	8	1 to 2 BCLK*8
0008 2822h	EXDMAC0	EXDMA peripheral request flag register	EDMPRF	8	8	1 to 2 BCLK*8
0008 2840h	EXDMAC1	EXDMA source address register	EDMSAR	32	32	1 to 2 BCLK*8
0008 2844h	EXDMAC1	EXDMA destination address register	EDMDAR	32	32	1 to 2 BCLK*8
0008 2848h	EXDMAC1	EXDMA transfer count register	EDMCRA	32	32	1 to 2 BCLK*8

Table 4.1 List of I/O Registers (Address Order) (16 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 8209h	TMR1	Timer counter	TCNT	8	8	2 to 3 PCLK*8
0008 820Ah	TMR0	Timer counter control register	TCCR	8	8	2 to 3 PCLK*8
0008 820Bh	TMR1	Timer counter control register	TCCR	8	8	2 to 3 PCLK*8
0008 8204h	TMR01	Time constant register A	TCORA	16	16	2 to 3 PCLK*8
0008 8206h	TMR01	Time constant register B	TCORB	16	16	2 to 3 PCLK*8
0008 8208h	TMR01	Timer counter	TCNT	16	16	2 to 3 PCLK*8
0008 820Ah	TMR01	Timer counter control register	TCCR	16	16	2 to 3 PCLK*8
0008 8210h	TMR2	Timer control register	TCR	8	8	2 to 3 PCLK*8
0008 8211h	TMR3	Timer control register	TCR	8	8	2 to 3 PCLK*8
0008 8212h	TMR2	Timer control/status register	TCSR	8	8	2 to 3 PCLK*8
0008 8213h	TMR3	Timer control/status register	TCSR	8	8	2 to 3 PCLK*8
0008 8214h	TMR2	Time constant register A	TCORA	8	8	2 to 3 PCLK*8
0008 8215h	TMR3	Time constant register A	TCORA	8	8	2 to 3 PCLK*8
0008 8216h	TMR2	Time constant register B	TCORB	8	8	2 to 3 PCLK*8
0008 8217h	TMR3	Time constant register B	TCORB	8	8	2 to 3 PCLK*8
0008 8218h	TMR2	Timer counter	TCNT	8	8	2 to 3 PCLK*8
0008 8219h	TMR3	Timer counter	TCNT	8	8	2 to 3 PCLK*8
0008 821Ah	TMR2	Timer counter control register	TCCR	8	8	2 to 3 PCLK*8
0008 821Bh	TMR3	Timer counter control register	TCCR	8	8	2 to 3 PCLK*8
0008 8214h	TMR23	Time constant register A	TCORA	16	16	2 to 3 PCLK*8
0008 8216h	TMR23	Time constant register B	TCORB	16	16	2 to 3 PCLK*8
0008 8218h	TMR23	Timer counter	TCNT	16	16	2 to 3 PCLK*8
0008 821Ah	TMR23	Timer counter control register	TCCR	16	16	2 to 3 PCLK*8
0008 8240h	SCI0	Serial mode register	SMR	8	8	2 to 3 PCLK*8
0008 8241h	SCI0	Bit rate register	BRR	8	8	2 to 3 PCLK*8
0008 8242h	SCI0	Serial control register	SCR	8	8	2 to 3 PCLK*8
0008 8243h	SCI0	Transmit data register	TDR	8	8	2 to 3 PCLK*8
0008 8244h	SCI0	Serial status register	SSR	8	8	2 to 3 PCLK*8
0008 8245h	SCI0	Receive data register	RDR	8	8	2 to 3 PCLK*8
0008 8246h	SCI0	Smart card mode register	SCMR	8	8	2 to 3 PCLK*8
0008 8247h	SCI0	Serial extended mode register	SEMR	8	8	2 to 3 PCLK*8
0008 8240h	SMCI0	Serial mode register	SMR	8	8	2 to 3 PCLK*8
0008 8241h	SMCI0	Bit rate register	BRR	8	8	2 to 3 PCLK*8
0008 8242h	SMCI0	Serial control register	SCR	8	8	2 to 3 PCLK*8
0008 8243h	SMCI0	Transmit data register	TDR	8	8	2 to 3 PCLK*8
0008 8244h	SMCI0	Serial status register	SSR	8	8	2 to 3 PCLK*8
0008 8245h	SMCI0	Receive data register	RDR	8	8	2 to 3 PCLK*8
0008 8246h	SMCI0	Smart card mode register	SCMR	8	8	2 to 3 PCLK*8
0008 8248h	SCI1	Serial mode register	SMR	8	8	2 to 3 PCLK*8
0008 8249h	SCI1	Bit rate register	BRR	8	8	2 to 3 PCLK*8
0008 824Ah	SCI1	Serial control register	SCR	8	8	2 to 3 PCLK*8
0008 824Bh	SCI1	Transmit data register	TDR	8	8	2 to 3 PCLK*8
0008 824Ch	SCI1	Serial status register	SSR	8	8	2 to 3 PCLK*8
0008 824Dh	SCI1	Receive data register	RDR	8	8	2 to 3 PCLK*8
0008 824Eh	SCI1	Smart card mode register	SCMR	8	8	2 to 3 PCLK*8

Table 4.1 List of I/O Registers (Address Order) (27 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 C06Eh	PORTE	Input buffer control register	ICR*7	8	8	2 to 3 PCLK*8
0008 C06Fh	PORTF	Input buffer control register	ICR*5*6*7	8	8	2 to 3 PCLK*8
0008 C070h	PORTG	Input buffer control register	ICR*5*6*7	8	8	2 to 3 PCLK*8
0008 C080h	PORT0	Open drain control register	ODR	8	8	2 to 3 PCLK*8
0008 C081h	PORT1	Open drain control register	ODR	8	8	2 to 3 PCLK*8
0008 C082h	PORT2	Open drain control register	ODR	8	8	2 to 3 PCLK*8
0008 C083h	PORT3	Open drain control register	ODR	8	8	2 to 3 PCLK*8
0008 C08Ch	PORTC	Open drain control register	ODR	8	8	2 to 3 PCLK*8
0008 C0C9h	PORT9	Pull-up resistor control register	PCR*6*7	8	8	2 to 3 PCLK*8
0008 C0CAh	PORTA	Pull-up resistor control register	PCR	8	8	2 to 3 PCLK*8
0008 C0CBh	PORTB	Pull-up resistor control register	PCR	8	8	2 to 3 PCLK*8
0008 C0CCh	PORTC	Pull-up resistor control register	PCR	8	8	2 to 3 PCLK*8
0008 C0CDh	PORTD	Pull-up resistor control register	PCR	8	8	2 to 3 PCLK*8
0008 C0CEh	PORTE	Pull-up resistor control register	PCR*7	8	8	2 to 3 PCLK*8
0008 C0D0h	PORTG	Pull-up resistor control register	PCR*5*6*7	8	8	2 to 3 PCLK*8
0008 C100h	IOPORT	Port function register 0	PF0CSE	8	8	2 to 3 PCLK*8
0008 C101h	IOPORT	Port function register 1	PF1CSS*6*7	8	8	2 to 3 PCLK*8
0008 C102h	IOPORT	Port function register 2	PF2CSS*6*7	8	8	2 to 3 PCLK*8
0008 C103h	IOPORT	Port function register 3	PF3BUS	8	8	2 to 3 PCLK*8
0008 C104h	IOPORT	Port function register 4	PF4BUS	8	8	2 to 3 PCLK*8
0008 C105h	IOPORT	Port function register 5	PF5BUS	8	8	2 to 3 PCLK*8
0008 C106h	IOPORT	Port function register 6	PF6BUS	8	8	2 to 3 PCLK*8
0008 C107h	IOPORT	Port function register 7	PF7DMA	8	8	2 to 3 PCLK*8
0008 C108h	IOPORT	Port function register 8	PF8IRQ	8	8	2 to 3 PCLK*8
0008 C109h	IOPORT	Port function register 9	PF9IRQ	8	8	2 to 3 PCLK*8
0008 C10Ah	IOPORT	Port function register A	PFAADC	8	8	2 to 3 PCLK*8
0008 C10Bh	IOPORT	Port function register B	PFBTMR	8	8	2 to 3 PCLK*8
0008 C10Ch	IOPORT	Port function register C	PFCMTU	8	8	2 to 3 PCLK*8
0008 C10Dh	IOPORT	Port function register D	PFDMTU	8	8	2 to 3 PCLK*8
0008 C10Eh	IOPORT	Port function register E	PFENET	8	8	2 to 3 PCLK*8
0008 C10Fh	IOPORT	Port function register F	PFFSCI	8	8	2 to 3 PCLK*8
0008 C110h	IOPORT	Port function register G	PFGSPI	8	8	2 to 3 PCLK*8
0008 C111h	IOPORT	Port function register H	PFHSPI	8	8	2 to 3 PCLK*8
0008 C113h	IOPORT	Port function register J	PFJCAN	8	8	2 to 3 PCLK*8
0008 C114h	IOPORT	Port function register K	PFKUSB	8	8	2 to 3 PCLK*8
0008 C115h	IOPORT	Port function register L	PFLUSB*6*7	8	8	2 to 3 PCLK*8
0008 C116h	IOPORT	Port function register M	PFMPOE*7	8	8	2 to 3 PCLK*8
0008 C117h	IOPORT	Port function register N	PFNPOE*7	8	8	2 to 3 PCLK*8
0008 C280h	SYSTEM	Deep standby control register	DPSBYCR	8	8	4 to 5 PCLK*8
0008 C281h	SYSTEM	Deep standby wait control register	DPSWCR	8	8	4 to 5 PCLK*8
0008 C282h	SYSTEM	Deep standby interrupt enable register	DPSIER	8	8	4 to 5 PCLK*8
0008 C283h	SYSTEM	Deep standby interrupt flag register	DPSIFR	8	8	4 to 5 PCLK*8
0008 C284h	SYSTEM	Deep standby interrupt edge register	DPSIEGR	8	8	4 to 5 PCLK*8
0008 C285h	SYSTEM	Reset status register	RSTSR	8	8	4 to 5 PCLK*8
0008 C289h	FLASH	Flash write erase protection register	FWEPROR	8	8	4 to 5 PCLK*8

Table 5.4 DC Characteristics (3)

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC

VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V

T_a = -40 to +85°C

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Supply current*2	In operation	Max.*3		I _{CC} *4	—	—	100	mA	ICLK = 100 MHz PCLK = 50 MHz BCLK = 50 MHz	
		Normal operation	Peripheral function: Clocks supplied*5		—	48	—			
			Peripheral function: Clocks not supplied*5		—	35	—			
		Increased by BGO operation*6			—	15	—			
	Sleep				—	20	60			
	All-module-clock-stop mode*7				—	14	28			
	Standby mode	Software standby mode			—	0.12	3.0	mA		
		Deep software standby mode	RTC in operation		RAM, USB retained	—	30	206	μA	
					RAM, USB power supply halted	—	26	66	μA	
			RTC halted		RAM, USB retained	—	25	200	μA	
					RAM, USB power supply halted	—	21	60	μA	
		Analog power supply current	During 12-bit A/D conversion (per unit)			AI _{CC}	—	2.5	3.0	mA
During 10-bit A/D conversion (per unit)			—	0.8	1.2		mA			
During D/A conversion (per channel)			—	0.3	2.0		μA			
Idle (all units)			—	30	35		μA			
During A/D or D/A standby (all units)			—	0.1	4.0		μA			
Reference power supply current	During 12-bit A/D conversion (per unit)			AI _{CC}	—	0.5	0.7	mA		
	During 10-bit A/D conversion (per unit)				—	0.06	0.1	mA		
	During D/A conversion (per channel)				—	0.6	1.0	mA		
	Idle (all units)				—	0.4	0.6	mA		
	During A/D or D/A standby (all units)				—	0.1	2.0	μA		
RAM standby voltage				V _{RAM}	2.48	—	—	V		
VCC rising gradient				SVCC	—	—	20	ms/V		

Note 1. The V_{IH} characteristic of the pins multiplexed with 5-V tolerant ports 00 to 02, 07, 12, 13, 16, 17, 20, 21, and 33 is the same as the V_{IH} characteristic of 5-V tolerant ports.

Note 2. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.

Note 3. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.

Note 4. ICC depends on f (ICLK) as follows. (ICLK: PCLK: BCLK: BCLK pin = 8 : 4: 8: 4)

ICC max. = 0.89 × f + 11 (max.)

ICC typ. = 0.43 × f + 5 (normal operation, peripheral function: clocks supplied)

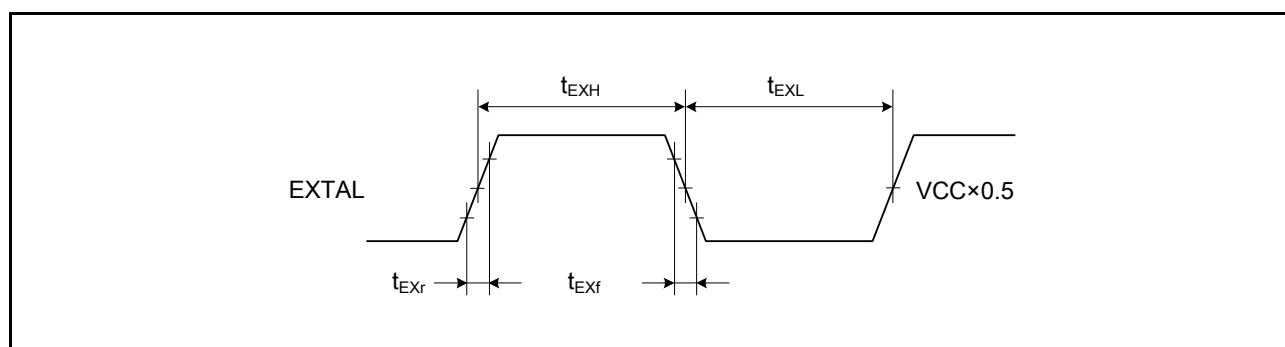
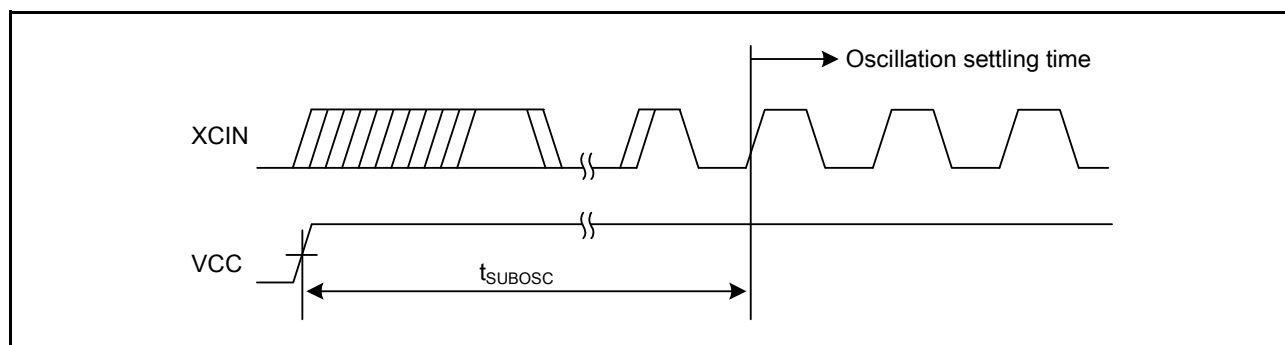
ICC typ. = 0.30 × f + 5 (normal operation, peripheral function: clocks not supplied)

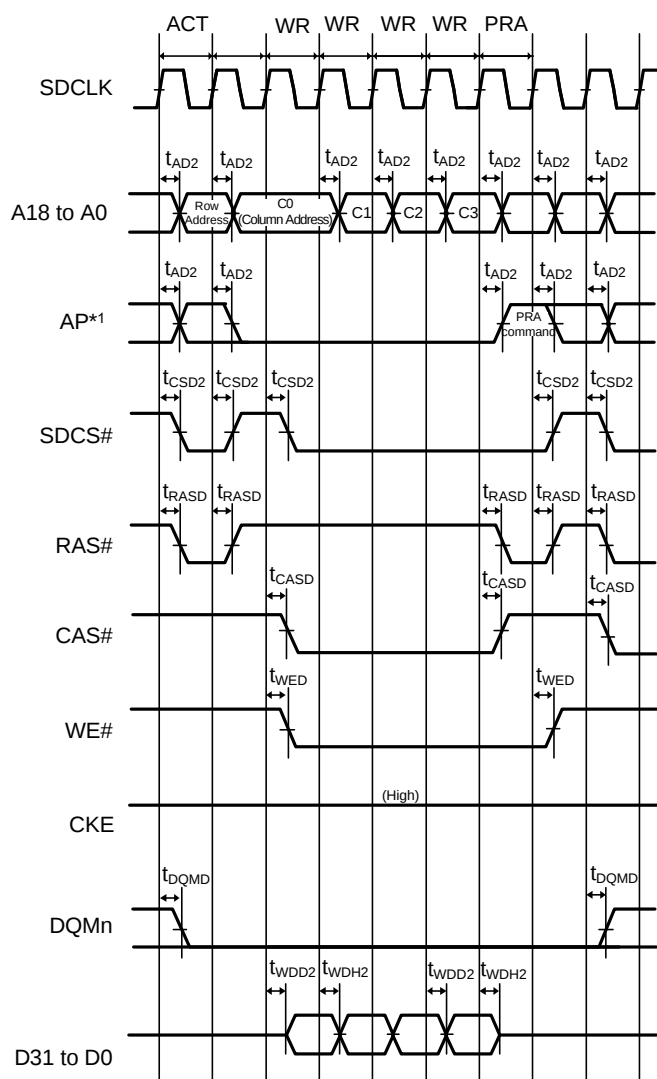
ICC max. = 0.48 × f + 12 (sleep mode)

Note 5. This does not include the BGO operation.

Note 6. Incremented if data is written to or erased from the ROM or data flash for data storage during the program execution.

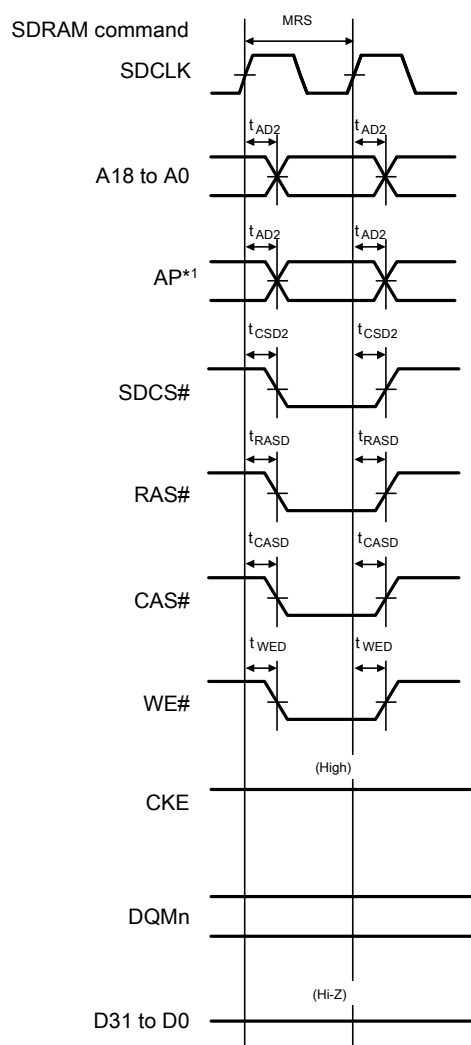
Note 7. The values are for reference.

**Figure 5.5 EXTAL External Input Clock Timing****Figure 5.6 XCIN Sub-Clock Oscillation Settling Time**



Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.18 SDRAM Space Multiple Write Bus Timing



Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.20 SDRAM Space Mode Register Set Bus Timing

Table 5.13 Timing of On-Chip Peripheral Modules (2)

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC

VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V

PCLK = 8 to 50 MHz

T_a = -40 to +85°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
SCI	Input clock cycle	Asynchronous	t_{Scyc}	$4 \times t_{\text{pCyc}}$	—	ns	Figure 5.34 and Figure 5.35
		Clock synchronous		$6 \times t_{\text{pCyc}}$	—		
	Input clock pulse width		t_{SCKW}	$0.4 \times t_{\text{Scyc}}$	$0.6 \times t_{\text{Scyc}}$	ns	
	Input clock rise time		t_{SCKr}	—	20	ns	
	Input clock fall time		t_{SCKf}	—	20	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	$16 \times t_{\text{pCyc}}$	—	ns	
		Clock synchronous		$4 \times t_{\text{pCyc}}$	—		
	Output clock pulse width		t_{SCKW}	$0.4 \times t_{\text{Scyc}}$	$0.6 \times t_{\text{Scyc}}$	ns	
	Output clock rise time		t_{SCKr}	—	20	ns	
	Output clock fall time		t_{SCKf}	—	20	ns	
	Transmit data delay time (clock synchronous)		t_{TXD}	—	40	ns	
	Receive data setup time (clock synchronous)		t_{RXS}	40	—	ns	
	Receive data hold time (clock synchronous)		t_{RXH}	40	—	ns	
A/D converter	10-bit A/D converter trigger input setup time		t_{TRGS}	25	—	ns	Figure 5.36
	12-bit A/D converter trigger input setup time		t_{TRGS}	25	—	ns	

Table 5.17 Timing of On-Chip Peripheral Modules (9)

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC

VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V

ICLK = 12.5 to 100 MHz

T_a = -40 to +85°C

Item		Symbol	Min.	Max.	Unit	Test Conditions
ETHERC(MII)	ET_TX_CLK cycle time	t _{Tcyc}	40	—	ns	—
	ET_TX_EN output delay time	t _{TENd}	1	20	ns	Figure 5.51
	ET_ETXD0 to ET_ETXD3 output delay time	t _{MTDd}	1	20	ns	
	ET_CRs setup time	t _{CRSs}	10	—	ns	
	ET_CRs hold time	t _{CRSh}	10	—	ns	
	ET_COL setup time	t _{COLs}	10	—	ns	
	ET_COL hold time	t _{COLh}	10	—	ns	
	ET_RX_CLK cycle time	t _{TRcyc}	40	—	ns	—
	ET_RX_DV setup time	t _{RDVs}	10		ns	Figure 5.53
	ET_RX_DV hold time	t _{RDVh}	10	—	ns	
	ET_ERXD0 to ET_ERXD3 setup time	t _{MRDs}	10	—	ns	
	ET_ERXD0 to ET_ERXD3 hold time	t _{MRDh}	10	—	ns	
	ET_RX_ER setup time	t _{RERs}	10	—	ns	Figure 5.54
	ET_RX_ER hold time	t _{RESh}	10	—	ns	
	ET_MDIO setup time	t _{MDIOs}	10	—	ns	Figure 5.55
	ET_MDIO hold time	t _{MDIOh}	10	—	ns	
	ET_MDIO utput hold time	t _{MDIOdh}	5	—	ns	Figure 5.56
	ET_WOL output delay time	t _{WOLd}	1	20	ns	Figure 5.57

Note 1. RMII_TXD_EN, RMII_TXD1, RMII_TXD0

Note 2. RMII_CRs_DV, RMII_RXD1, RMII_RXD0, RMII_RX_ER

Note 3. The user program must make settings so that this stipulation is satisfied.

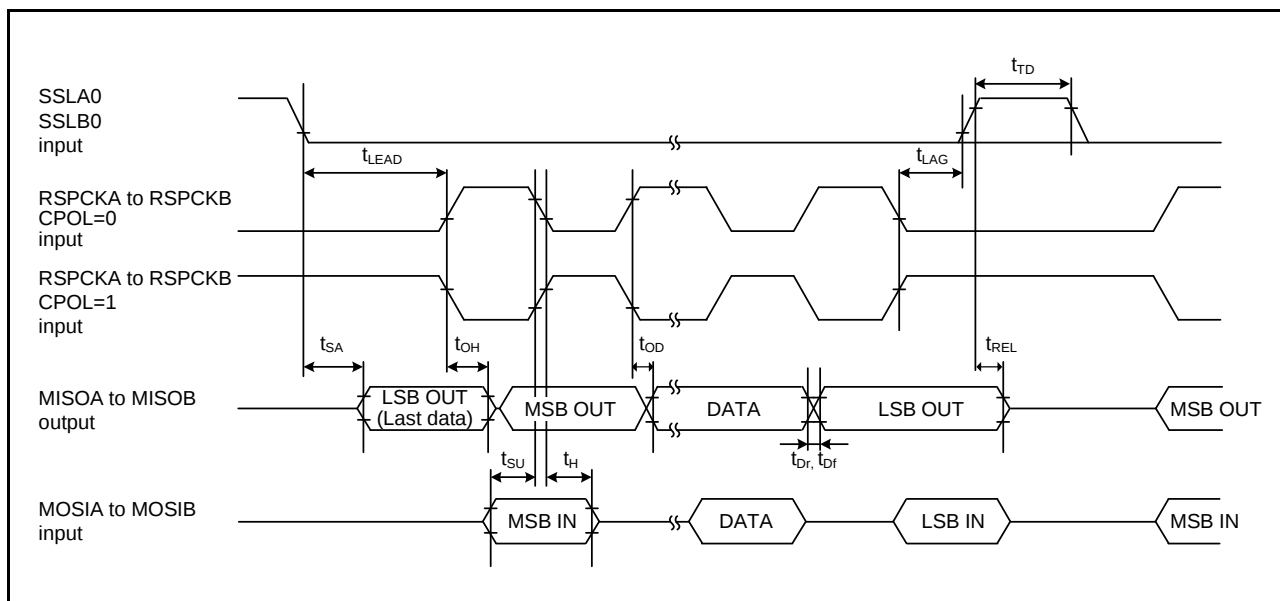


Figure 5.42 RSPI Timing (Slave, CPHA = 1)

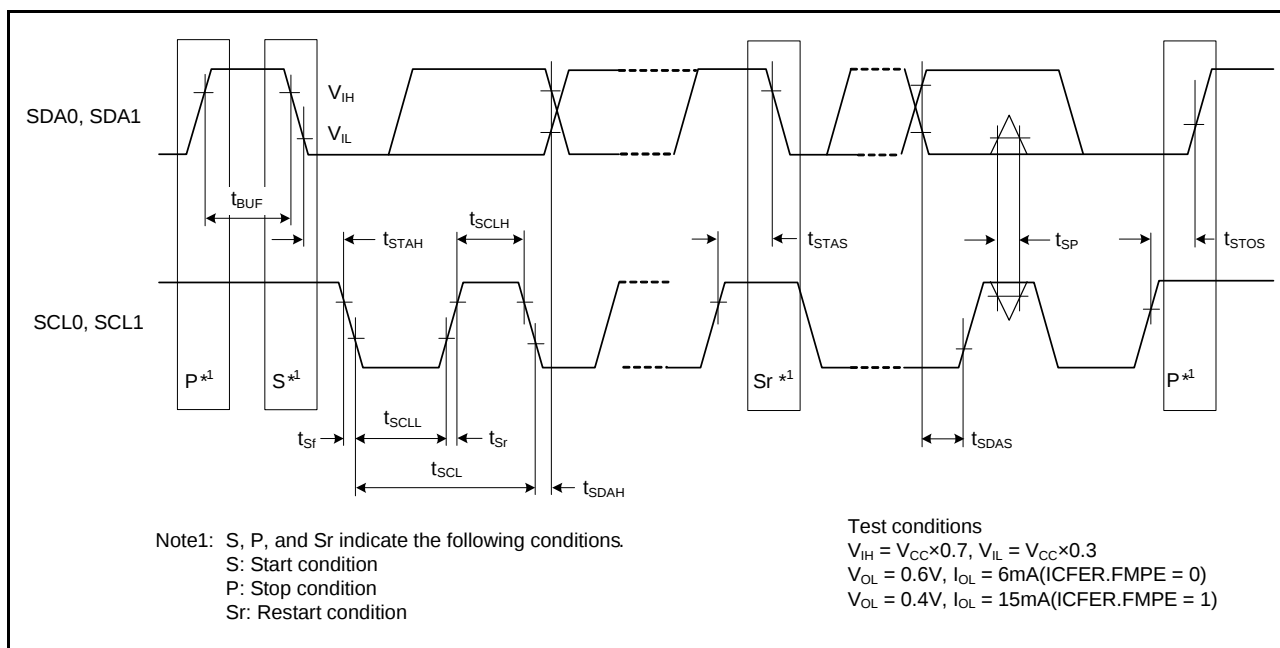


Figure 5.43 I2C Bus Interface Input/Output Timing

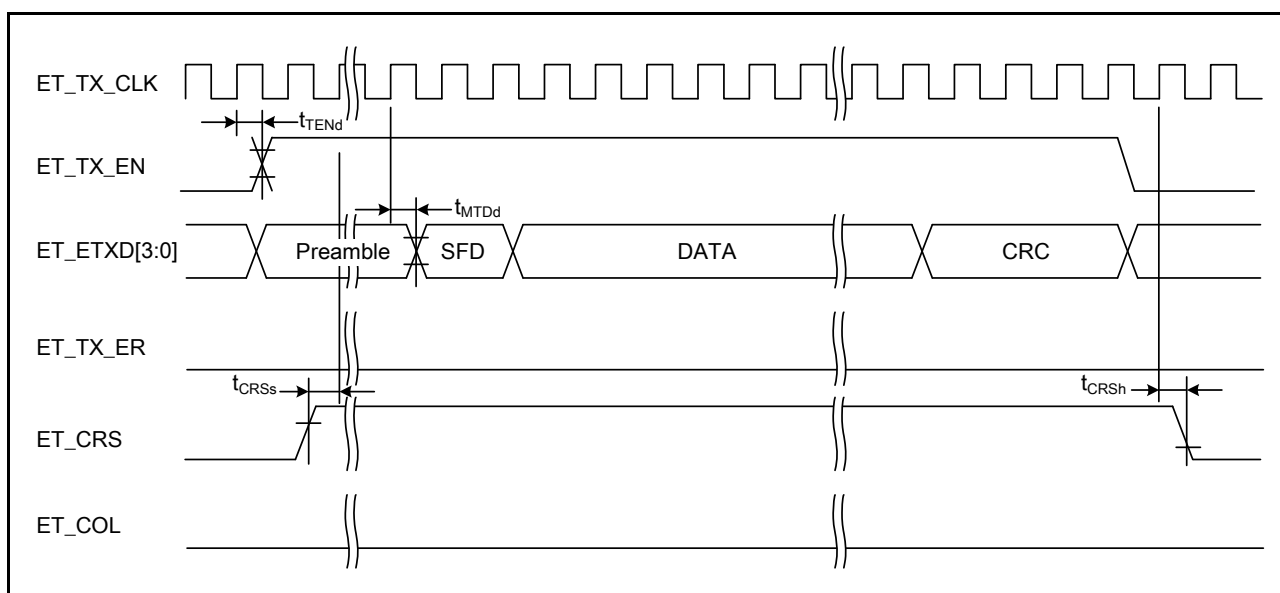


Figure 5.51 MII Transmission Timing (Normal Operation)

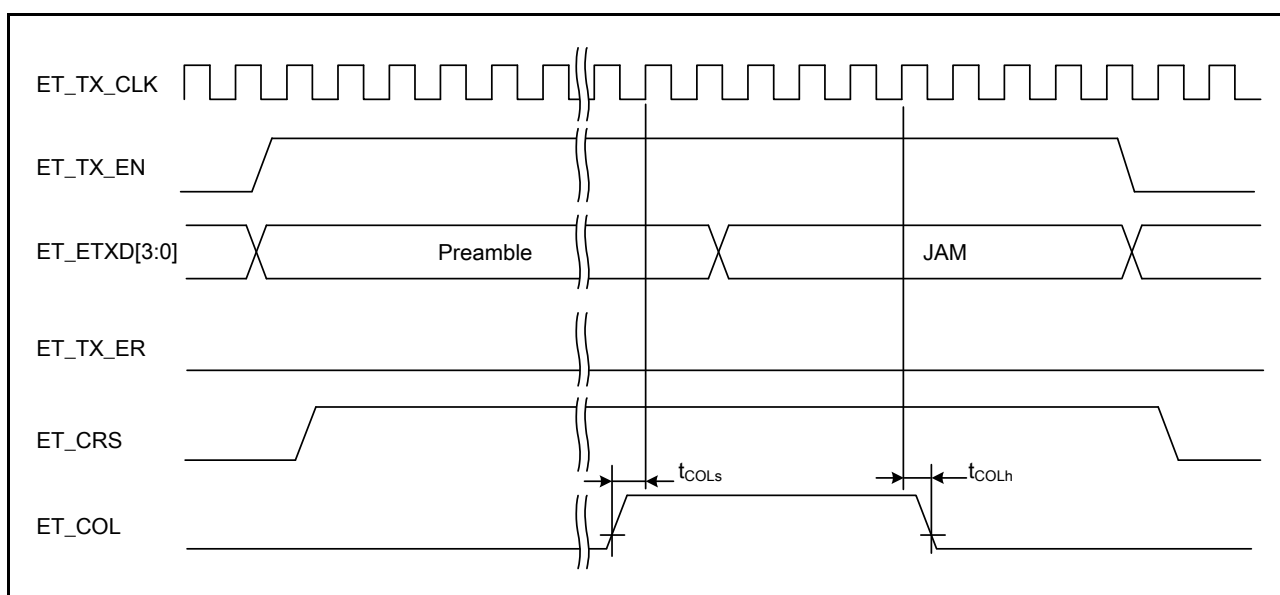


Figure 5.52 MII Transmission Timing (Conflict Occurrence)

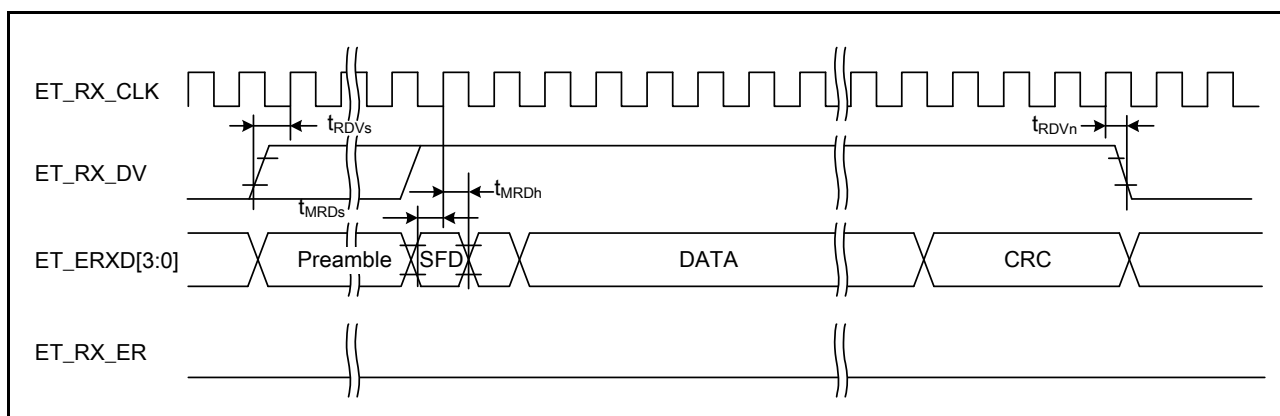


Figure 5.53 MII Reception Timing (Normal Operation)

5.6 D/A Conversion Characteristics

Table 5.22 D/A Conversion Characteristics

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC

VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V

T_a = -40 to +85°C

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	10	10	10	bits	
Conversion time	—	—	3.0	μs	20-pF capacitive load
Absolute accuracy	—	±2.0	±4.0	LSB	2-MΩ resistive load
	—	—	±3.0	LSB	4-MΩ resistive load
	—	—	±2.0	LSB	10-MΩ resistive load
RO output resistance	—	3.6	—	kΩ	

5.9 ROM (Flash Memory for Code Storage) Characteristics

Table 5.25 ROM (Flash Memory for Code Storage) Characteristics (1)

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC

VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V

Temperature range for the programming/erasure operation: T_a = -40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Rewrite/erase cycle*1	N _{PEC}	1000	—	—	Times	
Data hold time	t _{DRP}	30*2	—	—	Year	T _a = +85°C

Note 1. Definition of reprogram/erase cycle:

The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 256-byte programming is performed 16 times for different addresses in 4-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. The result obtained from the reliability test.

Table 5.26 ROM (Flash Memory for Code Storage) Characteristics (2)

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC

VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V

Temperature range for the programming/erasure operation: T_a = -40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Programming time	256 bytes	t _{P256}	—	2	12	ms	PCLK = 50 MHz N _{PEC} ≤ 100
	4 Kbytes	t _{P4K}	—	23	50	ms	
	16 Kbytes	t _{P16K}	—	90	200	ms	
	256 byte	t _{P256}	—	2.4	14.4	ms	PCLK = 50 MHz N _{PEC} > 100
	4 Kbytes	t _{P4K}	—	27.6	60	ms	
	16 Kbytes	t _{P16K}	—	108	240	ms	
Erasure time	4 Kbytes	t _{E4K}	—	25	60	ms	PCLK = 50 MHz N _{PEC} ≤ 100
	16 Kbytes	t _{E16K}	—	100	240	ms	
	4 Kbytes	t _{E4K}	—	30	72	ms	PCLK = 50 MHz N _{PEC} > 100
	16 Kbytes	t _{E16K}	—	120	288	ms	
Suspend delay time during writing		t _{SPD}	—	—	120	μs	Figure 5.67 PCLK = 50-MHz operation
First suspend delay time during erasing (in suspend priority mode)		t _{SESD1}	—	—	120	μs	
Second suspend delay time during erasing (in suspend priority mode)		t _{SESD2}	—	—	1.7	ms	
Suspend delay time during erasing (in erasure priority mode)		t _{SEED}	—	—	1.7	ms	

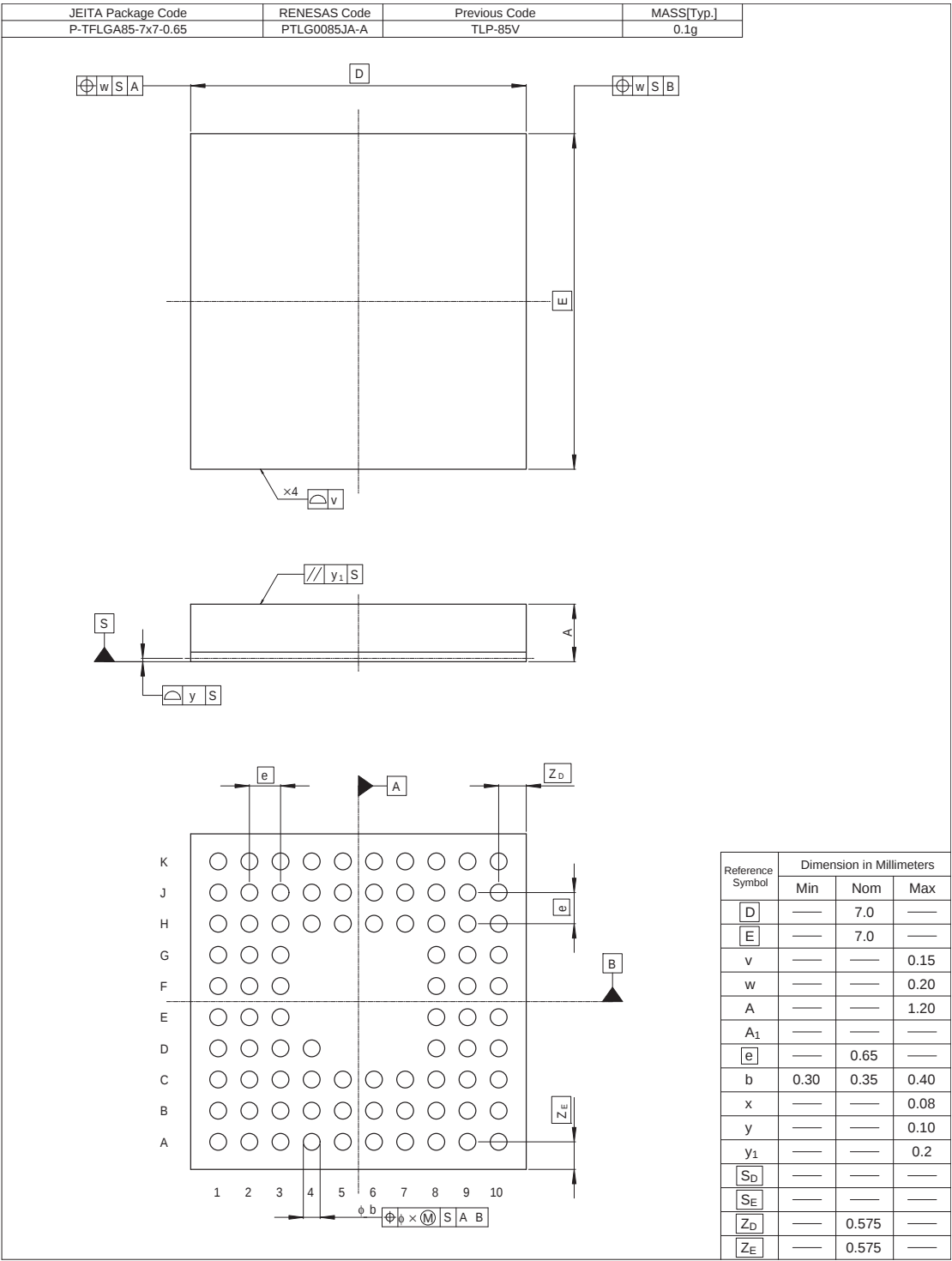


Figure E 85-Pin TFLGA (PTLG0085JA-A) Package Dimensions