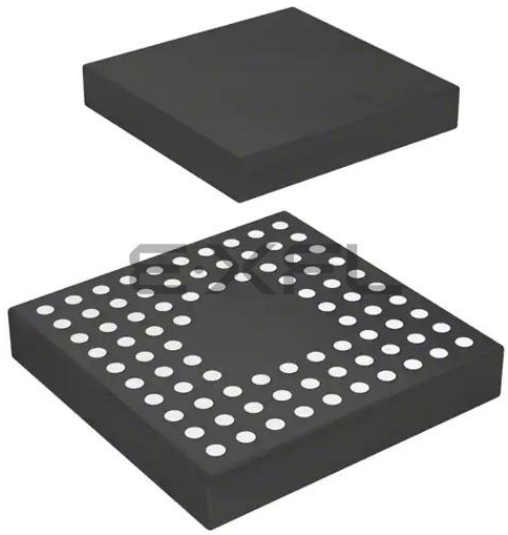
Renesas Electronics America Inc - R5F56218BDLD#U0 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	58
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	85-TFLGA
Supplier Device Package	85-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f56218bdld-u0

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 lists the functions of products.

Table 1.1 Outline of Specifications (1 / 4)

Classification	Module/Function	Description
CPU	CPU	・ Maximum operating frequency: 100 MHz ・ 32-bit RX CPU ・ Minimum instruction execution time: One instruction per state (cycle of the system clock) ・ Address space: 4-Gbyte linear ・ Register set of the CPU General purpose: Sixteen 32-bit registers Control: Nine 32-bit registers Accumulator: One 64-bit register ・ Basic instructions: 73 ・ Floating-point instructions: 8 ・ DSP instructions: 9 ・ Addressing modes: 10 ・ Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian ・ On-chip 32-bit multiplier: 32 x 32 → 64 bits ・ On-chip divider: 32 / 32 → 32 bits ・ Barrel shifter: 32 bits ・ Memory-protection unit (MPU)
	FPU	・ Single precision (32-bit) floating point ・ Data types and floating-point exceptions in conformance with the IEEE754 standard
Memory	ROM	・ ROM capacity: 512 Kbytes (max.) ・ Two on-board programming modes Boot mode (The user MAT is programmable via the SCI and USB.) User program mode ・ Parallel programmer mode (for off-board programming)
	RAM	RAM capacity: 96 Kbytes (max.)
	Data flash	Data flash capacity: 32 Kbytes
MCU operating modes		・ Single-chip mode, on-chip ROM enabled expansion mode, and on-chip ROM disabled expansion mode (software switching)
Clock	Clock generation circuit	・ Two circuits: Main clock oscillator and subclock oscillator ・ Internal oscillator: Low-speed on-chip oscillator ・ Structure of a PLL frequency synthesizer and frequency divider for selectable operating frequency ・ Oscillation stoppage detection ・ Independent frequency-division and multiplication settings for the system clock (ICLK), peripheral module clock (PCLK), and external bus clock (BCLK) The CPU and other bus masters run in synchronization with the system clock (ICLK): 8 to 100 MHz Peripheral modules run in synchronization with the peripheral module clock (PCLK): 8 to 50 MHz ・ Devices connected to the external bus run in synchronization with the external bus clock (BCLK pin): 8 to 50 MHz*1
Reset		・ Pin reset, power-on reset, voltage-monitoring reset, watchdog timer reset, independent watchdog timer reset, and deep software standby reset
Voltage detection circuit		・ When the voltage on VCC falls below the voltage detection level (Vdet), an internal reset or internal interrupt is generated.
Low power consumption	Low power consumption facilities	・ Module stop function ・ Four low power consumption modes Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode

Table 1.1 Outline of Specifications (2 / 4)

Classification	Module/Function	Description
Interrupt	Interrupt control unit	・Peripheral function interrupts: 146 sources ・External interrupts: 16 (pins IRQ0 to IRQ15) ・Non-maskable interrupts: 3 (the NMI pin, oscillation stop detection interrupt, and voltage-monitoring interrupt) ・Sixteen levels specifiable for the order of priority
	User break controller (as an optional function)	・Two breakpoint channels ・Address breaks in fetch cycles are specifiable (enabling ROM correction)
External bus extension		・The external address space can be divided into nine areas (CS0 to CS7, SDCS), each with independent control of access settings. Capacity of each area: 16 Mbytes (CS0 to CS7), 128 Mbytes (SDCS) A chip-select signal (CS0# to CS7#, SDCS#) can be output for each area. Each area is specifiable as an 8-, 16-, or 32-bit bus space (however, only 176-pin versions support 32-bit bus spaces). The data arrangement in each area is selectable as little or big endian (only for data). ・SDRAM interface connectable ・Bus format: Separate buses ・Wait control ・Write buffer facility
DMA	DMA controller	・4 channels ・Three transfer modes: Normal transfer, repeat transfer, and block transfer ・Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
	EXDMA controller	・2 channels ・Four transfer modes: Normal transfer, repeat transfer, block transfer, and cluster transfer ・Single-address transfer enabled with the EDACK signal ・Capable of direct data transfer to TFT LCD panels ・Activation sources: Software trigger, external DMA transfer requests (EDREQ), and interrupt requests from peripheral functions
	Data transfer controller	・Three transfer modes: Normal transfer, repeat transfer, and block transfer ・Activation sources: Software trigger, external interrupts and interrupt requests from peripheral functions
I/O ports	Programmable I/O ports	・I/O ports for the 176-pin LFBGA/145-pin TFLGA/144-pin LQFP/100-pin LQFP/85-pin TFLGA ・I/O pins: 126/103/103/72/58 ・Input pins: 2/2/2/2/2 ・Pull-up resistors: 56/44/44/40/28 ・Open-drain outputs: 35/33/33/27/23 ・5-V tolerance: 11/11/11/7/6
Timers	Multi-function timer pulse unit	・(16 bits x 6 channels) x 2 units ・Time bases for the 12 16-bit timer channels can be provided via up to 32 pulse-input/output lines and six pulse-input lines ・Select from among eight counter-input clock signals for each channel (PCLK/1, PCLK/4, PCLK/16, PCLK/64, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available. ・Input capture function ・21 output compare/input capture registers ・Pulse output mode ・Complementary PWM output mode ・Reset synchronous PWM mode ・Phase-counting mode ・Generation of triggers for A/D converter conversion
	Port output enable	・Controls the high-impedance state of the MTU's waveform output pins

Table 1.4 List of Pins and Pin Functions (176-Pin LFBGA) (3 / 6)

Pin No. 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	External Bus EXDMAC	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE, WDT)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
F15		PG5	D29					TRCLK
G1	VSS							
G2	MD1							
G3	MD0							
G4	MDE							
G12	VSS							
G13	VCC							
G14		PG6	D30					TRDATA2
G15		PA1	A1/DQM3			MTIOC6B/ PO17	SSLA2-B	
H1	XTAL							
H2		P35						NMI
H3	VCC							
H4	RES#							
H12		PG7	D31					TRDATA3
H13		PA2	A2			MTIOC6C/ PO18	SSLA3-B	
H14		PA4	A4			MTIOC7A/ PO20	SSLA0-B	
H15		PA3	A3			MTIOC6D/ PO19		
J1	EXTAL							
J2		P32				MTIOC0C/ PO10/ RTCOUT	CTX0/ TxD6-B	IRQ2-A
J3		PF3						TMS
J4		P34				MTIOC0A/ TMCI3-B/ PO12	SCK6-B	IRQ4-A
J12	VSS							
J13		PA5	A5			MTIOC7B/ PO21	RSPCKA-B	
J14		PA7	A7			MTIOC8B/ PO23	MISOA-B	
J15		PA6	A6			MTIOC8A/ PO22	MOSIA-B	
K1		P33				MTIOC0D/ PO11	CRX0/ RxD6-B	IRQ3-A
K2		P31			USB1_DPRPD	MTIOC4D-A/ TMCI2-B/ PO9	SSLB0-A	IRQ1-A
K3		PF0					TxD1-B	TDO
K4		PF4						TRST#
K12		PB1	A9			MTIOC9C/ PO25		
K13		P71	CS1#-B	ET_MDIO				
K14		P72	CS2#-B	ET_MDC				

Table 1.5 List of Pins and Pin Functions (145-Pin TFLGA) (2 / 5)

Pin No. 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	External Bus EXDMAC	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE, WDT)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
C10		P63	CS3#-A/ CAS#					
C11		PE5	D13				RSPCKB-B	IRQ5-A
C12		PE3	D11			POE8#		
C13	SDCLK	P70						
D1	EMLE							
D2	VCC							
D3		P02				TMCI1-A	SCK6-A	IRQ10-A
D4		P43						IRQ11-B/AN3
D5	VCC							
D6	VSS							
D7		P93	A19-B					
D8		PD4	D4			MTIC11U-B/ POE3#		
D9	VCC							
D10	VSS							
D11	VCC							
D12		PE7	D15				MISOB-B	IRQ7-A
D13		PE6	D14				MOSIB-B	IRQ6-A
E1	VCL							
E2	VSS							
E3		P00				TMRI0-A	TxD6-A	IRQ8-A
E4	BSCANP							
E5	(N.C)							
E10		P65	CS5#-A/ CKE					
E11		P67	CS7#-A/ DQM1					
E12		PA0	A0/BC0#			MTIOC6A/ PO16	SSLA1-B	
E13		P66	CS6#-A/ DQM0					
F1	XCIN							
F2	XCOUT							
F3						WDTOVF#		
F4	MDE							
F10		PA1	A1			MTIOC6B/ PO17	SSLA2-B	
F11		PA3	A3			MTIOC6D/ PO19		
F12	VCC							
F13		PA2	A2			MTIOC6C/ PO18	SSLA3-B	
G1	XTAL							
G2	VSS							

Table 1.5 List of Pins and Pin Functions (145-Pin TFLGA) (5 / 5)

Pin No. 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	External Bus EXDMAC	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE, WDT)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
M4		P15				MTIOC0B/ TMCI2-A/ PO13	SCK3-A	IRQ5-B
M5		P14			USB0_OVRCURA/ USB0_DPUPE-B	TMRI2		IRQ4-B
M6	VSS_USB							
M7		P55	WAIT#-B/ EDREQ0-C	ET_EXOUT		MTIOC4D-B		TRDATA3
M8		P50	WR0#/ WR#				SSLB1-A/ TxD2-B	
M9		PC6	A22/CS1#-C	ET_ETXD3		MTIC11V-A/ MTCLKA-B	MOSIA-A	
M10		P80	EDREQ0-A	ET_TX_EN/ RMII_TXD_EN		MTIOC3B-B		TRDATA0
M11		PC2	A18-A	ET_RX_DV		MTCLKE-A	SSLA3-A/ RxD5	
M12		PC1	A17-A	ET_ERXD2		MTCLKH-A	SSLA2-A/ SCK5	
M13	VSS							
N1		P21			USB0_EXICEN	MTIOC1B/ TMCI0-B/ PO1	SCL1/RxD0	
N2		P16			USB0_VBUS/ USB0_OVRCURB/ USB0_VBUSEN-B	MTIOC3C-A/ TMO2/ PO14	RxD3-A	IRQ6-B
N3	PLLVSS							
N4		P13				TMO3	SDA0/ TxD2-A	IRQ3-B/ ADTRG1#
N5					USB0_DM			
N6					USB0_DP			
N7		P54	EDACK0-C	ET_LINKSTA		MTIOC4B-B		TRDATA2
N8		P51	WR1#/BC1#/ WAIT#-D				SSLB2-A/ SCK2	
N9	VCC							
N10		PC5	A21/CS2#-C/ WAIT#-C	ET_ETXD2		MTIC11W-A/ MTCLKD-B	RSPCKA-A	
N11		PC4	A20/CS3#-C	ET_TX_CLK		MTCLKC-B	SSLA0-A	
N12		P76	CS6#-B	ET_RX_CLK/ REF50CK				
N13		P74	CS4#-B	ET_ERXD1/ RMII_RXD1				

1.5 Pin Functions

Table 1.8 lists the pin functions.

Table 1.9 Pin Functions (1 / 7)

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply.
	VCL	Input	Connect this pin to VSS via a 0.1-μF capacitor. The capacitor should be placed close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
	PLLVCC	Input	Power supply pin for the PLL circuit. Connect it to the system power supply.
	PLLVSS	Input	Ground pin for the PLL circuit.
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	BCLK	Output	Outputs the external bus clock for external devices.
	SDCLK	Output	Outputs the clock dedicated for the SDRAM.
	XCOUT	Output	Input/output pins for the subclock generation circuit. Connect a crystal resonator between XCOUT and XCIN.
	XCIN	Input	
Operating mode control	MD0, MD1, MDE	Input	Pins for setting the operating mode. The signal levels on these pins must not be changed during operation.
System control	RES#	Input	Reset signal input pin. This LSI enters the reset state when this signal goes low.
	EMLE	Input	Input pin to enable the connection of the on-chip emulator signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low.
	BSCANP	Input	Boundary scan pin. Boundary scan is enabled when this pin goes high. When not used, it should be driven low.
CNVSS	CNVSS	Input	Connect this pin to VSS via pull-down resister.
On-chip emulator	TRST#	Input	On-chip emulator pins or boundary scan pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator.
	TMS	Input	
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TRCLK	Output	This pin outputs the clock for synchronization with the trace data.
	TRSYNC	Output	This pin indicates that output from the TRDATA0 to TRDATA3 pins is valid.
	TRDATA0-A/TRDATA3-B	Output	These pins output the trace information.
Address bus	A0 to A15 A16-A/A16-B to A23-A/A23-B	Output	Output pins for the address.
Data bus	D0 to D31	I/O	Input and output pins for the bidirectional data bus.

4. I/O Registers

Table 4.1 List of I/O Registers (Address Order) (1 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 0000h	SYSTEM	Mode monitor register	MDMONR	16	16	3 ICLK
0008 0002h	SYSTEM	Mode status register	MDSR	16	16	3 ICLK
0008 0006h	SYSTEM	System control register 0	SYSCR0	16	16	3 ICLK
0008 0008h	SYSTEM	System control register 1	SYSCR1	16	16	3 ICLK
0008 000Ch	SYSTEM	Standby control register	SBYCR	16	16	3 ICLK
0008 0010h	SYSTEM	Module stop control register A	MSTPCRA	32	32	3 ICLK
0008 0014h	SYSTEM	Module stop control register B	MSTPCRB	32	32	3 ICLK
0008 0018h	SYSTEM	Module stop control register C	MSTPCRC	32	32	3 ICLK
0008 0020h	SYSTEM	System clock control register	SCKCR	32	32	3 ICLK
0008 0030h	SYSTEM	External bus clock control register	BCKCR	8	8	3 ICLK
0008 0040h	SYSTEM	Oscillation stop detection control register	OSTDCR	16	16	3 ICLK
0008 1300h	BSC	Bus error status clear register	BERCLR	8	8	2 ICLK
0008 1304h	BSC	Bus error monitoring enable register	BEREN	8	8	2 ICLK
0008 1308h	BSC	Bus error status register 1	BERSR1	8	8	2 ICLK
0008 130Ah	BSC	Bus error status register 2	BERSR2	16	16	2 ICLK
0008 2000h	DMAC0	DMA source address register	DMSAR	32	32	2 ICLK
0008 2004h	DMAC0	DMA destination address register	DMDAR	32	32	2 ICLK
0008 2008h	DMAC0	DMA transfer count register	DMCRA	32	32	2 ICLK
0008 200Ch	DMAC0	DMA block transfer count register	DMCRB	16	16	2 ICLK
0008 2010h	DMAC0	DMA transfer mode register	DMTMD	16	16	2 ICLK
0008 2013h	DMAC0	DMA interrupt setting register	DMINT	8	8	2 ICLK
0008 2014h	DMAC0	DMA address mode register	DMAMD	16	16	2 ICLK
0008 2018h	DMAC0	DMA offset register	DMOFR	32	32	2 ICLK
0008 201Ch	DMAC0	MA transfer enable register	DMCNT	8	8	2 ICLK
0008 201Dh	DMAC0	DMA software start register	DMREQ	8	8	2 ICLK
0008 201Eh	DMAC0	DMA status register	DMSTS	8	8	2 ICLK
0008 201Fh	DMAC0	DMA activation source flag control register	DMCSL	8	8	2 ICLK
0008 2040h	DMAC1	DMA source address register	DMSAR	32	32	2 ICLK
0008 2044h	DMAC1	DMA destination address register	DMDAR	32	32	2 ICLK
0008 2048h	DMAC1	DMA transfer count register	DMCRA	32	32	2 ICLK
0008 204Ch	DMAC1	DMA block transfer count register	DMCRB	16	16	2 ICLK
0008 2050h	DMAC1	DMA transfer mode register	DMTMD	16	16	2 ICLK
0008 2053h	DMAC1	DMA interrupt setting register	DMINT	8	8	2 ICLK
0008 2054h	DMAC1	DMA address mode register	DMAMD	16	16	2 ICLK
0008 205Ch	DMAC1	MA transfer enable register	DMCNT	8	8	2 ICLK
0008 205Dh	DMAC1	DMA software start register	DMREQ	8	8	2 ICLK
0008 205Eh	DMAC1	DMA status register	DMSTS	8	8	2 ICLK
0008 205Fh	DMAC1	DMA activation source flag control register	DMCSL	8	8	2 ICLK
0008 2080h	DMAC2	DMA source address register	DMSAR	32	32	2 ICLK
0008 2084h	DMAC2	DMA destination address register	DMDAR	32	32	2 ICLK
0008 2088h	DMAC2	DMA transfer count register	DMCRA	32	32	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (6 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 7044h	ICU	Interrupt request register 068	IR068	8	8	2 ICLK
0008 7045h	ICU	Interrupt request register 069	IR069	8	8	2 ICLK
0008 7046h	ICU	Interrupt request register 070	IR070	8	8	2 ICLK
0008 7047h	ICU	Interrupt request register 071	IR071	8	8	2 ICLK
0008 7048h	ICU	Interrupt request register 072	IR072	8	8	2 ICLK
0008 7049h	ICU	Interrupt request register 073	IR073	8	8	2 ICLK
0008 704Ah	ICU	Interrupt request register 074	IR074	8	8	2 ICLK
0008 704Bh	ICU	Interrupt request register 075	IR075	8	8	2 ICLK
0008 704Ch	ICU	Interrupt request register 076	IR076	8	8	2 ICLK
0008 704Dh	ICU	Interrupt request register 077	IR077	8	8	2 ICLK
0008 704Eh	ICU	Interrupt request register 078	IR078	8	8	2 ICLK
0008 704Fh	ICU	Interrupt request register 079	IR079	8	8	2 ICLK
0008 705Ah	ICU	Interrupt request register 090	IR090	8	8	2 ICLK
0008 705Bh	ICU	Interrupt request register 091	IR091	8	8	2 ICLK
0008 705Ch	ICU	Interrupt request register 092	IR092	8	8	2 ICLK
0008 7060h	ICU	Interrupt request register 096	IR096	8	8	2 ICLK
0008 7062h	ICU	Interrupt request register 098	IR098	8	8	2 ICLK
0008 7063h	ICU	Interrupt request register 099	IR099	8	8	2 ICLK
0008 7066h	ICU	Interrupt request register 102	IR102	8	8	2 ICLK
0008 7072h	ICU	Interrupt request register 114	IR114	8	8	2 ICLK
0008 7073h	ICU	Interrupt request register 115	IR115	8	8	2 ICLK
0008 7074h	ICU	Interrupt request register 116	IR116	8	8	2 ICLK
0008 7075h	ICU	Interrupt request register 117	IR117	8	8	2 ICLK
0008 7076h	ICU	Interrupt request register 118	IR118	8	8	2 ICLK
0008 7077h	ICU	Interrupt request register 119	IR119	8	8	2 ICLK
0008 7078h	ICU	Interrupt request register 120	IR120	8	8	2 ICLK
0008 7079h	ICU	Interrupt request register 121	IR121	8	8	2 ICLK
0008 707Ah	ICU	Interrupt request register 122	IR122	8	8	2 ICLK
0008 707Bh	ICU	Interrupt request register 123	IR123	8	8	2 ICLK
0008 707Ch	ICU	Interrupt request register 124	IR124	8	8	2 ICLK
0008 707Dh	ICU	Interrupt request register 125	IR125	8	8	2 ICLK
0008 707Eh	ICU	Interrupt request register 126	IR126	8	8	2 ICLK
0008 707Fh	ICU	Interrupt request register 127	IR127	8	8	2 ICLK
0008 7080h	ICU	Interrupt request register 128	IR128	8	8	2 ICLK
0008 7081h	ICU	Interrupt request register 129	IR129	8	8	2 ICLK
0008 7082h	ICU	Interrupt request register 130	IR130	8	8	2 ICLK
0008 7083h	ICU	Interrupt request register 131	IR131	8	8	2 ICLK
0008 7084h	ICU	Interrupt request register 132	IR132	8	8	2 ICLK
0008 7085h	ICU	Interrupt request register 133	IR133	8	8	2 ICLK
0008 7086h	ICU	Interrupt request register 134	IR134	8	8	2 ICLK
0008 7087h	ICU	Interrupt request register 135	IR135	8	8	2 ICLK
0008 7088h	ICU	Interrupt request register 136	IR136	8	8	2 ICLK
0008 7089h	ICU	Interrupt request register 137	IR137	8	8	2 ICLK
0008 708Ah	ICU	Interrupt request register 138	IR138	8	8	2 ICLK
0008 708Bh	ICU	Interrupt request register 139	IR139	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (16 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 8209h	TMR1	Timer counter	TCNT	8	8	2 to 3 PCLK*8
0008 820Ah	TMR0	Timer counter control register	TCCR	8	8	2 to 3 PCLK*8
0008 820Bh	TMR1	Timer counter control register	TCCR	8	8	2 to 3 PCLK*8
0008 8204h	TMR01	Time constant register A	TCORA	16	16	2 to 3 PCLK*8
0008 8206h	TMR01	Time constant register B	TCORB	16	16	2 to 3 PCLK*8
0008 8208h	TMR01	Timer counter	TCNT	16	16	2 to 3 PCLK*8
0008 820Ah	TMR01	Timer counter control register	TCCR	16	16	2 to 3 PCLK*8
0008 8210h	TMR2	Timer control register	TCR	8	8	2 to 3 PCLK*8
0008 8211h	TMR3	Timer control register	TCR	8	8	2 to 3 PCLK*8
0008 8212h	TMR2	Timer control/status register	TCSR	8	8	2 to 3 PCLK*8
0008 8213h	TMR3	Timer control/status register	TCSR	8	8	2 to 3 PCLK*8
0008 8214h	TMR2	Time constant register A	TCORA	8	8	2 to 3 PCLK*8
0008 8215h	TMR3	Time constant register A	TCORA	8	8	2 to 3 PCLK*8
0008 8216h	TMR2	Time constant register B	TCORB	8	8	2 to 3 PCLK*8
0008 8217h	TMR3	Time constant register B	TCORB	8	8	2 to 3 PCLK*8
0008 8218h	TMR2	Timer counter	TCNT	8	8	2 to 3 PCLK*8
0008 8219h	TMR3	Timer counter	TCNT	8	8	2 to 3 PCLK*8
0008 821Ah	TMR2	Timer counter control register	TCCR	8	8	2 to 3 PCLK*8
0008 821Bh	TMR3	Timer counter control register	TCCR	8	8	2 to 3 PCLK*8
0008 8214h	TMR23	Time constant register A	TCORA	16	16	2 to 3 PCLK*8
0008 8216h	TMR23	Time constant register B	TCORB	16	16	2 to 3 PCLK*8
0008 8218h	TMR23	Timer counter	TCNT	16	16	2 to 3 PCLK*8
0008 821Ah	TMR23	Timer counter control register	TCCR	16	16	2 to 3 PCLK*8
0008 8240h	SCI0	Serial mode register	SMR	8	8	2 to 3 PCLK*8
0008 8241h	SCI0	Bit rate register	BRR	8	8	2 to 3 PCLK*8
0008 8242h	SCI0	Serial control register	SCR	8	8	2 to 3 PCLK*8
0008 8243h	SCI0	Transmit data register	TDR	8	8	2 to 3 PCLK*8
0008 8244h	SCI0	Serial status register	SSR	8	8	2 to 3 PCLK*8
0008 8245h	SCI0	Receive data register	RDR	8	8	2 to 3 PCLK*8
0008 8246h	SCI0	Smart card mode register	SCMR	8	8	2 to 3 PCLK*8
0008 8247h	SCI0	Serial extended mode register	SEMR	8	8	2 to 3 PCLK*8
0008 8240h	SMCI0	Serial mode register	SMR	8	8	2 to 3 PCLK*8
0008 8241h	SMCI0	Bit rate register	BRR	8	8	2 to 3 PCLK*8
0008 8242h	SMCI0	Serial control register	SCR	8	8	2 to 3 PCLK*8
0008 8243h	SMCI0	Transmit data register	TDR	8	8	2 to 3 PCLK*8
0008 8244h	SMCI0	Serial status register	SSR	8	8	2 to 3 PCLK*8
0008 8245h	SMCI0	Receive data register	RDR	8	8	2 to 3 PCLK*8
0008 8246h	SMCI0	Smart card mode register	SCMR	8	8	2 to 3 PCLK*8
0008 8248h	SCI1	Serial mode register	SMR	8	8	2 to 3 PCLK*8
0008 8249h	SCI1	Bit rate register	BRR	8	8	2 to 3 PCLK*8
0008 824Ah	SCI1	Serial control register	SCR	8	8	2 to 3 PCLK*8
0008 824Bh	SCI1	Transmit data register	TDR	8	8	2 to 3 PCLK*8
0008 824Ch	SCI1	Serial status register	SSR	8	8	2 to 3 PCLK*8
0008 824Dh	SCI1	Receive data register	RDR	8	8	2 to 3 PCLK*8
0008 824Eh	SCI1	Smart card mode register	SCMR	8	8	2 to 3 PCLK*8

Table 4.1 List of I/O Registers (Address Order) (29 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 C412h	RTC	Minute alarm register	RMINAR	8	8	2 to 3 PCLK*8
0008 C414h	RTC	Hour alarm register	RHRAR	8	8	2 to 3 PCLK*8
0008 C416h	RTC	Day-of-week alarm register	RWKAR	8	8	2 to 3 PCLK*8
0008 C418h	RTC	Date alarm register	RDAYAR	8	8	2 to 3 PCLK*8
0008 C41Ah	RTC	Month alarm register	RMONAR	8	8	2 to 3 PCLK*8
0008 C41Ch	RTC	Year alarm register	RYRAR	16	16	2 to 3 PCLK*8
0008 C41Eh	RTC	Year alarm enable register	RYRAREN	8	8	2 to 3 PCLK*8
0008 C422h	RTC	RTC control register 1	RCR1	8	8	2 to 3 PCLK*8
0008 C424h	RTC	RTC control register 2	RCR2	8	8	2 to 3 PCLK*8
0009 0200h to 0009 03FFh	CAN0	Mailbox registers 0 to 31	MB0 to MB31	128	8, 16, 32	2 to 3 PCLK*8
0009 0400h	CAN0	Mask register 0	MKR0	32	8, 16, 32	2 to 3 PCLK*8
0009 0404h	CAN0	Mask register 1	MKR1	32	8, 16, 32	2 to 3 PCLK*8
0009 0408h	CAN0	Mask register 2	MKR2	32	8, 16, 32	2 to 3 PCLK*8
0009 040Ch	CAN0	Mask register 3	MKR3	32	8, 16, 32	2 to 3 PCLK*8
0009 0410h	CAN0	Mask register 4	MKR4	32	8, 16, 32	2 to 3 PCLK*8
0009 0414h	CAN0	Mask register 5	MKR5	32	8, 16, 32	2 to 3 PCLK*8
0009 0418h	CAN0	Mask register 6	MKR6	32	8, 16, 32	2 to 3 PCLK*8
0009 041Ch	CAN0	Mask register 7	MKR7	32	8, 16, 32	2 to 3 PCLK*8
0009 0420h	CAN0	FIFO received ID compare register 0	FIDCR0	32	8, 16, 32	2 to 3 PCLK*8
0009 0424h	CAN0	FIFO received ID compare register 1	FIDCR1	32	8, 16, 32	2 to 3 PCLK*8
0009 0428h	CAN0	Mask invalid register	MKIVLR	32	8, 16, 32	2 to 3 PCLK*8
0009 042Ch	CAN0	Mailbox interrupt enable register	MIER	32	8, 16, 32	2 to 3 PCLK*8
0009 0820h to 0009 083Fh	CAN0	Message control registers 0 to 31	MCTL0 to MCTL31	8	8	2 to 3 PCLK*8
0009 0840h	CAN0	Control register	CTLR	16	8, 16	2 to 3 PCLK*8
0009 0842h	CAN0	Status register	STR	16	8, 16	2 to 3 PCLK*8
0009 0844h	CAN0	Bit configuration register	BCR	32	8, 16, 32	2 to 3 PCLK*8
0009 0848h	CAN0	Receive FIFO control register	RFCR	8	8	2 to 3 PCLK*8
0009 0849h	CAN0	Receive FIFO pointer control register	RFPCR	8	8	2 to 3 PCLK*8
0009 084Ah	CAN0	Transmit FIFO control register	TFCR	8	8	2 to 3 PCLK*8
0009 084Bh	CAN0	Transmit FIFO pointer control register	TFPCR	8	8	2 to 3 PCLK*8
0009 084Ch	CAN0	Error interrupt enable register	EIER	8	8	2 to 3 PCLK*8
0009 084Dh	CAN0	Error interrupt factor judge register	EIFR	8	8	2 to 3 PCLK*8
0009 084Eh	CAN0	Receive error count register	RECR	8	8	2 to 3 PCLK*8
0009 084Fh	CAN0	Transmit error count register	TECR	8	8	2 to 3 PCLK*8
0009 0850h	CAN0	Error code store register	ECSR	8	8	2 to 3 PCLK*8
0009 0851h	CAN0	Channel search support register	CSSR	8	8	2 to 3 PCLK*8
0009 0852h	CAN0	Mailbox search status register	MSSR	8	8	2 to 3 PCLK*8
0009 0853h	CAN0	Mailbox search mode register	MSMR	8	8	2 to 3 PCLK*8
0009 0854h	CAN0	Time stamp register	TSR	16	8, 16	2 to 3 PCLK*8
0009 0856h	CAN0	Acceptance filter support register	AFSR	16	8, 16	2 to 3 PCLK*8
0009 0858h	CAN0	Test control register	TCR	8	8	2 to 3 PCLK*8
000A 0000h	USB0	System configuration control register	SYSCFG	16	16	3 to 4 PCLK*8
000A 0004h	USB0	System configuration status register 0	SYSSTS0	16	16	at least 9 PCLK*9

5.3.1 Clock Timing

Table 5.8 Clock Timing

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
T_a = -40 to +85°C

Item	Symbol	Min.	Max.	Unit	Test Conditions
BCLK pin output cycle time [176-pin LFBGA/145-pin TFLGA/144-pin LQFP]	t_{Bcyc}	20	125	ns	Figure 5.1
BCLK pin output cycle time [100-pin LQFP/85-pin TFLGA]	t_{Bcyc}	40	125	ns	
BCLK pin output high pulse width	t_{CH}	5	—	ns	
BCLK pin output low pulse width	t_{CL}	5	—	ns	
BCLK pin output rising time	t_{Cr}	—	5	ns	
BCLK pin output falling time	t_{Cf}	—	5	ns	
SDCLK pin output cycle time	t_{SDcyc}	20	125	ns	
SDCLK pin output high pulse width	t_{CH}	5	—	ns	
SDCLK pin output low pulse width	t_{CL}	5	—	ns	
SDCLK pin output rising time	t_{Cr}	—	5	ns	
SDCLK pin output falling time	t_{Cf}	—	5	ns	
Oscillation settling time after reset (crystal)	t_{OSC1}	10	—	ms	Figure 5.2
Oscillation settling time after leaving software standby mode (crystal)	t_{OSC2}	10	—	ms	Figure 5.3
Oscillation settling time after leaving deep software standby mode (crystal)	t_{OSC3}	10	—	ms	Figure 5.4
EXTAL external clock output delay settling time	t_{DEXT}	1	—	ms	Figure 5.2
EXTAL external clock input low pulse width	t_{EXL}	30.71	—	ns	Figure 5.5
EXTAL external clock input high pulse width	t_{EXH}	30.71	—	ns	
EXTAL external clock rising time	t_{EXr}	—	5	ns	
EXTAL external clock falling time	t_{EXf}	—	5	ns	
XCIN sub-clock oscillation settling time	t_{SUBOSC}	2	—	s	Figure 5.6
XCIN sub-clock oscillation frequency	f_{SUB}	32.768	—	kHz	
On-chip oscillator (IWDTCLK) oscillation frequency	$f_{IWDTCLK}$	62.5	187.5	kHz	

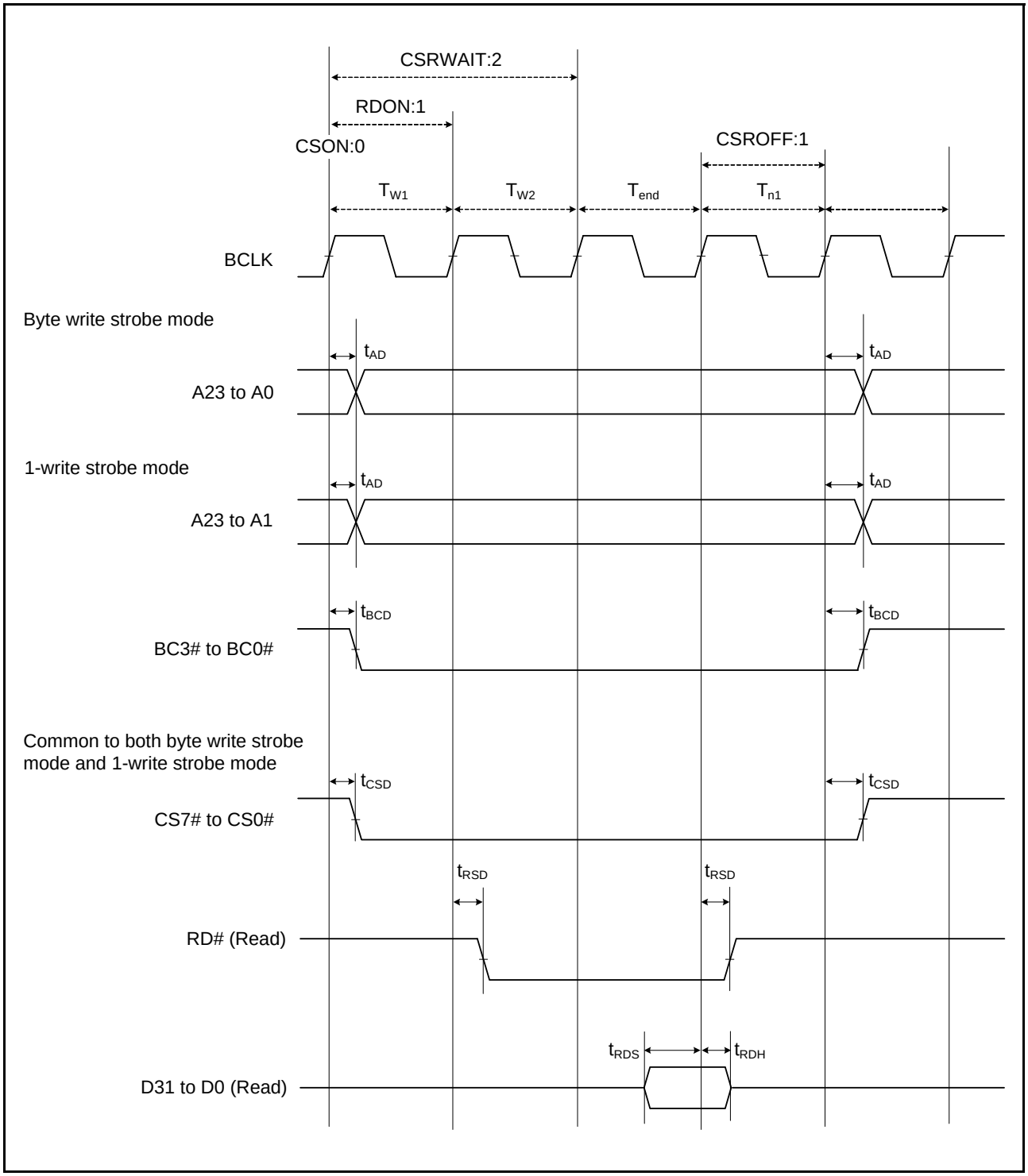


Figure 5.10 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)

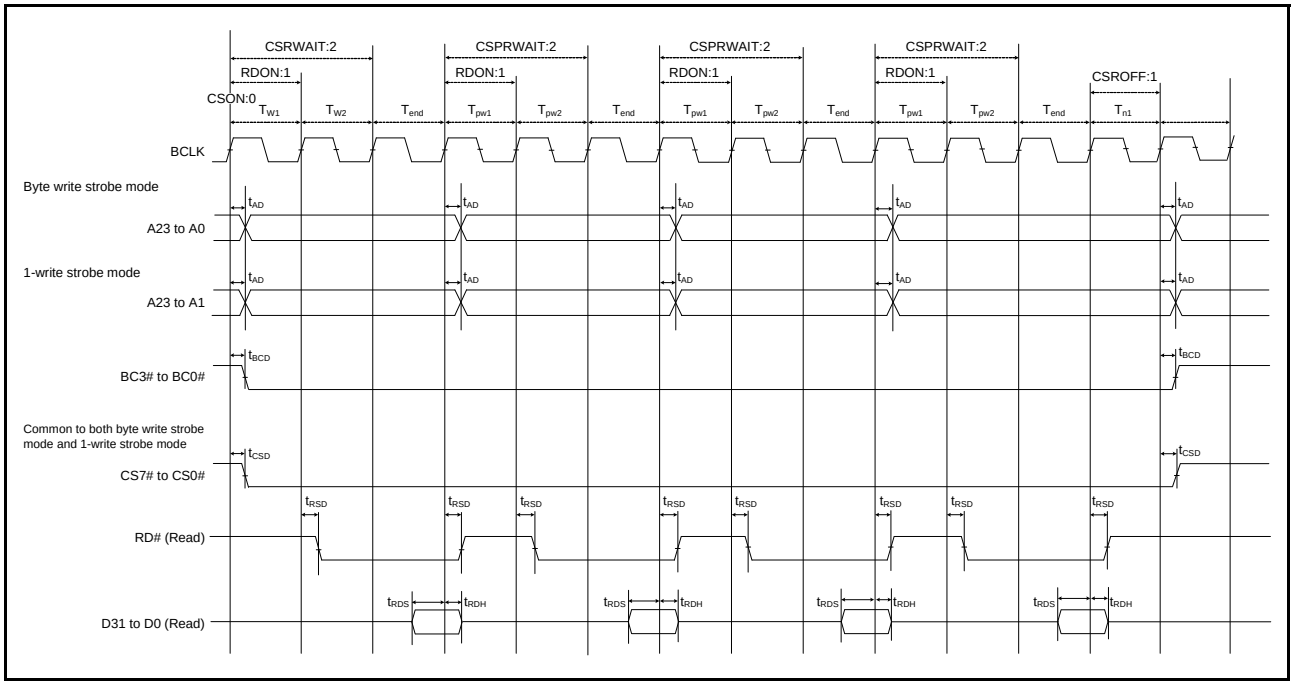


Figure 5.12 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)

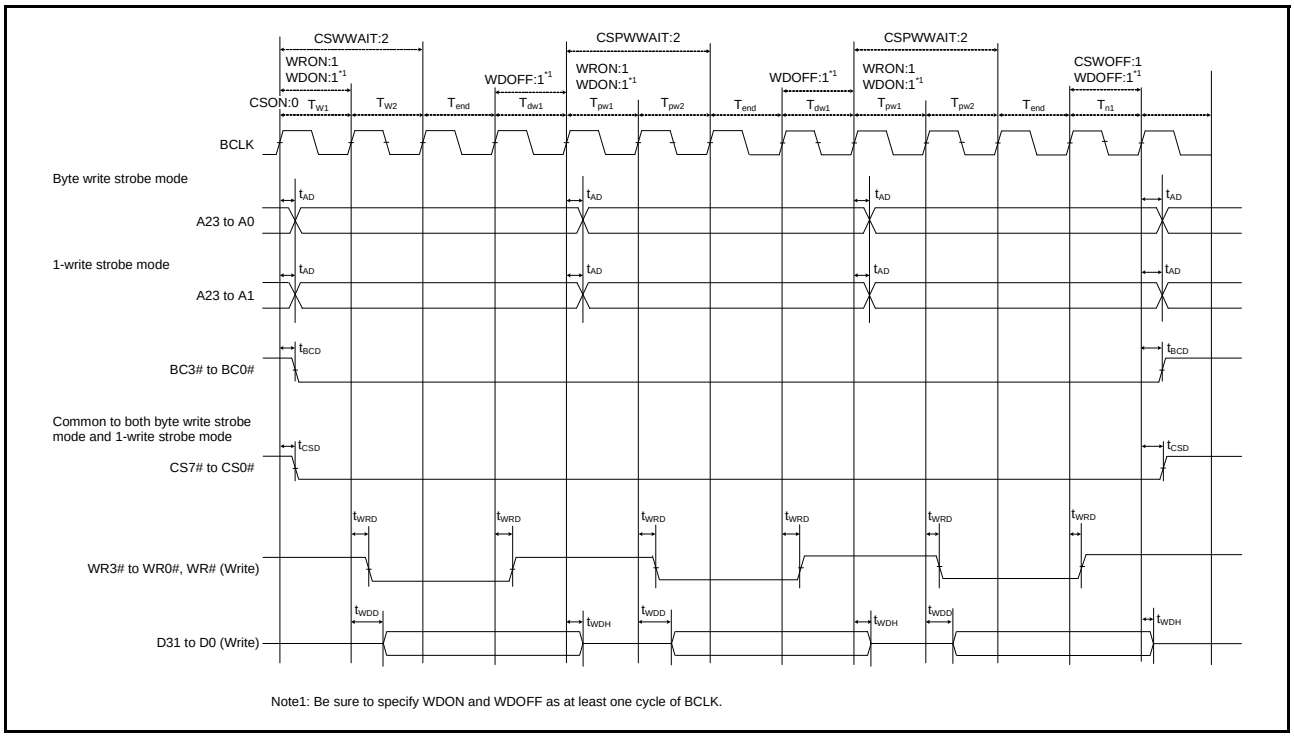


Figure 5.13 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)

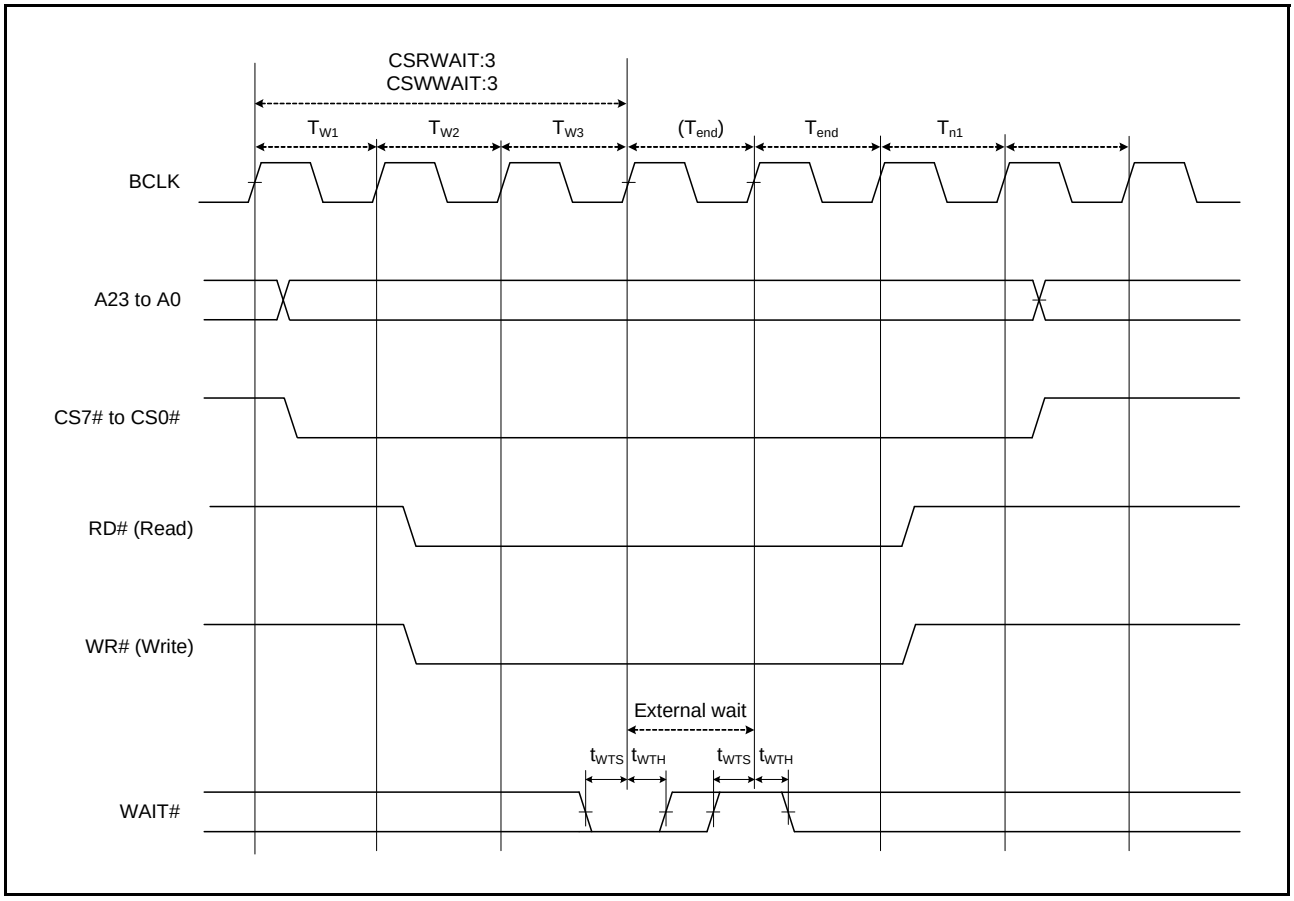


Figure 5.14 External Bus Timing/External Wait Control

Table 5.14 Timing of On-Chip Peripheral Modules (3)

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
PCLK = 8 to 50 MHz
T_a = -40 to +85°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
CAN	Transmit data delay time		t_{CTXD}	—	40.0	ns	Figure 5.37
	Receive data setup time		t_{CRXS}	40.0	—	ns	
	Receive data hold time		t_{CRXH}	40.0	—	ns	
RSPI	RSPCK clock cycle	Master	t_{SPcyc}	2	4096	t_{Pcyc} *1	Figure 5.38
		Slave		8	4096		
	RSPCK clock high pulse width	Master	t_{SPCKWH}	$(t_{SPcyc}-t_{SPCKR}-t_{SPCKF})$ / 2-3	—	ns	
		Slave		$(t_{SPcyc}-t_{SPCKR}-t_{SPCKF})$ / 2	—		
	RSPCK clock low pulse width	Master	t_{SPCKWL}	$(t_{SPcyc}-t_{SPCKR}-t_{SPCKF})$ / 2-3	—	ns	
		Slave		$(t_{SPcyc}-t_{SPCKR}-t_{SPCKF})$ / 2	—		
	RSPCK clock rise/fall time	Output [176-pin LFBGA/ 145-pin TFLGA/ 144-pin LQFP]	t_{SPCKr}, t_{SPCKf}	—	5	ns	
		Output [100-pin LQFP/ 85-pin TFLGA]		—	10		
		Input		—	1	µs	

Note 1. tPcyc: PCLK cycle

Table 5.14 Timing of On-Chip Peripheral Modules (4)

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
PCLK = 8 to 50 MHz
T_a = -40 to +85°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
RSPI	Data input setup time	Master [176-pin LFBGA/ 145-pin TFLGA/ 144-pin LQFP]	t_{SU}	16	—	ns	Figure 5.39 to Figure 5.42
		Master [100-pin LQFP/ 85-pin TFLGA]		30	—		
		Slave		20-2 × t_{Pcyc}	—		
	Data input hold time	Master	t_H	0	—	ns	
		Slave		20+2 × t_{Pcyc}	—		
	SSL setup time	Master	t_{LEAD}	1	8	t_{SPcyc}	
		Slave		4	—	t_{Pcyc}	
	SSL hold time	Master	t_{LAG}	1	8	t_{SPcyc}	
		Slave		4	—	t_{Pcyc}	
	Data output delay time	Master [176-pin LFBGA/ 145-pin TFLGA/ 144-pin LQFP]	t_{OD}	—	20	ns	
		Master [100-pin LQFP/ 85-pin TFLGA]		—	30		
		Slave [176-pin LFBGA/ 145-pin TFLGA/ 144-pin LQFP]		—	3 × t_{Pcyc}+40		
		Slave [100-pin LQFP/ 85-pin TFLGA]		—	3 × t_{Pcyc}+50		

Note 1. tPcyc: PCLK cycle

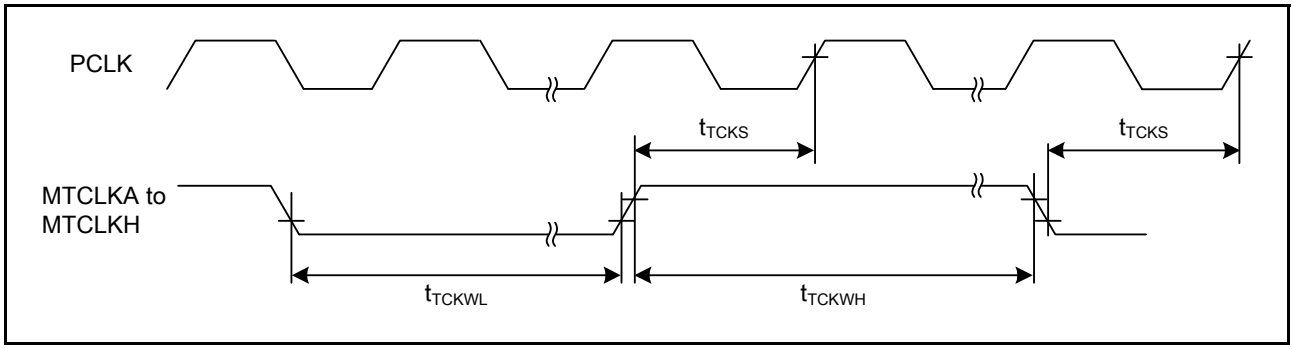


Figure 5.27 MTU2 Clock Input Timing

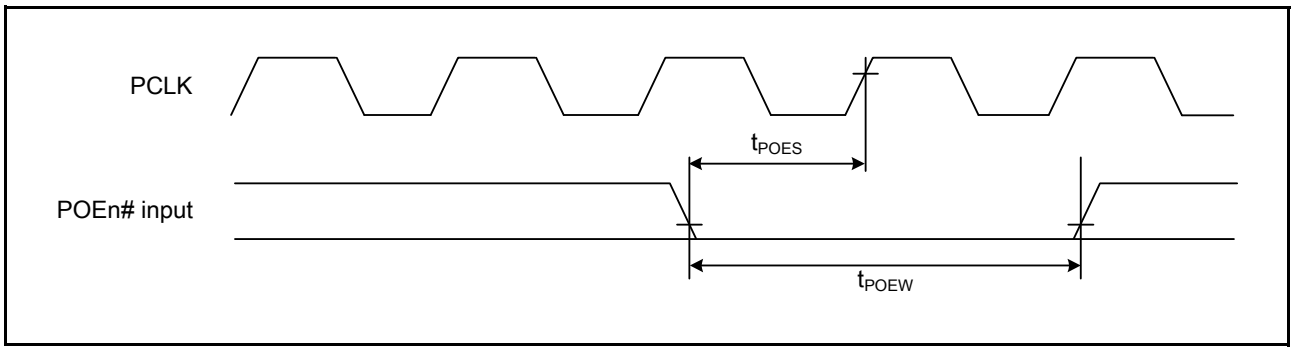


Figure 5.28 POE# Input Timing

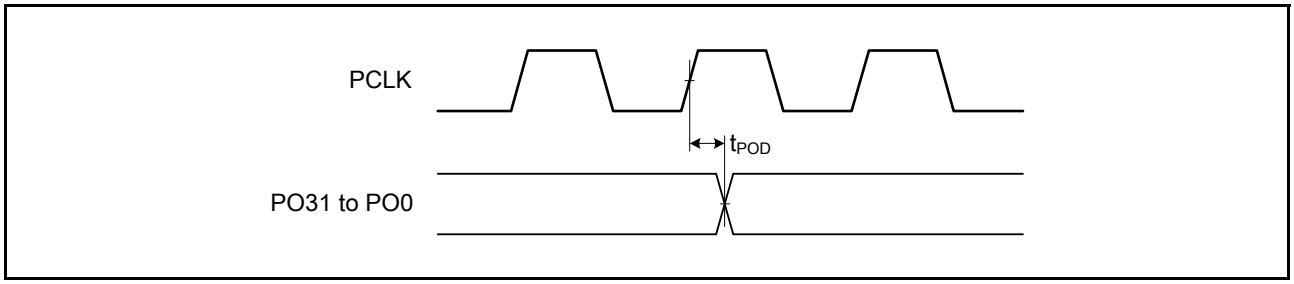


Figure 5.29 PPG Output Timing

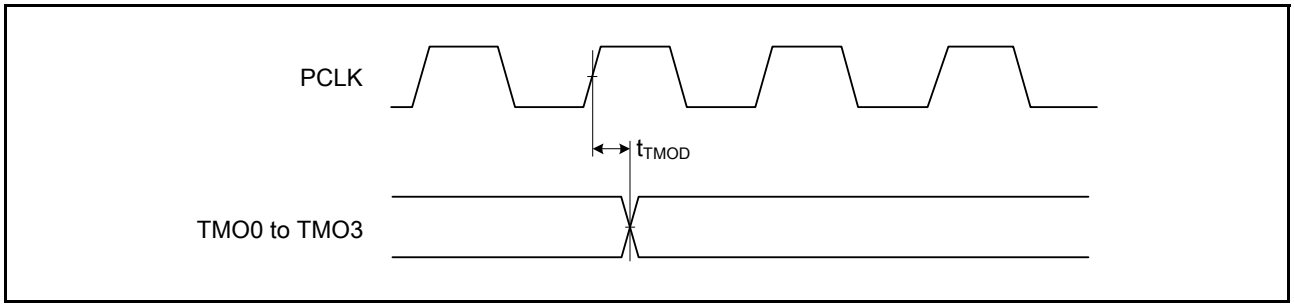


Figure 5.30 8-Bit Timer Output Timing

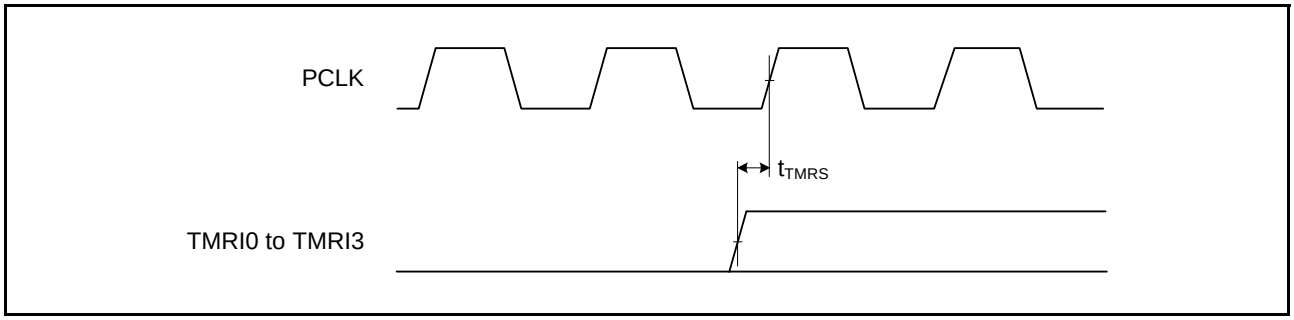


Figure 5.31 8-Bit Timer Reset Input Timing

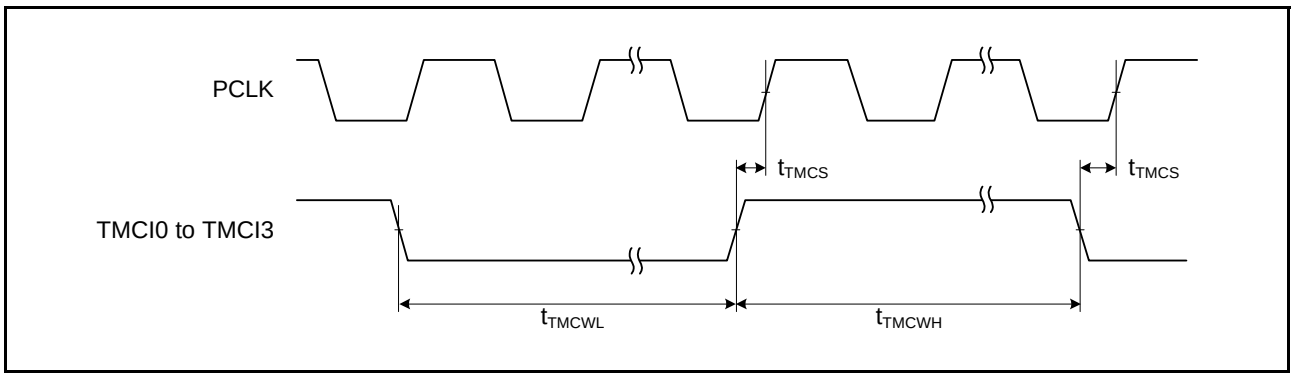


Figure 5.32 8-Bit Timer Clock Input Timing

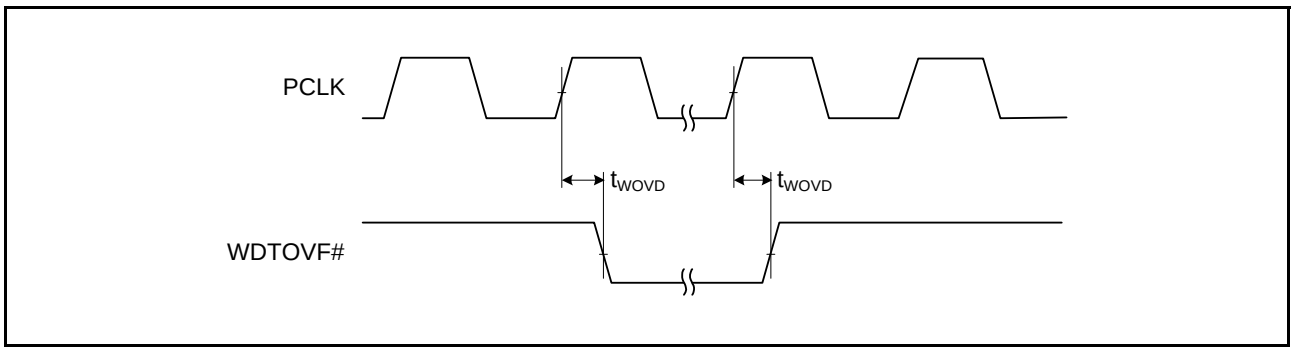


Figure 5.33 WDT Output Timing

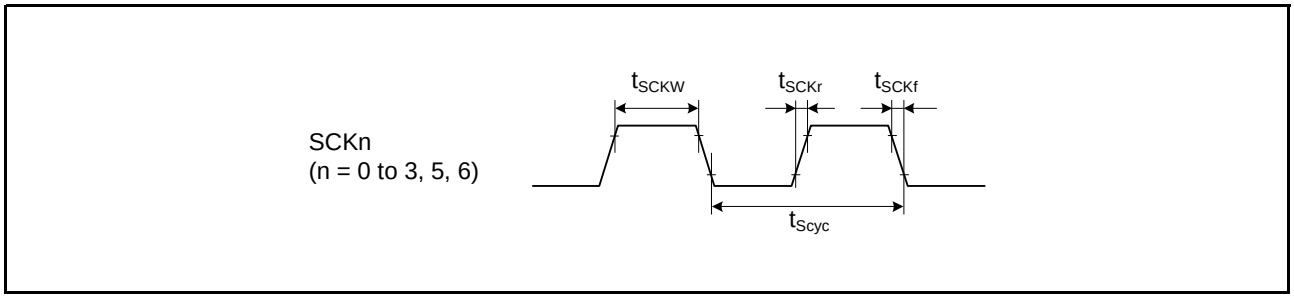


Figure 5.34 SCK Clock Input Timing

5.5 A/D Conversion Characteristics

Table 5.20 10-Bit A/D Conversion Characteristics

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
PCLK = 8 to 50 MHz
T_a = -40 to +85°C

Item			Min.	Typ.	Max.	Unit	Test Conditions
Resolution			10	10	10	bits	
Conversion time*1 (PCLK = 50-MHz operation)	With 0.1-µF external capacitor	When the capacitor is charged enough*2	0.8 (0.3)*3	—	—	µs	Sampling 15 states
	Without external capacitor	Permissible signal source impedance (max.) = 1.0 kΩ	1.0 (0.5)*3	—	—		Sampling 25 states
		Permissible signal source impedance (max.) = 5.0 kΩ	2.6 (2.1)*3	—	—		Sampling 105 states
Analog input capacitance			—	—	6.0	pF	
INL integral nonlinearity error			—	±1.5	±3.0	LSB	
Offset error			—	±1.5	±3.0	LSB	
Full-scale error			—	±1.5	±3.0	LSB	
Quantization error			—	±0.5	—	LSB	
Absolute accuracy			—	±1.5	±3.0	LSB	
DNL differential nonlinearity error			—	±0.5	±1.0	LSB	

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.
Note 2. The scanning is not supported.
Note 3. The value in parentheses indicates the sampling time.

Table 5.21 12-Bit A/D Conversion Characteristics

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
PCLK = 8 to 50 MHz
T_a = -40 to +85°C

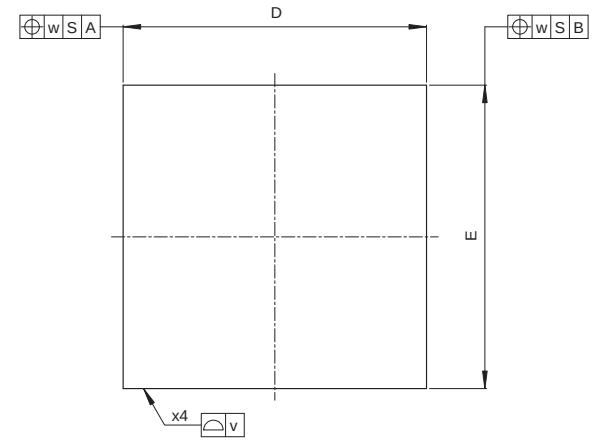
Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	12	12	12	bits	
Conversion time*1	1.0	—	—	µs	AVCC ≥ 3.0
	2.0	—	—	µs	AVCC ≥ 2.7
Analog input capacitance	—	—	30	pF	
Offset error	—	±2.0	±7.5	LSB	
Full-scale error	—	±2.0	±7.5	LSB	
Quantization error	—	±0.5	—	LSB	
Absolute accuracy	—	±2.5	±8.0	LSB	
Nonlinearity error	—	±2.0	±4.0	LSB	

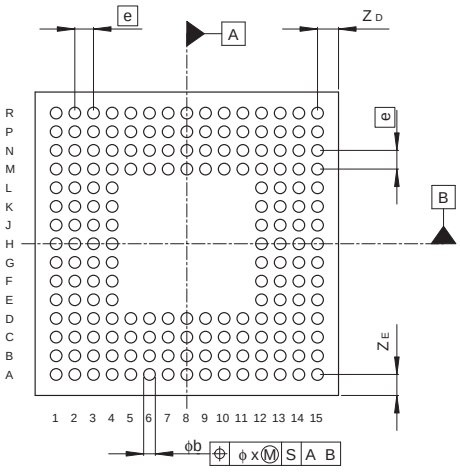
Note 1. The time conversion takes is the sum of the sampling interval and the time comparison takes (permissible signal-source impedance is up to 1.0 kΩ)

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in "Packages" on Renesas Electronics Corp website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFBGA176-13x13-0.80	PLBG0176GA-A	BP-176/BP-176V	0.45g





Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	13.0	—
E	—	13.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.40
A_1	0.35	0.40	0.45
e	—	0.80	—
b	0.45	0.50	0.55
x	—	—	0.08
y	—	—	0.10
y_1	—	—	0.2
S_D	—	—	—
S_E	—	—	—
Z_D	—	0.90	—
Z_E	—	0.90	—

Figure A 176-Pin LFBGA (PLBG0176GA-A) Package Dimensions