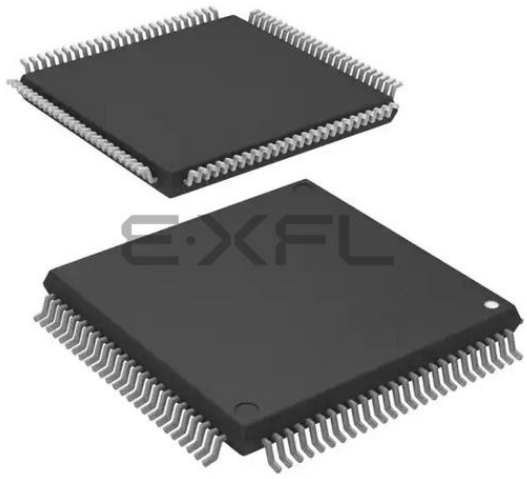
Renesas Electronics America Inc - R5F562N7BDFP#V0 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	72
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562n7bdfp-v0

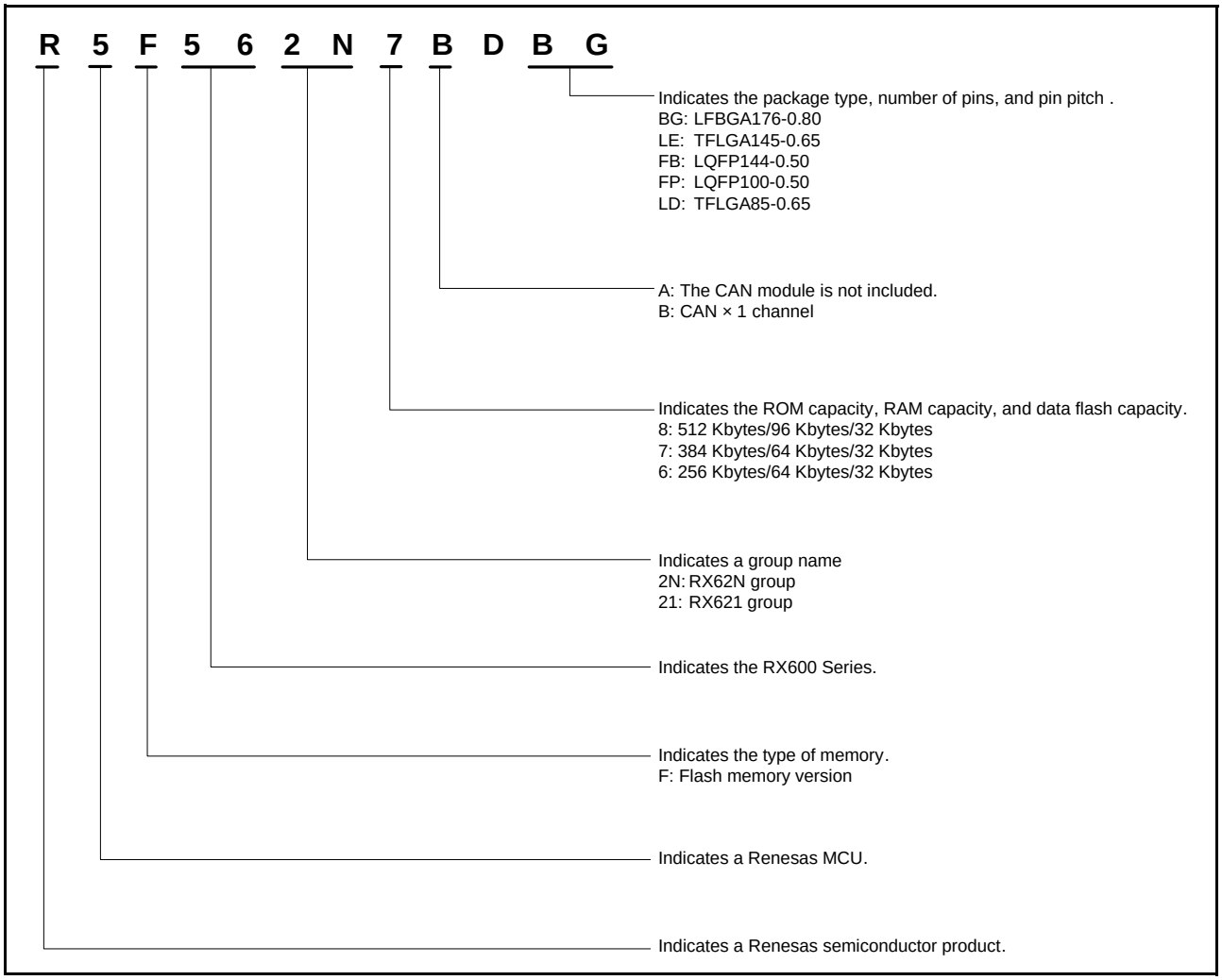

Figure 1.1 How to Read the Product Part No.

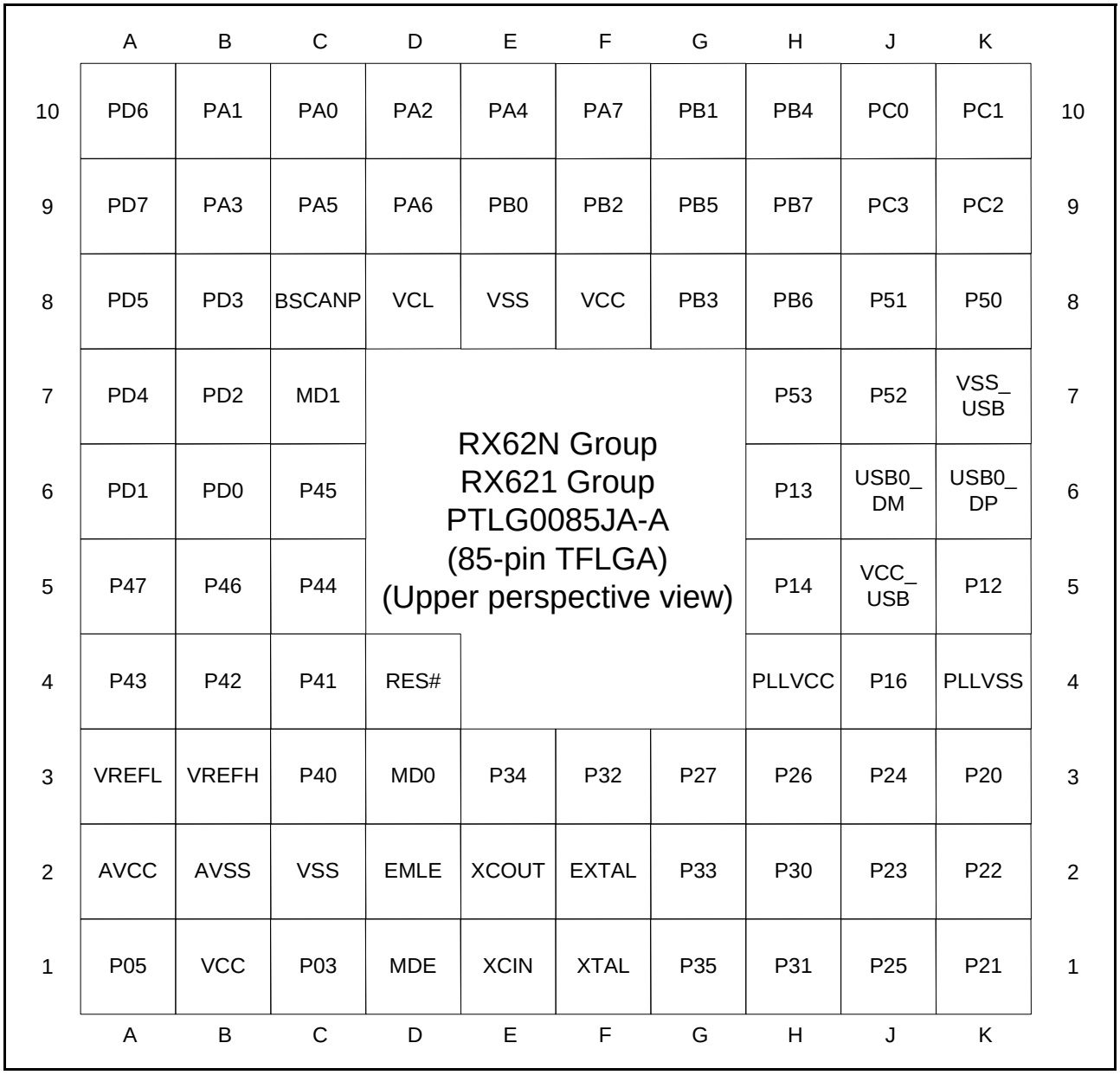

Figure 1.9 Pin Assignment of the 85-Pin TFLGA

Table 1.5 List of Pins and Pin Functions (145-Pin TFLGA) (1 / 5)

Pin No. 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	External Bus EXDMAC	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE, WDT)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
A1	AVSS							
A2	AVCC							
A3	VREFL							
A4		P42						IRQ10-B/AN2
A5		P44						IRQ12/AN4
A6		P47						IRQ15-B/AN7
A7		P91	A17-B					
A8		PD0	D0			POE7#		
A9		PD3	D3			MTIC11V-B/ POE4#		
A10		PD6	D6			MTIC5V/ POE1#		
A11		P60	CS0#-A					
A12		P62	CS2#-A/ RAS#					
A13		P64	CS4#-A/ WE#					
B1		P03						IRQ11-A/DA0
B2		P07						IRQ15-A/ ADTRG0#-A
B3	VREFH							
B4		P40						IRQ8-B/AN0
B5		P45						IRQ13-B/AN5
B6		P90	A16-B					
B7		PD1	D1			POE6#		
B8		PD5	D5			MTIC5W/ POE2#		
B9	VSS							
B10		PE0	D8				SSLB1-B	
B11		PE2	D10			POE9#	SSLB3-B	
B12		PE1	D9				SSLB2-B	
B13		PE4	D12				SSLB0-B	
C1		P01				TMCI0-A	RxD6-A	IRQ9-A
C2		P05						IRQ13-A/DA1
C3	VSS							
C4		P41						IRQ9-B/AN1
C5		P46						IRQ14/AN6
C6		P92	A18-B					
C7		PD2	D2			MTIC11W-B/ POE5#		
C8		PD7	D7			MTIC5U/ POE0#		
C9		P61	CS1#-A/ SDCS#					

Table 1.5 List of Pins and Pin Functions (145-Pin TFLGA) (3 / 5)

Pin No. 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	External Bus EXDMAC	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE, WDT)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
G3	MD1							
G4	MD0							
G10	VSS							
G11		PA5	A5			MTIOC7B/ PO21	RSPCKA-B	
G12		PA6	A6			MTIOC8A/ PO22	MOSIA-B	
G13		PA4	A4			MTIOC7A/ PO20	SSLA0-B	
H1	EXTAL							
H2		P34				MTIOC0A/ TMCI3/ PO12	SCK6-B	IRQ4-A/ TRST#
H3	VCC							
H4	RES#							
H10		PB0	A8			MTIOC9A/ PO24		
H11		P71	CS1#-B	ET_MDIO				
H12		PB1	A9			MTIOC9C/ PO25		
H13		PA7	A7			MTIOC8B/ PO23	MISOA-B	
J1		P33				MTIOC0D/ PO11	CRX0/ RxD6-B	IRQ3-A
J2		P27	CS7#-C			MTIOC2B/ PO7	RSPCKB-A/ SCK1	TCK
J3		P35						NMI
J4		P32				MTIOC0C/ PO10/ RTCOUT	CTX0/ TxD6-B	IRQ2-A
J10		PB2	A10			MTIOC9B/ MTCLKG-B/ PO26		
J11		PB4	A12			MTIOC10A/ MTCLKE-B/ PO28		
J12		PB5	A13			MTIOC10C/ MTCLKF-B/ PO29		
J13		P72	CS2#-B	ET_MDC				
K1		P30				MTIOC4B-A/ TMRI3/ PO8	RxD1/ MISOB-A	IRQ0/ TDI
K2		P24	CS4#-C/ EDREQ1-B		USB0_VBUSEN-A	MTIOC4A-A/ MTCLKA-A/ TMRI1/PO4	SCK3-B	
K3		P31				MTIOC4D-A/ TMCI2-B/ PO9	SSLB0-A	IRQ1/ TMS

Table 1.5 List of Pins and Pin Functions (145-Pin TFLGA) (4 / 5)

Pin No. 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	External Bus EXDMAC	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE, WDT)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
K4		P26	CS6#-C			MTIOC2A/ TMO1/ PO6	MOSIB-A/ TxD1	TDO
K5	BCLK	P53						
K6	VSS							
K7		PC7	A23/ CS0#-B	ET_COL		MTIC11U-A/ MTCLKB-B	MISOA-A	
K8		P82	EDREQ1-A	ET_ETXD1/ RMII_TXD1		MTIOC4A-B		TRSYNC
K9		PC3	A19-A	ET_TX_ER		MTCLKF-A	TxD5	
K10		PB7	A15			MTIOC10D/ PO31		
K11		P73	CS3#-B	ET_WOL				
K12		PC0	A16-A	ET_ERXD3		MTCLKG-A	SSLA1-A	
K13		PB3	A11			MTIOC9D/ MTCLKH-B/ PO27		
L1		P25	CS5#-C/ EDACK1-B		USB0_DPRPD	MTIOC4C-A/ MTCLKB-A/ PO5	RxD3-B	ADTRG0#-B
L2		P22	EDREQ0-B		USB0_DRPD	MTIOC3B-A/ MTCLKC-A/ TMO0/PO2	SCK0	
L3		P17				MTIOC3A/ PO15	TxD3-A	IRQ7-B
L4		P12				TMCI1-B	SCL0/ RxD2-A	IRQ2-B
L5	VCC_USB							
L6		P56	EDACK1-C			MTIOC3C-B		
L7		P52	RD#				SSLB3-A/ RxD2-B	
L8		P83	EDACK1-A	ET_CRS/ RMII_CRS_DV		MTIOC4C-B		TRCLK
L9		P81	EDACK0-A	ET_ETXD0/ RMII_TXD0		MTIOC3D-B		TRDATA1
L10		P77	CS7#-B	ET_RX_ER/ RMII_RX_ER				
L11		P75	CS5#-B	ET_ERXD0/ RMII_RXD0				
L12	VCC							
L13		PB6	A14			MTIOC10B/ PO30		
M1		P23	EDACK0-B		USB0_DPUPE-A	MTIOC3D-A/ MTCLKD-A/ PO3	TxD3-B	
M2		P20			USB0_ID	MTIOC1A/ TMRI0-B/ PO0	SDA1/ TxD0	
M3	PLLVCC							

Table 1.5 List of Pins and Pin Functions (145-Pin TFLGA) (5 / 5)

Pin No. 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	External Bus EXDMAC	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE, WDT)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
M4		P15				MTIOC0B/ TMCI2-A/ PO13	SCK3-A	IRQ5-B
M5		P14			USB0_OVRCURA/ USB0_DPUPE-B	TMRI2		IRQ4-B
M6	VSS_USB							
M7		P55	WAIT#-B/ EDREQ0-C	ET_EXOUT		MTIOC4D-B		TRDATA3
M8		P50	WR0#/ WR#				SSLB1-A/ TxD2-B	
M9		PC6	A22/CS1#-C	ET_ETXD3		MTIC11V-A/ MTCLKA-B	MOSIA-A	
M10		P80	EDREQ0-A	ET_TX_EN/ RMII_TXD_EN		MTIOC3B-B		TRDATA0
M11		PC2	A18-A	ET_RX_DV		MTCLKE-A	SSLA3-A/ RxD5	
M12		PC1	A17-A	ET_ERXD2		MTCLKH-A	SSLA2-A/ SCK5	
M13	VSS							
N1		P21			USB0_EXICEN	MTIOC1B/ TMCI0-B/ PO1	SCL1/RxD0	
N2		P16			USB0_VBUS/ USB0_OVRCURB/ USB0_VBUSEN-B	MTIOC3C-A/ TMO2/ PO14	RxD3-A	IRQ6-B
N3	PLLVSS							
N4		P13				TMO3	SDA0/ TxD2-A	IRQ3-B/ ADTRG1#
N5					USB0_DM			
N6					USB0_DP			
N7		P54	EDACK0-C	ET_LINKSTA		MTIOC4B-B		TRDATA2
N8		P51	WR1#/BC1#/ WAIT#-D				SSLB2-A/ SCK2	
N9	VCC							
N10		PC5	A21/CS2#-C/ WAIT#-C	ET_ETXD2		MTIC11W-A/ MTCLKD-B	RSPCKA-A	
N11		PC4	A20/CS3#-C	ET_TX_CLK		MTCLKC-B	SSLA0-A	
N12		P76	CS6#-B	ET_RX_CLK/ REF50CK				
N13		P74	CS4#-B	ET_ERXD1/ RMII_RXD1				

Table 1.6 List of Pins and Pin Functions (144-Pin LQFP) (5 / 5)

Pin No. 144-Pin LQFP	Power Supply Clock System Control	I/O Port	External Bus EXDMAC	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE, WDT)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
112		P64	CS4#-A/ WE#					
113		P63	CS3#-A/ CAS#					
114		P62	CS2#-A/ RAS#					
115		P61	CS1#-A/ SDCS#					
116	VSS							
117		P60	CS0#-A					
118	VCC							
119		PD7	D7			MTIC5U/ POE0#		
120		PD6	D6			MTIC5V/ POE1#		
121		PD5	D5			MTIC5W/ POE2#		
122		PD4	D4			MTIC11U-B/ POE3#		
123		PD3	D3			MTIC11V-B/ POE4#		
124		PD2	D2			MTIC11W-B/ POE5#		
125		PD1	D1			POE6#		
126		PD0	D0			POE7#		
127		P93	A19-B					
128		P92	A18-B					
129		P91	A17-B					
130	VSS							
131		P90	A16-B					
132	VCC							
133		P47						IRQ15-B/AN7
134		P46						IRQ14/AN6
135		P45						IRQ13-B/AN5
136		P44						IRQ12/AN4
137		P43						IRQ11-B/AN3
138		P42						IRQ10-B/AN2
139		P41						IRQ9-B/AN1
140	VREFL							
141		P40						IRQ8-B/AN0
142	VREFH							
143	AVCC							
144		P07						IRQ15-A/ ADTRG0#-A

Table 1.9 Pin Functions (5 / 7)

Classifications	Pin Name	I/O	Description
Ethernet controller	REF50CK	Input	50-MHz reference clock. This pin inputs reference signals for transmission/reception timings in RMII mode.
	RMII_CRS_DV	Input	Indicates that there are carrier detection signals and valid receive data on RMII_RXD1 and RMII_RXD0 in RMII mode.
	RMII_TXD0, RMII_TXD1	Output	2-bit transmit data in RMII mode.
	RMII_RXD0, RMII_RXD1	Input	2-bit receive data in RMII mode.
	RMII_TXD_EN	Output	Output pin for data transmit enable signals in RMII mode.
	RMII_RX_ER	Input	Indicates an error has occurred during reception of data in RMII mode.
	ET_CRS	Input	Carrier detection/data reception enable pin.
	ET_RX_DV	Input	Indicates that there are valid receive data on ET_ERXD3 to ET_ERXD0.
	ET_EXOUT	Output	General-purpose external output pin.
	ET_LINKSTA	Input	Inputs link status from the PHY-LSI.
	ET_ETXD0 to ET_ETXD3	Output	4 bits of MII transmit data.
	ET_ERXD0 to ET_ERXD3	Input	4 bits of MII receive data.
	ET_TX_EN	Output	Transmit enable pin. Indicates that transmit data is ready on ET_ETXD3 to ET_ETXD0.
	ET_TX_ER	Output	Transmit error pin. Notifies the PHY_LSI of an error during transmission.
	ET_RX_ER	Input	Receive error pin. Recognizes an error during reception.
	ET_TX_CLK	Input	Transmit clock pin. This pin inputs reference signals for output timings from ET_TX_EN, ET_ETXD3 to ET_ETXD0, and ET_TX_ER.
	ET_RX_CLK	Input	Receive clock pin. This pin inputs reference signals for input timings to ET_RX_DV, ET_ERXD3 to ET_ERXD0, and ET_RX_ER.
	ET_COL	Input	Inputs collision detection signals.
	ET_WOL	Output	Receives Magic Packets™
	ET_MDC	Output	Outputs reference clock signals for information transfer via ET_MDIO.
	ET_MDIO	I/O	These pins carry bidirectional signals for the exchange of management information between the RX62N Group and the PHY-LSI.

2. CPU

The RX CPU has sixteen general-purpose registers, nine control registers, and one accumulator used for DSP instructions.

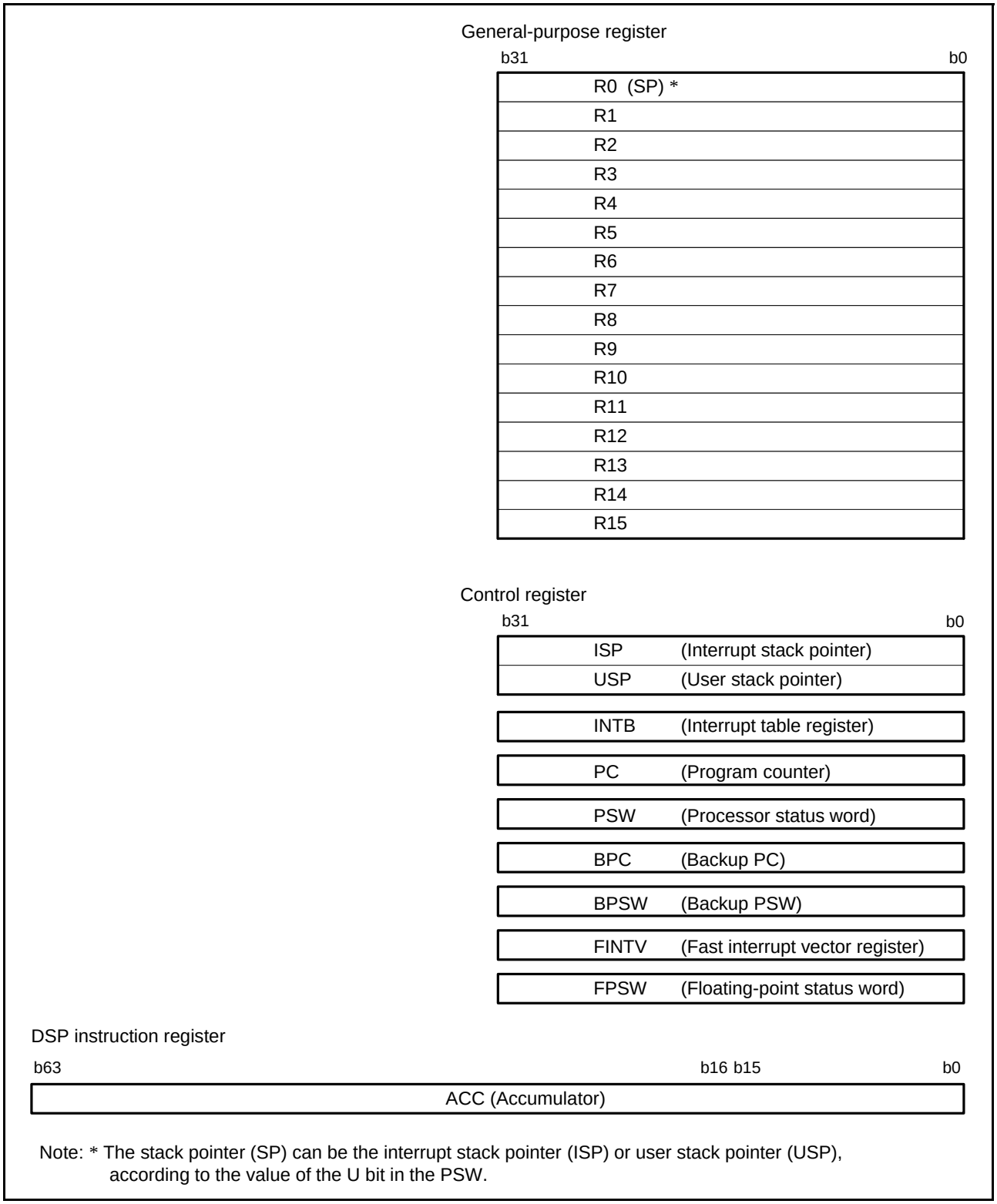

Figure 2.1 Register Set of the CPU

Table 4.1 List of I/O Registers (Address Order) (6 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 7044h	ICU	Interrupt request register 068	IR068	8	8	2 ICLK
0008 7045h	ICU	Interrupt request register 069	IR069	8	8	2 ICLK
0008 7046h	ICU	Interrupt request register 070	IR070	8	8	2 ICLK
0008 7047h	ICU	Interrupt request register 071	IR071	8	8	2 ICLK
0008 7048h	ICU	Interrupt request register 072	IR072	8	8	2 ICLK
0008 7049h	ICU	Interrupt request register 073	IR073	8	8	2 ICLK
0008 704Ah	ICU	Interrupt request register 074	IR074	8	8	2 ICLK
0008 704Bh	ICU	Interrupt request register 075	IR075	8	8	2 ICLK
0008 704Ch	ICU	Interrupt request register 076	IR076	8	8	2 ICLK
0008 704Dh	ICU	Interrupt request register 077	IR077	8	8	2 ICLK
0008 704Eh	ICU	Interrupt request register 078	IR078	8	8	2 ICLK
0008 704Fh	ICU	Interrupt request register 079	IR079	8	8	2 ICLK
0008 705Ah	ICU	Interrupt request register 090	IR090	8	8	2 ICLK
0008 705Bh	ICU	Interrupt request register 091	IR091	8	8	2 ICLK
0008 705Ch	ICU	Interrupt request register 092	IR092	8	8	2 ICLK
0008 7060h	ICU	Interrupt request register 096	IR096	8	8	2 ICLK
0008 7062h	ICU	Interrupt request register 098	IR098	8	8	2 ICLK
0008 7063h	ICU	Interrupt request register 099	IR099	8	8	2 ICLK
0008 7066h	ICU	Interrupt request register 102	IR102	8	8	2 ICLK
0008 7072h	ICU	Interrupt request register 114	IR114	8	8	2 ICLK
0008 7073h	ICU	Interrupt request register 115	IR115	8	8	2 ICLK
0008 7074h	ICU	Interrupt request register 116	IR116	8	8	2 ICLK
0008 7075h	ICU	Interrupt request register 117	IR117	8	8	2 ICLK
0008 7076h	ICU	Interrupt request register 118	IR118	8	8	2 ICLK
0008 7077h	ICU	Interrupt request register 119	IR119	8	8	2 ICLK
0008 7078h	ICU	Interrupt request register 120	IR120	8	8	2 ICLK
0008 7079h	ICU	Interrupt request register 121	IR121	8	8	2 ICLK
0008 707Ah	ICU	Interrupt request register 122	IR122	8	8	2 ICLK
0008 707Bh	ICU	Interrupt request register 123	IR123	8	8	2 ICLK
0008 707Ch	ICU	Interrupt request register 124	IR124	8	8	2 ICLK
0008 707Dh	ICU	Interrupt request register 125	IR125	8	8	2 ICLK
0008 707Eh	ICU	Interrupt request register 126	IR126	8	8	2 ICLK
0008 707Fh	ICU	Interrupt request register 127	IR127	8	8	2 ICLK
0008 7080h	ICU	Interrupt request register 128	IR128	8	8	2 ICLK
0008 7081h	ICU	Interrupt request register 129	IR129	8	8	2 ICLK
0008 7082h	ICU	Interrupt request register 130	IR130	8	8	2 ICLK
0008 7083h	ICU	Interrupt request register 131	IR131	8	8	2 ICLK
0008 7084h	ICU	Interrupt request register 132	IR132	8	8	2 ICLK
0008 7085h	ICU	Interrupt request register 133	IR133	8	8	2 ICLK
0008 7086h	ICU	Interrupt request register 134	IR134	8	8	2 ICLK
0008 7087h	ICU	Interrupt request register 135	IR135	8	8	2 ICLK
0008 7088h	ICU	Interrupt request register 136	IR136	8	8	2 ICLK
0008 7089h	ICU	Interrupt request register 137	IR137	8	8	2 ICLK
0008 708Ah	ICU	Interrupt request register 138	IR138	8	8	2 ICLK
0008 708Bh	ICU	Interrupt request register 139	IR139	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (13 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 735Ch	ICU	Interrupt source priority register 5C	IPR5C	8	8	2 ICLK
0008 735Dh	ICU	Interrupt source priority register 5D	IPR5D	8	8	2 ICLK
0008 735Eh	ICU	Interrupt source priority register 5E	IPR5E	8	8	2 ICLK
0008 735Fh	ICU	Interrupt source priority register 5F	IPR5F	8	8	2 ICLK
0008 7360h	ICU	Interrupt source priority register 60	IPR60	8	8	2 ICLK
0008 7361h	ICU	Interrupt source priority register 61	IPR61	8	8	2 ICLK
0008 7362h	ICU	Interrupt source priority register 62	IPR62	8	8	2 ICLK
0008 7363h	ICU	Interrupt source priority register 63	IPR63	8	8	2 ICLK
0008 7364h	ICU	Interrupt source priority register 64	IPR64	8	8	2 ICLK
0008 7365h	ICU	Interrupt source priority register 65	IPR65	8	8	2 ICLK
0008 7366h	ICU	Interrupt source priority register 66	IPR66	8	8	2 ICLK
0008 7367h	ICU	Interrupt source priority register 67	IPR67	8	8	2 ICLK
0008 7368h	ICU	Interrupt source priority register 68	IPR68	8	8	2 ICLK
0008 7369h	ICU	Interrupt source priority register 69	IPR69	8	8	2 ICLK
0008 736Ah	ICU	Interrupt source priority register 6A	IPR6A	8	8	2 ICLK
0008 736Bh	ICU	Interrupt source priority register 6B	IPR6B	8	8	2 ICLK
0008 7370h	ICU	Interrupt source priority register 70	IPR70	8	8	2 ICLK
0008 7371h	ICU	Interrupt source priority register 71	IPR71	8	8	2 ICLK
0008 7372h	ICU	Interrupt source priority register 72	IPR72	8	8	2 ICLK
0008 7373h	ICU	Interrupt source priority register 73	IPR73	8	8	2 ICLK
0008 7374h	ICU	Interrupt source priority register 74	IPR74	8	8	2 ICLK
0008 7375h	ICU	Interrupt source priority register 75	IPR75	8	8	2 ICLK
0008 7380h	ICU	Interrupt source priority register 80	IPR80	8	8	2 ICLK
0008 7381h	ICU	Interrupt source priority register 81	IPR81	8	8	2 ICLK
0008 7382h	ICU	Interrupt source priority register 82	IPR82	8	8	2 ICLK
0008 7383h	ICU	Interrupt source priority register 83	IPR83	8	8	2 ICLK
0008 7385h	ICU	Interrupt source priority register 85	IPR85	8	8	2 ICLK
0008 7386h	ICU	Interrupt source priority register 86	IPR86	8	8	2 ICLK
0008 7388h	ICU	Interrupt source priority register 88	IPR88	8	8	2 ICLK
0008 7389h	ICU	Interrupt source priority register 89	IPR89	8	8	2 ICLK
0008 738Ah	ICU	Interrupt source priority register 8A	IPR8A	8	8	2 ICLK
0008 738Bh	ICU	Interrupt source priority register 8B	IPR8B	8	8	2 ICLK
0008 738Ch	ICU	Interrupt source priority register 8C	IPR8C	8	8	2 ICLK
0008 738Dh	ICU	Interrupt source priority register 8D	IPR8D	8	8	2 ICLK
0008 738Eh	ICU	Interrupt source priority register 8E	IPR8E	8	8	2 ICLK
0008 738Fh	ICU	Interrupt source priority register 8F	IPR8F	8	8	2 ICLK
0008 7400h	ICU	DMACA activation source select register 0	DMRSR0	8	8	2 ICLK
0008 7404h	ICU	DMACA activation source select register 1	DMRSR1	8	8	2 ICLK
0008 7408h	ICU	DMACA activation source select register 2	DMRSR2	8	8	2 ICLK
0008 740Ch	ICU	DMACA activation source select register 3	DMRSR3	8	8	2 ICLK
0008 7500h	ICU	IRQ control register 0	IRQCR0	8	8	2 ICLK
0008 7501h	ICU	IRQ control register 1	IRQCR1	8	8	2 ICLK
0008 7502h	ICU	IRQ control register 2	IRQCR2	8	8	2 ICLK
0008 7503h	ICU	IRQ control register 3	IRQCR3	8	8	2 ICLK
0008 7504h	ICU	IRQ control register 4	IRQCR4	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (14 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 7505h	ICU	IRQ control register 5	IRQCR5	8	8	2 ICLK
0008 7506h	ICU	IRQ control register 6	IRQCR6	8	8	2 ICLK
0008 7507h	ICU	IRQ control register 7	IRQCR7	8	8	2 ICLK
0008 7508h	ICU	IRQ control register 8	IRQCR8	8	8	2 ICLK
0008 7509h	ICU	IRQ control register 9	IRQCR9	8	8	2 ICLK
0008 750Ah	ICU	IRQ control register 10	IRQCR10	8	8	2 ICLK
0008 750Bh	ICU	IRQ control register 11	IRQCR11	8	8	2 ICLK
0008 750Ch	ICU	IRQ control register 12	IRQCR12	8	8	2 ICLK
0008 750Dh	ICU	IRQ control register 13	IRQCR13	8	8	2 ICLK
0008 750Eh	ICU	IRQ control register 14	IRQCR14	8	8	2 ICLK
0008 750Fh	ICU	IRQ control register 15	IRQCR15	8	8	2 ICLK
0008 7580h	ICU	Non-maskable interrupt status register	NMISR	8	8	2 ICLK
0008 7581h	ICU	Non-maskable interrupt enable register	NMIER	8	8	2 ICLK
0008 7582h	ICU	Non-maskable interrupt clear register	NMICLR	8	8	2 ICLK
0008 7583h	ICU	NMI pin interrupt control register	NMICR	8	8	2 ICLK
0008 8000h	CMT	Compare match timer start register 0	CMSTR0	16	16	2 to 3 PCLK*8
0008 8002h	CMT0	Compare match timer control register	CMCR	16	16	2 to 3 PCLK*8
0008 8004h	CMT0	Compare match timer counter	CMCNT	16	16	2 to 3 PCLK*8
0008 8006h	CMT0	Compare match timer constant register	CMCOR	16	16	2 to 3 PCLK*8
0008 8008h	CMT1	Compare match timer control register	CMCR	16	16	2 to 3 PCLK*8
0008 800Ah	CMT1	Compare match timer counter	CMCNT	16	16	2 to 3 PCLK*8
0008 800Ch	CMT1	Compare match timer constant register	CMCOR	16	16	2 to 3 PCLK*8
0008 8010h	CMT	Compare match timer start register 1	CMSTR1	16	16	2 to 3 PCLK*8
0008 8012h	CMT2	Compare match timer control register	CMCR	16	16	2 to 3 PCLK*8
0008 8014h	CMT2	Compare match timer counter	CMCNT	16	16	2 to 3 PCLK*8
0008 8016h	CMT2	Compare match timer constant register	CMCOR	16	16	2 to 3 PCLK*8
0008 8018h	CMT3	Compare match timer control register	CMCR	16	16	2 to 3 PCLK*8
0008 801Ah	CMT3	Compare match timer counter	CMCNT	16	16	2 to 3 PCLK*8
0008 801Ch	CMT3	Compare match timer constant register	CMCOR	16	16	2 to 3 PCLK*8
0008 8028h	WDT	Timer control/status register	READ.TCSR	8	8	2 to 3 PCLK*8
0008 8028h	WDT	Write window A register	WRITE.WINA	16	16	2 to 3 PCLK*8
0008 8029h	WDT	Timer counter	READ.TCNT	8	8	2 to 3 PCLK*8
0008 802Ah	WDT	Write window B register	WRITE.WINB	16	16	2 to 3 PCLK*8
0008 802Bh	WDT	Reset control/status register	READ.RSTCSR	8	8	2 to 3 PCLK*8
0008 8030h	IWDT	IWDT refresh register	IWDTRR	8	8	2 to 3 PCLK*8
0008 8032h	IWDT	IWDT control register	IWDTCR	16	16	2 to 3 PCLK*8
0008 8034h	IWDT	IWDT status register	IWDTSR	16	16	2 to 3 PCLK*8
0008 8040h	AD0	A/D data register A	ADDRA	16	16	2 to 3 PCLK*8
0008 8042h	AD0	A/D data register B	ADDRB	16	16	2 to 3 PCLK*8
0008 8044h	AD0	A/D data register C	ADDRC	16	16	2 to 3 PCLK*8
0008 8046h	AD0	A/D data register D	ADDRD	16	16	2 to 3 PCLK*8
0008 8050h	AD0	A/D control/status register	ADCSR	8	8	2 to 3 PCLK*8
0008 8051h	AD0	A/D control register	ADCR	8	8	2 to 3 PCLK*8
0008 8052h	AD0	ADDRn format select register	ADDPR	8	8	2 to 3 PCLK*8

Table 4.1 List of I/O Registers (Address Order) (17 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 824Fh	SCI1	Serial extended mode register	SEMR	8	8	2 to 3 PCLK*8
0008 8248h	SMCI1	Serial mode register	SMR	8	8	2 to 3 PCLK*8
0008 8249h	SMCI1	Bit rate register	BRR	8	8	2 to 3 PCLK*8
0008 824Ah	SMCI1	Serial control register	SCR	8	8	2 to 3 PCLK*8
0008 824Bh	SMCI1	Transmit data register	TDR	8	8	2 to 3 PCLK*8
0008 824Ch	SMCI1	Serial status register	SSR	8	8	2 to 3 PCLK*8
0008 824Dh	SMCI1	Receive data register	RDR	8	8	2 to 3 PCLK*8
0008 824Eh	SMCI1	Smart card mode register	SCMR	8	8	2 to 3 PCLK*8
0008 8250h	SCI2	Serial mode register	SMR	8	8	2 to 3 PCLK*8
0008 8251h	SCI2	Bit rate register	BRR	8	8	2 to 3 PCLK*8
0008 8252h	SCI2	Serial control register	SCR	8	8	2 to 3 PCLK*8
0008 8253h	SCI2	Transmit data register	TDR	8	8	2 to 3 PCLK*8
0008 8254h	SCI2	Serial status register	SSR	8	8	2 to 3 PCLK*8
0008 8255h	SCI2	Receive data register	RDR	8	8	2 to 3 PCLK*8
0008 8256h	SCI2	Smart card mode register	SCMR	8	8	2 to 3 PCLK*8
0008 8257h	SCI2	Serial extended mode register	SEMR	8	8	2 to 3 PCLK*8
0008 8250h	SMCI2	Serial mode register	SMR	8	8	2 to 3 PCLK*8
0008 8251h	SMCI2	Bit rate register	BRR	8	8	2 to 3 PCLK*8
0008 8252h	SMCI2	Serial control register	SCR	8	8	2 to 3 PCLK*8
0008 8253h	SMCI2	Transmit data register	TDR	8	8	2 to 3 PCLK*8
0008 8254h	SMCI2	Serial status register	SSR	8	8	2 to 3 PCLK*8
0008 8255h	SMCI2	Receive data register	RDR	8	8	2 to 3 PCLK*8
0008 8256h	SMCI2	Smart card mode register	SCMR	8	8	2 to 3 PCLK*8
0008 8258h	SCI3	Serial mode register	SMR	8	8	2 to 3 PCLK*8
0008 8259h	SCI3	Bit rate register	BRR	8	8	2 to 3 PCLK*8
0008 825Ah	SCI3	Serial control register	SCR	8	8	2 to 3 PCLK*8
0008 825Bh	SCI3	Transmit data register	TDR	8	8	2 to 3 PCLK*8
0008 825Ch	SCI3	Serial status register	SSR	8	8	2 to 3 PCLK*8
0008 825Dh	SCI3	Receive data register	RDR	8	8	2 to 3 PCLK*8
0008 825Eh	SCI3	Smart card mode register	SCMR	8	8	2 to 3 PCLK*8
0008 825Fh	SCI3	Serial extended mode register	SEMR	8	8	2 to 3 PCLK*8
0008 8258h	SMCI3	Serial mode register	SMR	8	8	2 to 3 PCLK*8
0008 8259h	SMCI3	Bit rate register	BRR	8	8	2 to 3 PCLK*8
0008 825Ah	SMCI3	Serial control register	SCR	8	8	2 to 3 PCLK*8
0008 825Bh	SMCI3	Transmit data register	TDR	8	8	2 to 3 PCLK*8
0008 825Ch	SMCI3	Serial status register	SSR	8	8	2 to 3 PCLK*8
0008 825Dh	SMCI3	SMCI3 Receive data register	RDR	8	8	2 to 3 PCLK*8
0008 825Eh	SMCI3	SMCI3 Smart card mode register	SCMR	8	8	2 to 3 PCLK*8
0008 8268h	SCI5	Serial mode register	SMR	8	8	2 to 3 PCLK*8
0008 8269h	SCI5	Bit rate register	BRR	8	8	2 to 3 PCLK*8
0008 826Ah	SCI5	Serial control register	SCR	8	8	2 to 3 PCLK*8
0008 826Bh	SCI5	Transmit data register	TDR	8	8	2 to 3 PCLK*8
0008 826Ch	SCI5	Serial status register	SSR	8	8	2 to 3 PCLK*8
0008 826Dh	SCI5	Receive data register	RDR	8	8	2 to 3 PCLK*8
0008 826Eh	SCI5	Smart card mode register	SCMR	8	8	2 to 3 PCLK*8

Table 4.1 List of I/O Registers (Address Order) (19 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 8310h	RIIC0	I²C bus bit rate low-level register	ICBRL	8	8	2 to 3 PCLK*8
0008 8311h	RIIC0	I²C bus bit rate high-level register	ICBRH	8	8	2 to 3 PCLK*8
0008 8312h	RIIC0	I²C bus transmit data register	ICDRT	8	8	2 to 3 PCLK*8
0008 8313h	RIIC0	I²C bus receive data register	ICDRR	8	8	2 to 3 PCLK*8
0008 8320h	RIIC1	I²C bus control register 1	ICCR1	8	8	2 to 3 PCLK*8
0008 8321h	RIIC1	I²C bus control register 2	ICCR2	8	8	2 to 3 PCLK*8
0008 8322h	RIIC1	I²C bus mode register 1	ICMR1	8	8	2 to 3 PCLK*8
0008 8323h	RIIC1	I²C bus mode register 2	ICMR2	8	8	2 to 3 PCLK*8
0008 8324h	RIIC1	I²C bus mode register 3	ICMR3	8	8	2 to 3 PCLK*8
0008 8325h	RIIC1	I²C bus function enable register	ICFER	8	8	2 to 3 PCLK*8
0008 8326h	RIIC1	I²C bus status enable register	ICSER	8	8	2 to 3 PCLK*8
0008 8327h	RIIC1	I²C bus interrupt enable register	ICIER	8	8	2 to 3 PCLK*8
0008 8328h	RIIC1	I²C bus status register 1	ICSR1	8	8	2 to 3 PCLK*8
0008 8329h	RIIC1	I²C bus status register 2	ICSR2	8	8	2 to 3 PCLK*8
0008 832Ah	RIIC1	Slave address register L0	SARL0	8	8	2 to 3 PCLK*8
0008 832Ah	RIIC1	Timeout internal counter	TMOCNT	16	16	2 to 3 PCLK*8
0008 832Ah	RIIC1	Timeout internal counter L	TMOCNTL	8	8	2 to 3 PCLK*8
0008 832Bh	RIIC1	Slave address register U0	SARU0	8	8	2 to 3 PCLK*8
0008 832Bh	RIIC1	Timeout internal counter U	TMOCNTU		8	2 to 3 PCLK*8
0008 832Ch	RIIC1	Slave address register L1	SARL1	8	8	2 to 3 PCLK*8
0008 832Dh	RIIC1	Slave address register U1	SARU1	8	8	2 to 3 PCLK*8
0008 832Eh	RIIC1	Slave address register L2	SARL2	8	8	2 to 3 PCLK*8
0008 832Fh	RIIC1	Slave address register U2	SARU2	8	8	2 to 3 PCLK*8
0008 8330h	RIIC1	I²C bus bit rate low-level register	ICBRL	8	8	2 to 3 PCLK*8
0008 8331h	RIIC1	I²C bus bit rate high-level register	ICBRH	8	8	2 to 3 PCLK*8
0008 8332h	RIIC1	I²C bus transmit data register	ICDRT	8	8	2 to 3 PCLK*8
0008 8333h	RIIC1	I²C bus receive data register	ICDRR	8	8	2 to 3 PCLK*8
0008 8380h	RSPI0	RSPI control register	SPCR	8	8	2 to 3 PCLK*8
0008 8381h	RSPI0	RSPI slave select polarity register	SSLP	8	8	2 to 3 PCLK*8
0008 8382h	RSPI0	RSPI pin control register	SPPCR	8	8	2 to 3 PCLK*8
0008 8383h	RSPI0	RSPI status register	SPSR	8	8	2 to 3 PCLK*8
0008 8384h	RSPI0	RSPI data register	SPDR	32	16, 32	2 to 3 PCLK*8
0008 8388h	RSPI0	RSPI sequence control register	SPSCR	8	8	2 to 3 PCLK*8
0008 8389h	RSPI0	RSPI sequence status register	SPSSR	8	8	2 to 3 PCLK*8
0008 838Ah	RSPI0	RSPI bit rate register	SPBR	8	8	2 to 3 PCLK*8
0008 838Bh	RSPI0	RSPI data control register	SPDCR	8	8	2 to 3 PCLK*8
0008 838Ch	RSPI0	RSPI clock delay register	SPCKD	8	8	2 to 3 PCLK*8
0008 838Dh	RSPI0	RSPI slave select negation delay register	SSLND	8	8	2 to 3 PCLK*8
0008 838Eh	RSPI0	RSPI next-access delay register	SPND	8	8	2 to 3 PCLK*8
0008 838Fh	RSPI0	RSPI control register 2	SPCR2	8	8	2 to 3 PCLK*8
0008 8390h	RSPI0	RSPI command register 0	SPCMD0	16	16	2 to 3 PCLK*8
0008 8392h	RSPI0	RSPI command register 1	SPCMD1	16	16	2 to 3 PCLK*8
0008 8394h	RSPI0	RSPI command register 2	SPCMD2	16	16	2 to 3 PCLK*8
0008 8396h	RSPI0	RSPI command register 3	SPCMD3	16	16	2 to 3 PCLK*8
0008 8398h	RSPI0	RSPI command register 4	SPCMD4	16	16	2 to 3 PCLK*8

Table 4.1 List of I/O Registers (Address Order) (33 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000A 0254h	USB1	USB request type register	USBREQ	16	16	at least 9 PCLK*9
000A 0256h	USB1	USB request value register	USBVAL	16	16	at least 9 PCLK*9
000A 0258h	USB1	USB request index register	USBINDX	16	16	at least 9 PCLK*9
000A 025Ah	USB1	USB request length register	USBLENG	16	16	at least 9 PCLK*9
000A 025Ch	USB1	DCP configuration register	DCPCFG	16	16	at least 9 PCLK*9
000A 025Eh	USB1	DCP maximum packet size register	DCPMAXP	16	16	at least 9 PCLK*9
000A 0260h	USB1	DCP control register	DCPCTR	16	16	at least 9 PCLK*9
000A 0264h	USB1	Pipe window select register	PIPESEL	16	16	at least 9 PCLK*9
000A 0268h	USB1	Pipe configuration register	PIPECFG	16	16	at least 9 PCLK*9
000A 026Ch	USB1	Pipe maximum packet size register	PIPEMAXP	16	16	at least 9 PCLK*9
000A 026Eh	USB1	Pipe cycle control register	PIPEPERI	16	16	at least 9 PCLK*9
000A 0270h	USB1	Pipe 1 control register	PIPE1CTR	16	16	at least 9 PCLK*9
000A 0272h	USB1	Pipe 2 control register	PIPE2CTR	16	16	at least 9 PCLK*9
000A 0274h	USB1	Pipe 3 control register	PIPE3CTR	16	16	at least 9 PCLK*9
000A 0276h	USB1	Pipe 4 control register	PIPE4CTR	16	16	at least 9 PCLK*9
000A 0278h	USB1	Pipe 5 control register	PIPE5CTR	16	16	at least 9 PCLK*9
000A 027Ah	USB1	Pipe 6 control register	PIPE6CTR	16	16	at least 9 PCLK*9
000A 027Ch	USB1	Pipe 7 control register	PIPE7CTR	16	16	at least 9 PCLK*9
000A 027Eh	USB1	Pipe 8 control register	PIPE8CTR	16	16	at least 9 PCLK*9
000A 0280h	USB1	Pipe 9 control register	PIPE9CTR	16	16	at least 9 PCLK*9
000A 0290h	USB1	Pipe 1 transaction counter enable register	PIPE1TRE	16	16	at least 9 PCLK*9
000A 0292h	USB1	Pipe 1 transaction counter register	PIPE1TRN	16	16	at least 9 PCLK*9
000A 0294h	USB1	Pipe 2 transaction counter enable register	PIPE2TRE	16	16	at least 9 PCLK*9
000A 0296h	USB1	Pipe 2 transaction counter register	PIPE2TRN	16	16	at least 9 PCLK*9
000A 0298h	USB1	Pipe 3 transaction counter enable register	PIPE3TRE	16	16	at least 9 PCLK*9
000A 029Ah	USB1	Pipe 3 transaction counter register	PIPE3TRN	16	16	at least 9 PCLK*9

Table 5.17 Timing of On-Chip Peripheral Modules (8)

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
ICLK = 12.5 to 100 MHz
T_a = -40 to +85°C

Item		Symbol	Min.	Max.	Unit	Test Conditions
ETHERC(RMII)	REF50CK cycle time	T_{ck}	20	—	ns	Figure 5.44 to Figure 5.47
	REF50CK frequency Typ. 50 MHz	—	—	50 + 100ppm	MHz	
	REF50CK duty	—	35	65	%	
	REF50CK rise/fall time	$T_{ckr/ckf}$	0.5	3.5	ns	
	RMII_xxxx*1 output delay time	T_{co}	2.5	12.5	ns	
	RMII_xxxx*2 setup time	T_{su}	3	—	ns	
	RMII_xxxx*2 hold time	T_{hd}	1	—	ns	
	RMII_xxxx*1*2 rise/fall time	Tr/Tf	0.5	6	ns	
	ET_MDIO setup time	t_{MDIOs}	10	—	ns	Figure 5.48
	ET_MDIO hold time	t_{MDIOh}	10	—	ns	
	ET_MDIO output hold time*3	t_{MDIODh}	5	—	ns	Figure 5.49
	ET_WOL output delay time	t_{WOLd}	1	20	ns	Figure 5.50

Note 1. RMII_TXD_EN, RMII_TXD1, RMII_TXD0
Note 2. RMII_CRS_DV, RMII_RXD1, RMII_RXD0, RMII_RX_ER
Note 3. The user program must make settings so that this stipulation is satisfied.

Table 5.17 Timing of On-Chip Peripheral Modules (9)

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
ICLK = 12.5 to 100 MHz
T_a = -40 to +85°C

Item		Symbol	Min.	Max.	Unit	Test Conditions
ETHERC(MII)	ET_TX_CLK cycle time	t_{Tcyc}	40	—	ns	—
	ET_TX_EN output delay time	t_{TENd}	1	20	ns	Figure 5.51
	ET_ETXD0 to ET_ETXD3 output delay time	t_{MTDd}	1	20	ns	
	ET_CRS setup time	t_{CRSs}	10	—	ns	
	ET_CRS hold time	t_{CRSh}	10	—	ns	
	ET_COL setup time	t_{COLs}	10	—	ns	Figure 5.52
	ET_COL hold time	t_{COLh}	10	—	ns	
	ET_RX_CLK cycle time	t_{TRcyc}	40	—	ns	—
	ET_RX_DV setup time	t_{RDVs}	10		ns	Figure 5.53
	ET_RX_DV hold time	t_{RDVh}	10	—	ns	
	ET_ERXD0 to ET_ERXD3 setup time	t_{MRDs}	10	—	ns	
	ET_ERXD0 to ET_ERXD3 hold time	t_{MRDh}	10	—	ns	
	ET_RX_ER setup time	t_{RERs}	10	—	ns	Figure 5.54
	ET_RX_ER hold time	t_{RESh}	10	—	ns	
	ET_MDIO setup time	t_{MDIOs}	10	—	ns	Figure 5.55
	ET_MDIO hold time	t_{MDIOh}	10	—	ns	
	ET_MDIO utput hold time	t_{MDIOdh}	5	—	ns	Figure 5.56
	ET_WOL output delay time	t_{WOLd}	1	20	ns	Figure 5.57

Note 1. RMII_TXD_EN, RMII_TXD1, RMII_TXD0
Note 2. RMII_CRS_DV, RMII_RXD1, RMII_RXD0, RMII_RX_ER
Note 3. The user program must make settings so that this stipulation is satisfied.

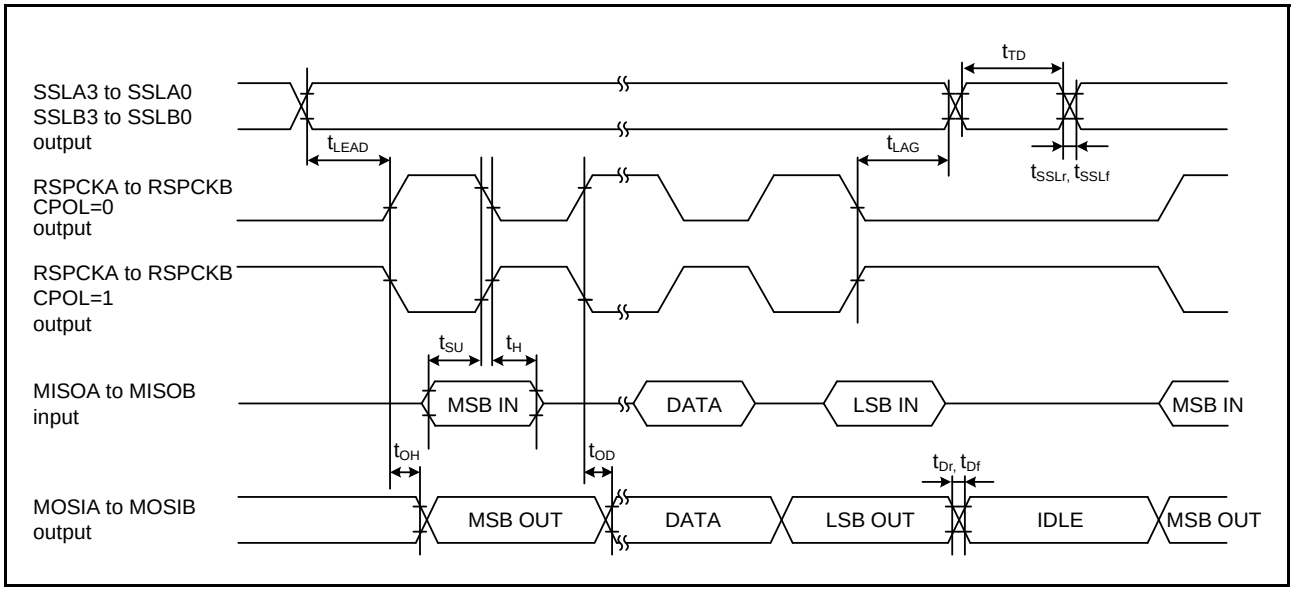

Figure 5.40 RSPI Timing (Master, CPHA = 1)

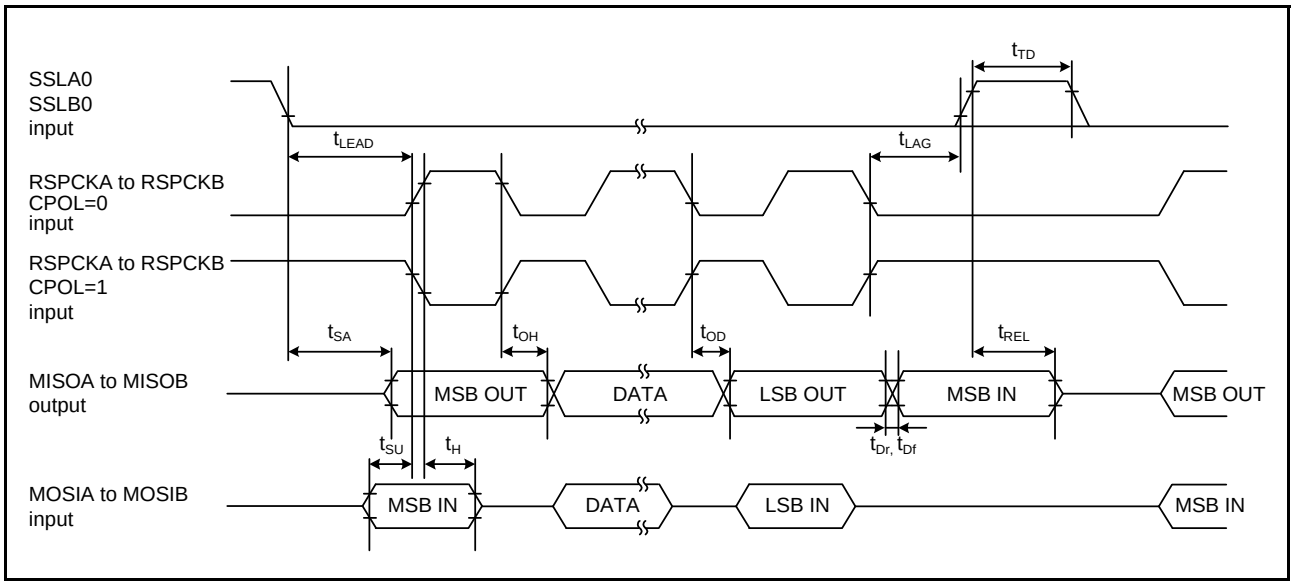

Figure 5.41 RSPI Timing (Slave, CPHA = 0)

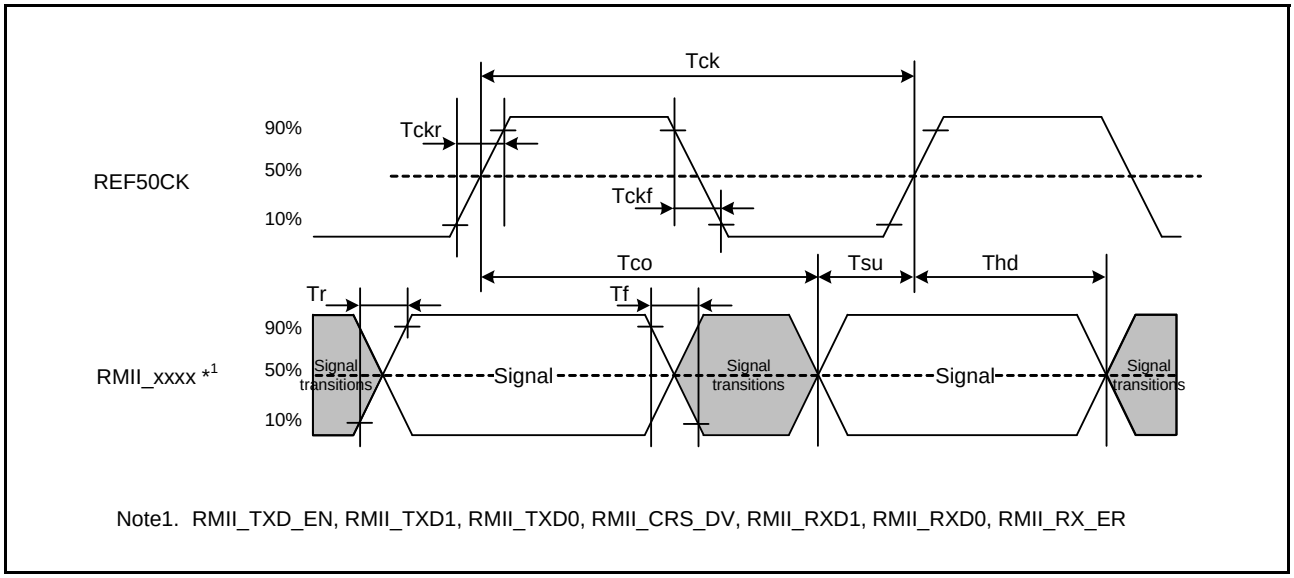

Figure 5.44 REF50CK and RMII Signal Timing

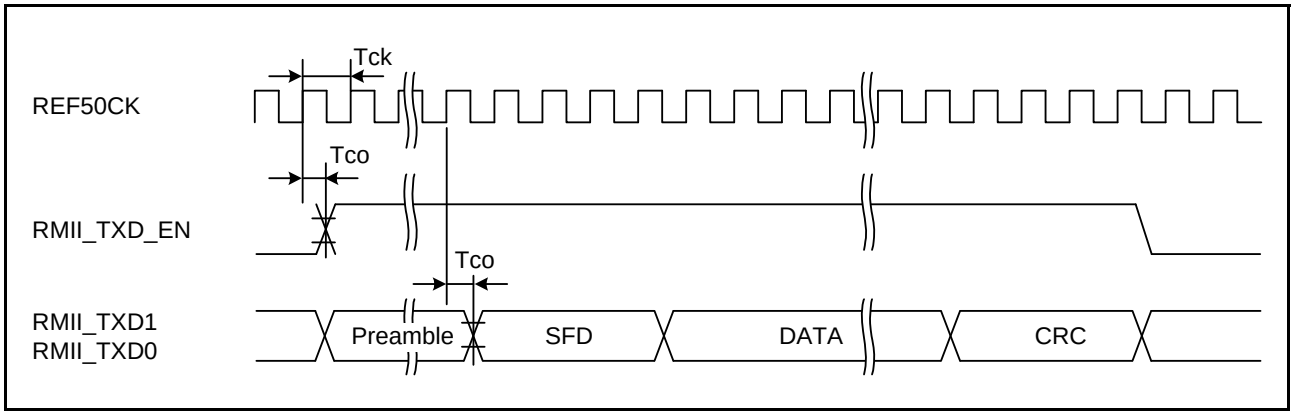

Figure 5.45 RMII Transmission Timing

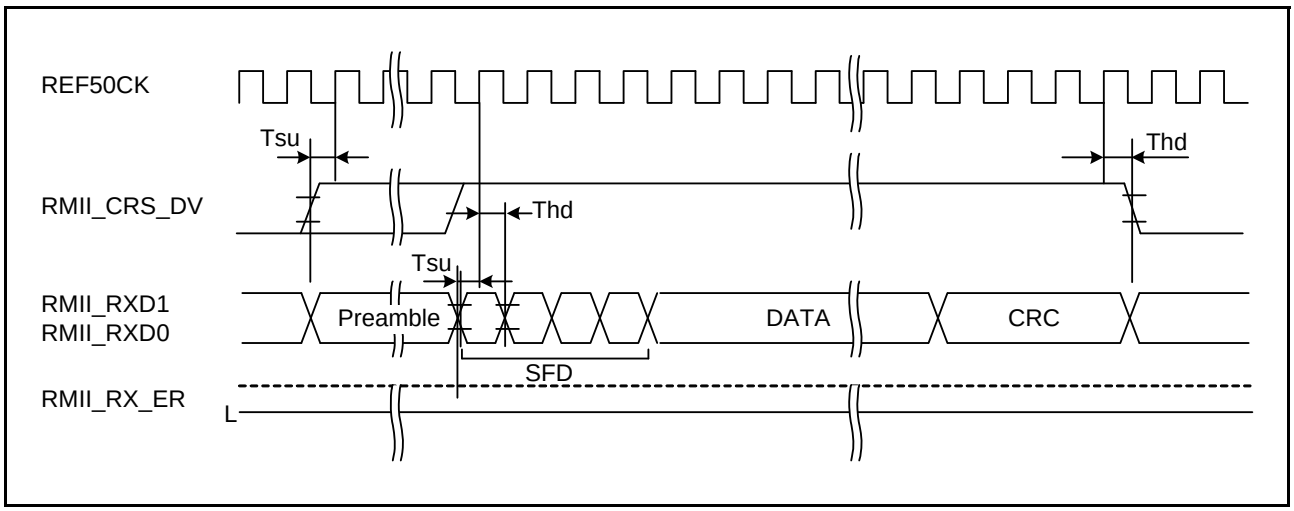

Figure 5.46 RMII Reception Timing (Normal Operation)

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.40	Jul 16, 2014	4. I/O Registers		
		69, 70	Table 5.1 List of I/O Registers (Address Order), changed	TN-RX*-A012A/E
		5. Electrical Characteristics		
		91	Table 5.4 DC Characteristics (3), Note 1, changed	
		101 to 104	Figure 5.10 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized) to Figure 5.14 External Bus Timing/External Wait Control, changed	
		114	Table 5.13 Timing of On-Chip Peripheral Modules (2): SCI changed	
		140	Table 5.25 ROM (Flash Memory for Code Storage) Characteristics (1), Note 2, changed, Note 3, deleted, Table 5.26 ROM (Flash Memory for Code Storage) Characteristics (2), added	TN-RX*-A051A/E
		Appendix 2. Package Dimensions		
		145	Figure C 144-Pin LQFP (PLQP0144KA-A) Package Dimensions, Figure D 100-Pin LQFP (PLQP0100KB-A) Package Dimensions, changed	