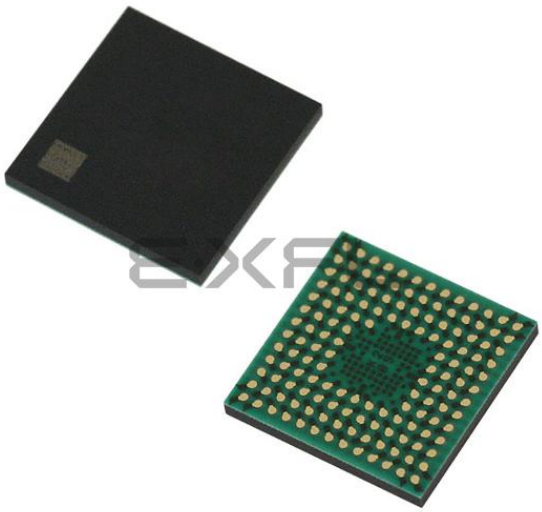
Renesas Electronics America Inc - R5F562N7BDLE#U0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	103
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10/12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	145-TFLGA
Supplier Device Package	145-TFLGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562n7bdle-u0

1.2 List of Products

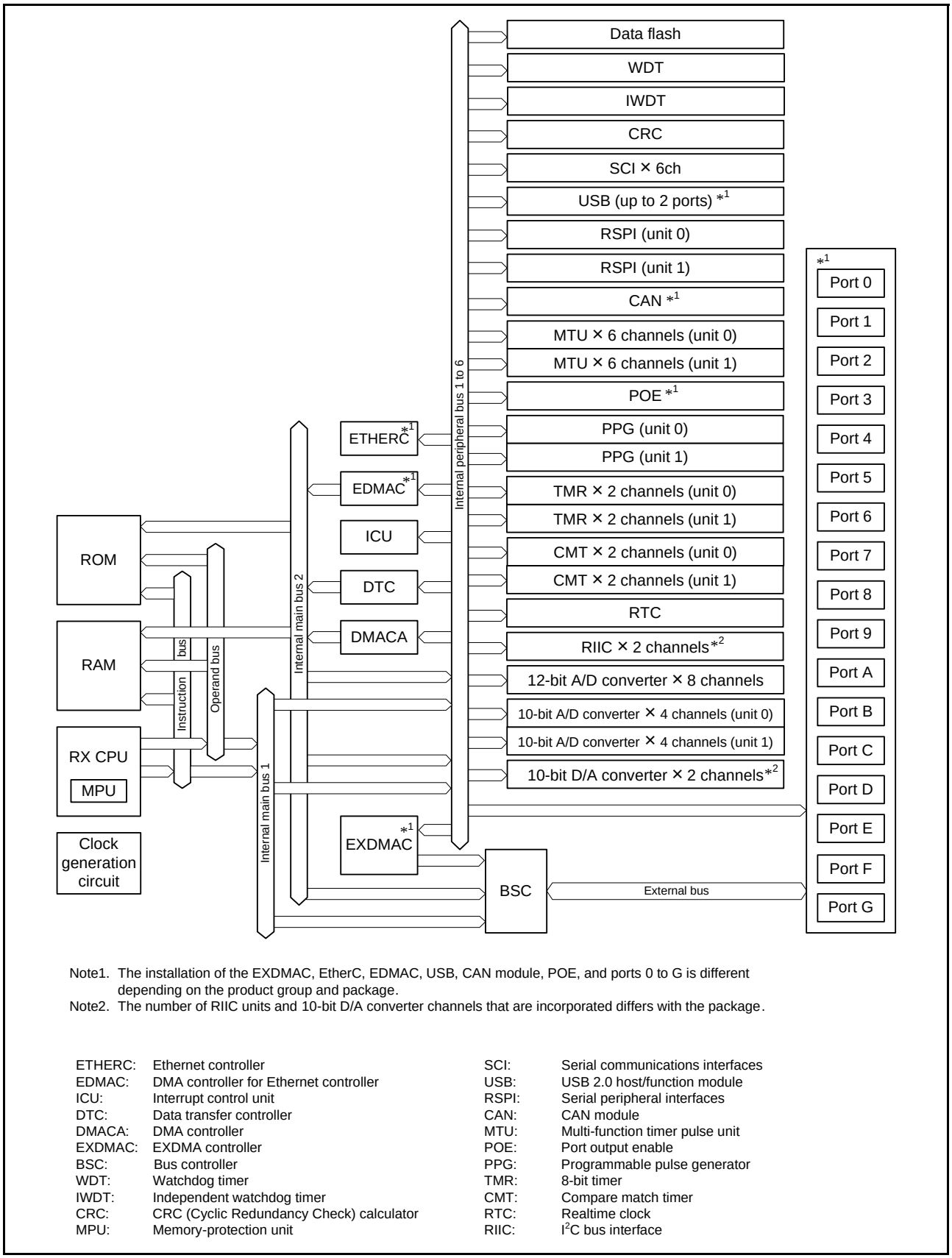
Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no.

Table 1.3 List of Products

Group	Part No.	Package	ROM Capacity	RAM Capacity	Data Flash	Operating Frequency (Max.)
RX62N	R5F562N8BDBG	PLBG0176GA-A	512 Kbytes	96 Kbytes	32 Kbytes	100 MHz
	R5F562N8BDLE	PTLG0145JB-A	512 Kbytes	96 Kbytes	32 Kbytes	100 MHz
	R5F562N8BDFB	PLQP0144KA-A	512 Kbytes	96 Kbytes	32 Kbytes	100 MHz
	R5F562N8BDFP	PLQP0100KB-A	512 Kbytes	96 Kbytes	32 Kbytes	100 MHz
	R5F562N7BDBG	PLBG0176GA-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz
	R5F562N7BDLE	PTLG0145JB-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz
	R5F562N7BDFB	PLQP0144KA-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz
	R5F562N7BDFP	PLQP0100KB-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz
	R5F562N8ADBG	PLBG0176GA-A	512 Kbytes	96 Kbytes	32 Kbytes	100 MHz
	R5F562N8ADLE	PTLG0145JB-A	512 Kbytes	96 Kbytes	32 Kbytes	100 MHz
	R5F562N8ADFB	PLQP0144KA-A	512 Kbytes	96 Kbytes	32 Kbytes	100 MHz
	R5F562N8ADFP	PLQP0100KB-A	512 Kbytes	96 Kbytes	32 Kbytes	100 MHz
	R5F562N7ADBG	PLBG0176GA-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz
	R5F562N7ADLE	PTLG0145JB-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz
	R5F562N7ADFB	PLQP0144KA-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz
	R5F562N7ADFP	PLQP0100KB-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz
RX621	R5F56218BDBG	PLBG0176GA-A	512 Kbytes	96 Kbytes	32 Kbytes	100 MHz
	R5F56218BDLE	PTLG0145JB-A	512 Kbytes	96 Kbytes	32 Kbytes	100 MHz
	R5F56218BDFB	PLQP0144KA-A	512 Kbytes	96 Kbytes	32 Kbytes	100 MHz
	R5F56218BDFP	PLQP0100KB-A	512 Kbytes	96 Kbytes	32 Kbytes	100 MHz
	R5F56218BDLD	PTLG0085JA-A	512 Kbytes	96 Kbytes	32 Kbytes	100 MHz
	R5F56217BDBG	PLBG0176GA-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz
	R5F56217BDLE	PTLG0145JB-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz
	R5F56217BDFB	PLQP0144KA-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz
	R5F56217BDFP	PLQP0100KB-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz
	R5F56217BDLD	PTLG0085JA-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz
	R5F56216BDBG	PLBG0176GA-A	256 Kbytes	64 Kbytes	32 Kbytes	100 MHz
	R5F56216BDLE	PTLG0145JB-A	256 Kbytes	64 Kbytes	32 Kbytes	100 MHz
	R5F56216BDFB	PLQP0144KA-A	256 Kbytes	64 Kbytes	32 Kbytes	100 MHz
	R5F56216BDFP	PLQP0100KB-A	256 Kbytes	64 Kbytes	32 Kbytes	100 MHz
	R5F56216BDLD	PTLG0085JA-A	256 Kbytes	64 Kbytes	32 Kbytes	100 MHz

1.3 Block Diagram

Figure 1.2 shows a block diagram.



Note1. The installation of the EXDMAC, EtherC, EDMAC, USB, CAN module, POE, and ports 0 to G is different depending on the product group and package.
Note2. The number of RIIC units and 10-bit D/A converter channels that are incorporated differs with the package.

ETHERC:	Ethernet controller	SCI:	Serial communications interfaces
EDMAC:	DMA controller for Ethernet controller	USB:	USB 2.0 host/function module
ICU:	Interrupt control unit	RSPI:	Serial peripheral interfaces
DTC:	Data transfer controller	CAN:	CAN module
DMACA:	DMA controller	MTU:	Multi-function timer pulse unit
EXDMAC:	EXDMA controller	POE:	Port output enable
BSC:	Bus controller	PPG:	Programmable pulse generator
WDT:	Watchdog timer	TMR:	8-bit timer
IWDT:	Independent watchdog timer	CMT:	Compare match timer
CRC:	CRC (Cyclic Redundancy Check) calculator	RTC:	Realtime clock
MPU:	Memory-protection unit	RIIC:	I^2C bus interface

Figure 1.2 Block Diagram

Table 1.4 List of Pins and Pin Functions (176-Pin LFBGA) (5 / 6)

Pin No. 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	External Bus EXDMAC	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE, WDT)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
N2		P23	EDACK0-B		USB0_DPUPE-A	MTIOC3D-A/ MTCLKD-A/ PO3	TxD3-B	
N3		P20			USB0_ID	MTIOC1A/ TMRI0-B/ PO0	SDA1/ TxD0	
N4		P17			USB1_VBUS/ USB1_OVRCURB/ USB1_VBUSEN-B	MTIOC3A/ PO15	TxD3-A	IRQ7-B
N5		P15			USB1_OVRCURA/ USB1_DPUPE-B	MTIOC0B/ TMCI2-A/ PO13	SCK3-A	IRQ5-B
N6		P57	WAIT#-A/ WR3#/ BC3#/ EDREQ1-C					
N7		P10			USB1_DPUPE-A	MTIC5W-A/ TMRI3-A		IRQ0-B
N8		P52	RD#				SSLB3-A/ RxD2-B	
N9	VCC							
N10		PC5	A21-A/ CS2#-C/ WAIT#-C	ET_ETXD2		MTIC11W-A/ MTCLKD-B	RSPCKA-A	
N11		PC3	A19-A	ET_TX_ER		MTCLKF-A	TxD5	
N12		PC2	A18-A	ET_RX_DV		MTCLKE-A	SSLA3-A/ RxD5	
N13		P74	CS4#-B	ET_ERXD1/ RMII_RXD1				
N14		P73	CS3#-B	ET_WOL				
N15		PB5	A13			MTIOC10C/ MTCLKF-B/ PO29		
P1		P24	CS4#-C/ EDREQ1-B		USB0_VBUSEN-A	MTIOC4A-A/ MTCLKA-A/ TMRI1/ PO4	SCK3-B	
P2	PLLVCC							
P3		P16			USB0_VBUS/ USB0_OVRCURB/ USB0_VBUSEN-B	MTIOC3C-A/ TMO2/ PO14	RxD3-A	IRQ6-B
P4		P14			USB0_OVRCURA/ USB0_DPUPE-B	TMRI2		IRQ4-B
P5		P13				TMO3	SDA0/ TxD2-A	IRQ3-B/ ADTRG1#
P6	VCC_USB							

Table 1.5 List of Pins and Pin Functions (145-Pin TFLGA) (3 / 5)

Pin No. 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	External Bus EXDMAC	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE, WDT)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
G3	MD1							
G4	MD0							
G10	VSS							
G11		PA5	A5			MTIOC7B/ PO21	RSPCKA-B	
G12		PA6	A6			MTIOC8A/ PO22	MOSIA-B	
G13		PA4	A4			MTIOC7A/ PO20	SSLA0-B	
H1	EXTAL							
H2		P34				MTIOC0A/ TMCI3/ PO12	SCK6-B	IRQ4-A/ TRST#
H3	VCC							
H4	RES#							
H10		PB0	A8			MTIOC9A/ PO24		
H11		P71	CS1#-B	ET_MDIO				
H12		PB1	A9			MTIOC9C/ PO25		
H13		PA7	A7			MTIOC8B/ PO23	MISOA-B	
J1		P33				MTIOC0D/ PO11	CRX0/ RxD6-B	IRQ3-A
J2		P27	CS7#-C			MTIOC2B/ PO7	RSPCKB-A/ SCK1	TCK
J3		P35						NMI
J4		P32				MTIOC0C/ PO10/ RTCOUT	CTX0/ TxD6-B	IRQ2-A
J10		PB2	A10			MTIOC9B/ MTCLKG-B/ PO26		
J11		PB4	A12			MTIOC10A/ MTCLKE-B/ PO28		
J12		PB5	A13			MTIOC10C/ MTCLKF-B/ PO29		
J13		P72	CS2#-B	ET_MDC				
K1		P30				MTIOC4B-A/ TMRI3/ PO8	RxD1/ MISOB-A	IRQ0/ TDI
K2		P24	CS4#-C/ EDREQ1-B		USB0_VBUSEN-A	MTIOC4A-A/ MTCLKA-A/ TMRI1/PO4	SCK3-B	
K3		P31				MTIOC4D-A/ TMCI2-B/ PO9	SSLB0-A	IRQ1/ TMS

Table 1.6 List of Pins and Pin Functions (144-Pin LQFP) (3 / 5)

Pin No. 144-Pin LQFP	Power Supply Clock System Control	I/O Port	External Bus EXDMAC	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE, WDT)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
55		P51	WR1#/BC1#/ WAIT#-D				SSLB2-A/ SCK2	
56		P50	WR0#/ WR#				SSLB1-A/ TxD2-B	
57	VSS							
58		P83	EDACK1-A	ET_CRS/ RMII_CRS_DV		MTIOC4C-B		TRCLK
59	VCC							
60		PC7	A23/ CS0#-B	ET_COL		MTIC11U-A/ MTCLKB-B	MISOA-A	
61		PC6	A22/ CS1#-C	ET_ETXD3		MTIC11V-A/ MTCLKA-B	MOSIA-A	
62		PC5	A21/CS2#-C/ WAIT#-C	ET_ETXD2		MTIC11W-A/ MTCLKD-B	RSPCKA-A	
63		P82	EDREQ1-A	ET_ETXD1/ RMII_TXD1		MTIOC4A-B		TRSYNC
64		P81	EDACK0-A	ET_ETXD0/ RMII_TXD0		MTIOC3D-B		TRDATA1
65		P80	EDREQ0-A	ET_TX_EN/ RMII_TXD_EN		MTIOC3B-B		TRDATA0
66		PC4	A20/CS3#-C	ET_TX_CLK		MTCLKC-B	SSLA0-A	
67		PC3	A19-A	ET_TX_ER		MTCLKF-A	TxD5	
68		P77	CS7#-B	ET_RX_ER/ RMII_RX_ER				
69		P76	CS6#-B	ET_RX_CLK/ REF50CK				
70		PC2	A18-A	ET_RX_DV		MTCLKE-A	SSLA3-A/ RxD5	
71		P75	CS5#-B	ET_ERXD0/ RMII_RXD0				
72		P74	CS4#-B	ET_ERXD1/ RMII_RXD1				
73		PC1	A17-A	ET_ERXD2		MTCLKH-A	SSLA2-A/ SCK5	
74	VCC							
75		PC0	A16-A	ET_ERXD3		MTCLKG-A	SSLA1-A	
76	VSS							
77		P73	CS3#-B	ET_WOL				
78		PB7	A15			MTIOC10D/ PO31		
79		PB6	A14			MTIOC10B/ PO30		
80		PB5	A13			MTIOC10C/ MTCLKF-B/ PO29		
81		PB4	A12			MTIOC10A/ MTCLKE-B/ PO28		

Table 1.8 List of Pins and Pin Functions (85-Pin TFLGA) (3 / 3)

Pin No. 85-Pin TFLGA	Power Supply Clock System Control	I/O Port	External Bus	USB	Timers (MTU, TMR, PPG)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
J4		P16		USB0_VBUS/ USB0_OVRCURB/ USB0_VBUSEN-B	MTIOC3C/TMO2/PO14		IRQ6
J5	VCC_USB						
J6				USB0_DM			
J7		P52	RD#			RxD2-B/SSLB3	
J8		P51	WAIT#			SCK2/SSLB2	
J9		PC3	A19		MTCLKF-A	TxD5	
J10		PC0	A16		MTCLKG-A		
K1		P21		USB0_EXICEN	MTIOC1B/TMCI0/PO1	RxD0/SCL1	
K2		P22		USB0_DRPD	MTIOC3B/MTCLKC/TMO0/PO2	SCK0	
K3		P20		USB0_ID	MTIOC1A/TMRI0/PO0	TxD0/SDA1	
K4	PLLVSS						
K5		P12			TMCI1	RxD2-A/SCL0	IRQ2-B
K6				USB0_DP			
K7	VSS_USB						
K8		P50	WR0#			TxD2-B/SSLB1	
K9		PC2	A18		MTCLKE-A	RxD5	
K10		PC1	A17		MTCLKH-A	SCK5	

Table 1.9 Pin Functions (4 / 7)

Classifications	Pin Name	I/O	Description
8-bit timer	TMO0 to TMO3	Output	Output pins for the compare match signals.
	TMCI0-A/TMCI0-B TMCI1-A/TMCI1-B TMCI2-A/TMCI2-B TMCI3-A/TMCI3-B	Input	Input pins for the external clock signals that drive for the counters.
	TMRI0-A/TMRI0-B TMRI1 TMRI2 TMRI3-A/TMRI3-B	Input	Input pins for the counter-reset signals.
Watchdog timer	WDTOVF#	Output	Output pin for the counter-overflow signal in watchdog-timer mode.
Serial communications interface	TxD0 TxD1-A/TxD1-B TxD2-A/TxD2-B TxD3-A/TxD3-B TxD5 TxD6-A/TxD6-B	Output	Output pins for data transmission.
	RxD0 RxD1-A/RxD1-B RxD2-A/RxD2-B RxD3-A/RxD3-B RxD5 RxD6-A/RxD6-B	Input	Input pins for data reception.
	SCK0 SCK1-A/SCK1-B SCK2-A/SCK2-B SCK3-A/SCK3-B SCK5 SCK6-A/SCK6-B	I/O	Input/output pins for clock signals.
I^2C bus interface	SCL0, SCL1	I/O	Input/output pins for I^2C bus interface clocks. Bus can be directly driven by the NMOS open drain output.
	SDA0, SDA1	I/O	Input/output pins for I^2C bus interface data. Bus can be directly driven by the NMOS open drain output.

Table 1.9 Pin Functions (6 / 7)

Classifications	Pin Name	I/O	Description
USB 2.0 host/function module	VCC_USB	Input	Power-supply pin for the USB. Connect this pin to the system power supply even when the USB is not to be used.
	VSS_USB	Input	Ground pin for the USB. Connect this pin to the system power supply (0 V) even when the USB is not to be used.
	USB0_DP USB1_DP	I/O	Inputs or outputs D+ data for the USB bus.
	USB0_DM USB1_DM	I/O	Inputs or outputs D- data for the USB bus.
	USB0_DPRPD USB1_DPRPD	Output	Enable D+ pull-down.
	USB0_DRPD USB1_DRPD	Output	Enable D- pull-down.
	USB0_EXICEN USB1_EXICEN	Output	Connect these pins to the OTG power supply IC.
	USB0_ID USB1_ID	Input	Connect these pins to the OTG power supply IC.
	USB0_VBUSEN-A/ USB0_VBUSEN-B USB1_VBUSEN-A/ USB1_VBUSEN-B	Output	VBUS power enable pins for the USB.
	USB0_DPUPE-A/ USB0_DPUPE-B USB1_DPUPE-A/ USB1_DPUPE-B	Output	Pull-up pins for the USB.
	USB0_OVRCURA/ USB0_OVRCURB USB1_OVRCURA/ USB1_OVRCURB	Input	Over current pins for the USB.
	USB0_VBUS USB1_VBUS	Input	Input pins for detection of connection and disconnection of the USB cable.
CAN module	CRX0	Input	Input pins for the CAN.
	CTX0	Output	Output pins for the CAN.
Serial peripheral interfaces	RSPCKA-A/ RSPCKA-B	I/O	Clock input/output pins for the RSPI.
	RSPCKB-A/ RSPCKB-B	I/O	Clock input/output pins for the RSPI
	MOSIA-A/MOSIA-B MOSIB-A/MOSIB-B	I/O	Input or output data output from the master for the RSPI.
	MISOA-A/MISOA-B MISOB-A/MISOB-B	I/O	Input or output data output from the slave for the RSPI.
	SSLA0-A/SSLA0-B	I/O	Select the slave for the RSPI.
	SSLA1-A/SSLA1-B SSLA2-A/SSLA2-B SSLA3-A/SSLA3-B	Output	
	SSLB0-A/SSLB0-B	I/O	
	SSLB1-A/SSLB1-B SSLB2-A/SSLB2-B SSLB3-A/SSLB3-B	Output	
Realtime clock	RTCOUT	Output	Output pin for 1-Hz clock.
A/D converter	AN0 to AN7	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRG0#-A/ADTRG0#-B ADTRG1#	Input	Input pins for the external trigger signals that start the A/D conversion.
D/A converter	DA0, DA1	Output	Output pins for the analog signals from the D/A converter.

Table 4.1 List of I/O Registers (Address Order) (26 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 C023h	PORT3	Data register	DR	8	8	2 to 3 PCLK*8
0008 C024h	PORT4	Data register	DR	8	8	2 to 3 PCLK*8
0008 C025h	PORT5	Data register	DR	8	8	2 to 3 PCLK*8
0008 C026h	PORT6	Data register	DR*6*7	8	8	2 to 3 PCLK*8
0008 C027h	PORT7	Data register	DR*6*7	8	8	2 to 3 PCLK*8
0008 C028h	PORT8	Data register	DR*6*7	8	8	2 to 3 PCLK*8
0008 C029h	PORT9	Data register	DR*6*7	8	8	2 to 3 PCLK*8
0008 C02Ah	PORTA	Data register	DR	8	8	2 to 3 PCLK*8
0008 C02Bh	PORTB	Data register	DR	8	8	2 to 3 PCLK*8
0008 C02Ch	PORTC	Data register	DR	8	8	2 to 3 PCLK*8
0008 C02Dh	PORTD	Data register	DR	8	8	2 to 3 PCLK*8
0008 C02Eh	PORTE	Data register	DR*7	8	8	2 to 3 PCLK*8
0008 C02Fh	PORTF	Data register	DR*5*6*7	8	8	2 to 3 PCLK*8
0008 C030h	PORTG	Data register	DR**5*6*7	8	8	2 to 3 PCLK*8
0008 C040h	PORT0	Port register	PORT	8	8	2 to 3 PCLK*8
0008 C041h	PORT1	Port register	PORT	8	8	2 to 3 PCLK*8
0008 C042h	PORT2	Port register	PORT	8	8	2 to 3 PCLK*8
0008 C043h	PORT3	Port register	PORT	8	8	2 to 3 PCLK*8
0008 C044h	PORT4	Port register	PORT	8	8	2 to 3 PCLK*8
0008 C045h	PORT5	Port register	PORT	8	8	2 to 3 PCLK*8
0008 C046h	PORT6	Port register	PORT*6*7	8	8	2 to 3 PCLK*8
0008 C047h	PORT7	Port register	PORT*6*7	8	8	2 to 3 PCLK*8
0008 C048h	PORT8	Port register	PORT*6*7	8	8	2 to 3 PCLK*8
0008 C049h	PORT9	Port register	PORT*6*7	8	8	2 to 3 PCLK*8
0008 C04Ah	PORTA	Port register	PORT	8	8	2 to 3 PCLK*8
0008 C04Bh	PORTB	Port register	PORT	8	8	2 to 3 PCLK*8
0008 C04Ch	PORTC	Port register	PORT	8	8	2 to 3 PCLK*8
0008 C04Dh	PORTD	Port register	PORT	8	8	2 to 3 PCLK*8
0008 C04Eh	PORTE	Port register	PORT*7	8	8	2 to 3 PCLK*8
0008 C04Fh	PORTF	Port register	PORT*5*6*7	8	8	2 to 3 PCLK*8
0008 C050h	PORTG	Port register	PORT*5*6*7	8	8	2 to 3 PCLK*8
0008 C060h	PORT0	Input buffer control register	ICR	8	8	2 to 3 PCLK*8
0008 C061h	PORT1	Input buffer control register	ICR	8	8	2 to 3 PCLK*8
0008 C062h	PORT2	Input buffer control register	ICR	8	8	2 to 3 PCLK*8
0008 C063h	PORT3	Input buffer control register	ICR	8	8	2 to 3 PCLK*8
0008 C064h	PORT4	Input buffer control register	ICR	8	8	2 to 3 PCLK*8
0008 C065h	PORT5	Input buffer control register	ICR	8	8	2 to 3 PCLK*8
0008 C066h	PORT6	Input buffer control register	ICR*6*7	8	8	2 to 3 PCLK*8
0008 C067h	PORT7	Input buffer control register	ICR*6*7	8	8	2 to 3 PCLK*8
0008 C068h	PORT8	Input buffer control register	ICR*6*7	8	8	2 to 3 PCLK*8
0008 C069h	PORT9	Input buffer control register	ICR*6*7	8	8	2 to 3 PCLK*8
0008 C06Ah	PORTA	Input buffer control register	ICR	8	8	2 to 3 PCLK*8
0008 C06Bh	PORTB	Input buffer control register	ICR	8	8	2 to 3 PCLK*8
0008 C06Ch	PORTC	Input buffer control register	ICR	8	8	2 to 3 PCLK*8
0008 C06Dh	PORTD	Input buffer control register	ICR	8	8	2 to 3 PCLK*8

Table 4.1 List of I/O Registers (Address Order) (33 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000A 0254h	USB1	USB request type register	USBREQ	16	16	at least 9 PCLK*9
000A 0256h	USB1	USB request value register	USBVAL	16	16	at least 9 PCLK*9
000A 0258h	USB1	USB request index register	USBINDX	16	16	at least 9 PCLK*9
000A 025Ah	USB1	USB request length register	USBLENG	16	16	at least 9 PCLK*9
000A 025Ch	USB1	DCP configuration register	DCPCFG	16	16	at least 9 PCLK*9
000A 025Eh	USB1	DCP maximum packet size register	DCPMAXP	16	16	at least 9 PCLK*9
000A 0260h	USB1	DCP control register	DCPCTR	16	16	at least 9 PCLK*9
000A 0264h	USB1	Pipe window select register	PIPESEL	16	16	at least 9 PCLK*9
000A 0268h	USB1	Pipe configuration register	PIPECFG	16	16	at least 9 PCLK*9
000A 026Ch	USB1	Pipe maximum packet size register	PIPEMAXP	16	16	at least 9 PCLK*9
000A 026Eh	USB1	Pipe cycle control register	PIPEPERI	16	16	at least 9 PCLK*9
000A 0270h	USB1	Pipe 1 control register	PIPE1CTR	16	16	at least 9 PCLK*9
000A 0272h	USB1	Pipe 2 control register	PIPE2CTR	16	16	at least 9 PCLK*9
000A 0274h	USB1	Pipe 3 control register	PIPE3CTR	16	16	at least 9 PCLK*9
000A 0276h	USB1	Pipe 4 control register	PIPE4CTR	16	16	at least 9 PCLK*9
000A 0278h	USB1	Pipe 5 control register	PIPE5CTR	16	16	at least 9 PCLK*9
000A 027Ah	USB1	Pipe 6 control register	PIPE6CTR	16	16	at least 9 PCLK*9
000A 027Ch	USB1	Pipe 7 control register	PIPE7CTR	16	16	at least 9 PCLK*9
000A 027Eh	USB1	Pipe 8 control register	PIPE8CTR	16	16	at least 9 PCLK*9
000A 0280h	USB1	Pipe 9 control register	PIPE9CTR	16	16	at least 9 PCLK*9
000A 0290h	USB1	Pipe 1 transaction counter enable register	PIPE1TRE	16	16	at least 9 PCLK*9
000A 0292h	USB1	Pipe 1 transaction counter register	PIPE1TRN	16	16	at least 9 PCLK*9
000A 0294h	USB1	Pipe 2 transaction counter enable register	PIPE2TRE	16	16	at least 9 PCLK*9
000A 0296h	USB1	Pipe 2 transaction counter register	PIPE2TRN	16	16	at least 9 PCLK*9
000A 0298h	USB1	Pipe 3 transaction counter enable register	PIPE3TRE	16	16	at least 9 PCLK*9
000A 029Ah	USB1	Pipe 3 transaction counter register	PIPE3TRN	16	16	at least 9 PCLK*9

Table 5.3 DC Characteristics (2)

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
T_a = -40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	All output pins	V_{OH}	VCC-0.5	—	—	V	I_{OH} = -1 mA
Output low voltage	All output pins (except for RIIC pins)	V_{OL}	—	—	0.5	V	I_{OL} = 1.0 mA
	RIIC pins		—	—	0.4	V	I_{OL} = 3.0 mA
			—	—	0.6		I_{OL} = 6.0 mA
	RIIC pins (only P12 and P13 in channel 0)	V_{OL}	—	—	0.4	V	I_{OL} = 15.0 mA (ICFER.FMPE = 1)
			—	0.4	—		I_{OL} = 20.0 mA (ICFER.FMPE = 1)
Input leakage current	RES#, MD pin, EMLE, NMI	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	Ports 03, 05, 10, 11, 14, 15 ports 22 to 27 ports 30 to 32, 34, 35 ports 4 to G	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0 V V_{in} = VCC
	Ports 00 to 02, 07, 12, 13 Ports 16, 17, 20, 21, 33		—	—	5.0		
Input pull-up MOS current	Ports 9 to E, G	$-I_p$	10	—	300	µA	VCC = 2.7 to 3.6 V V_{in} = 0 V
Input capacitance	All input pins (except for ports 12, 13, 20, 21 ports 40 to 47, and EMLE)	C_{in}	—	—	15	pF	V_{in} = 0 V f = 1 MHz T_a = 25°C
	Ports 12, 13, 20, 21, Ports 40 to 47, EMLE		—	—	30		

Table 5.4 DC Characteristics (3)

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
T_a = -40 to +85°C

Item					Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Supply current*2	In operation	Max.*3			I_{CC}*4	—	—	100	mA	ICLK = 100 MHz PCLK = 50 MHz BCLK = 50 MHz
		Normal operation	Peripheral function: Clocks supplied*5			—	48	—		
			Peripheral function: Clocks not supplied*5			—	35	—		
		Increased by BGO operation*6				—	15	—		
	Sleep					—	20	60		
	All-module-clock-stop mode*7					—	14	28		
	Standby mode	Software standby mode				—	0.12	3.0	mA	
		Deep software standby mode	RTC in operation	RAM, USB retained		—	30	206	µA	
				RAM, USB power supply halted		—	26	66	µA	
			RTC halted	RAM, USB retained		—	25	200	µA	
				RAM, USB power supply halted		—	21	60	µA	
Analog power supply current	During 12-bit A/D conversion (per unit)				AI_{CC}	—	2.5	3.0	mA	
	During 10-bit A/D conversion (per unit)					—	0.8	1.2	mA	
	During D/A conversion (per channel)					—	0.3	2.0	µA	
	Idle (all units)					—	30	35	µA	
	During A/D or D/A standby (all units)					—	0.1	4.0	µA	
Reference power supply current	During 12-bit A/D conversion (per unit)				AI_{CC}	—	0.5	0.7	mA	
	During 10-bit A/D conversion (per unit)					—	0.06	0.1	mA	
	During D/A conversion (per channel)					—	0.6	1.0	mA	
	Idle (all units)					—	0.4	0.6	mA	
	During A/D or D/A standby (all units)					—	0.1	2.0	µA	
RAM standby voltage					V_{RAM}	2.48	—	—	V	
VCC rising gradient					SVCC	—	—	20	ms/V	

Note 1. The V_{IH} characteristic of the pins multiplexed with 5-V tolerant ports 00 to 02, 07, 12, 13, 16, 17, 20, 21, and 33 is the same as the V_{IH} characteristic of 5-V tolerant ports.
Note 2. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 3. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
Note 4. ICC depends on f (ICLK) as follows. (ICLK: PCLK: BCLK: BCLK pin = 8 : 4: 8: 4)
ICC max. = 0.89 x f + 11 (max.)
ICC typ. = 0.43 x f + 5 (normal operation, peripheral function: clocks supplied)
ICC typ. = 0.30 x f + 5 (normal operation, peripheral function: clocks not supplied)
ICC max. = 0.48 x f + 12 (sleep mode)
Note 5. This does not include the BGO operation.
Note 6. Incremented if data is written to or erased from the ROM or data flash for data storage during the program execution.
Note 7. The values are for reference.

Table 5.5 Permissible Output Currents

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
T_a = -40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (average value per pin)	All output pins except for RIIC pins	I_{OL}	—	—	2.0	mA
	RIIC pins (ICFER.FMPE = 0)	I_{OL}	—	—	6.0	mA
	RIIC pins (ICFER.FMPE = 1)	I_{OL}	—	—	20.0	mA
Permissible output low current (max. value per pin)	All output pins except for RIIC pins	I_{OL}	—	—	4.0	mA
	RIIC pins (ICFER.FMPE = 0)	I_{OL}	—	—	6.0	mA
	RIIC pins (ICFER.FMPE = 1)	I_{OL}	—	—	20.0	mA
Permissible output low current (total)	Total of all output pins	ΣI_{OL}	—	—	80	mA
Permissible output high current (average value per pin)	All output pins (except for USB_DPUPE pin)	$-I_{OH}$	—	—	2.0	mA
	USB_DPUPE pin	$-I_{OH}$	—	—	3.0	mA
Permissible output high current (max. value per pin)	All output pins	$-I_{OH}$	—	—	4.0	mA
Permissible output high current (total)	Total of all output pins	$\Sigma-I_{OH}$	—	—	80	mA

Caution: To protect the LSI's reliability, the output current values should not exceed the permissible output current.

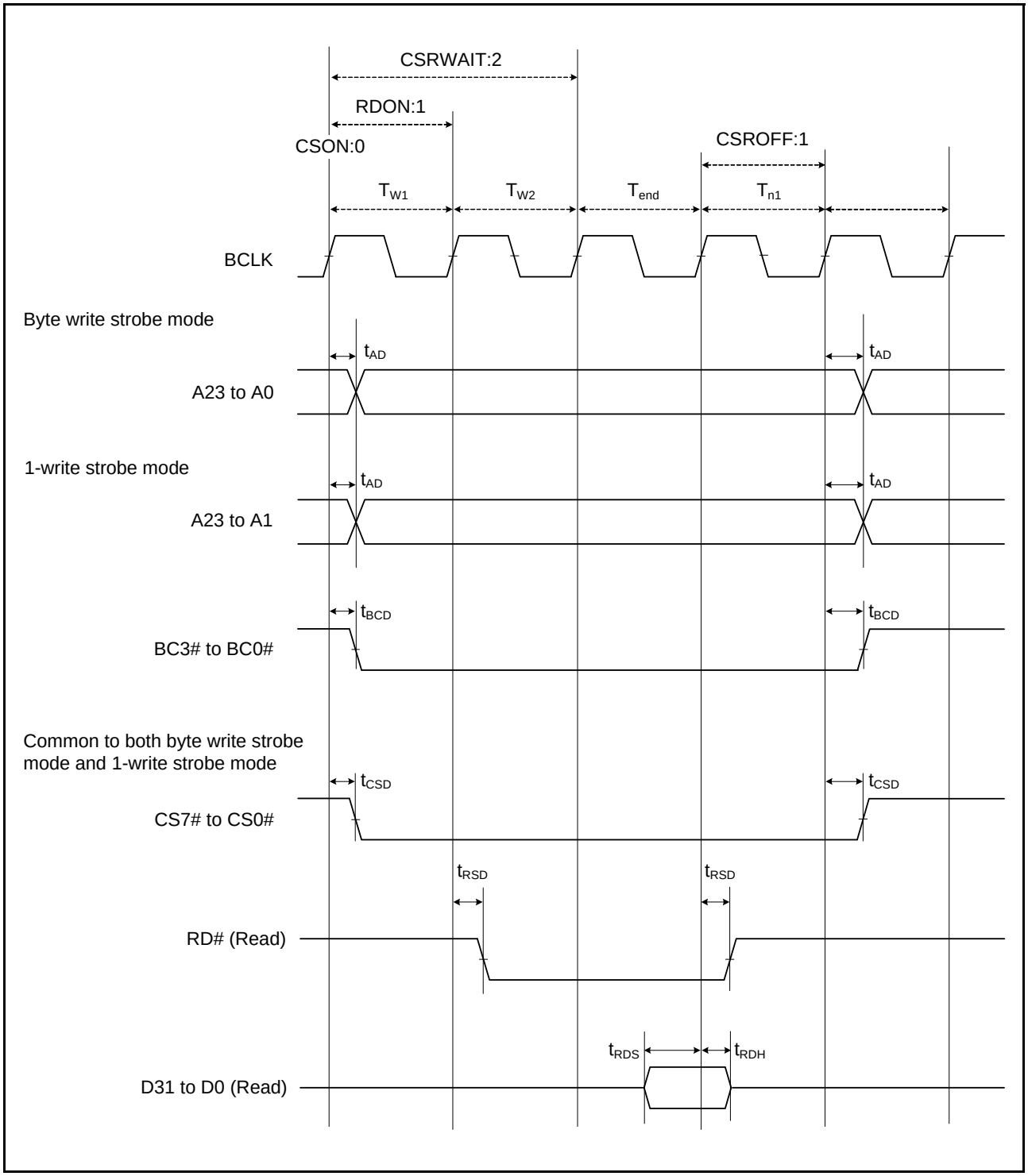


Figure 5.10 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)

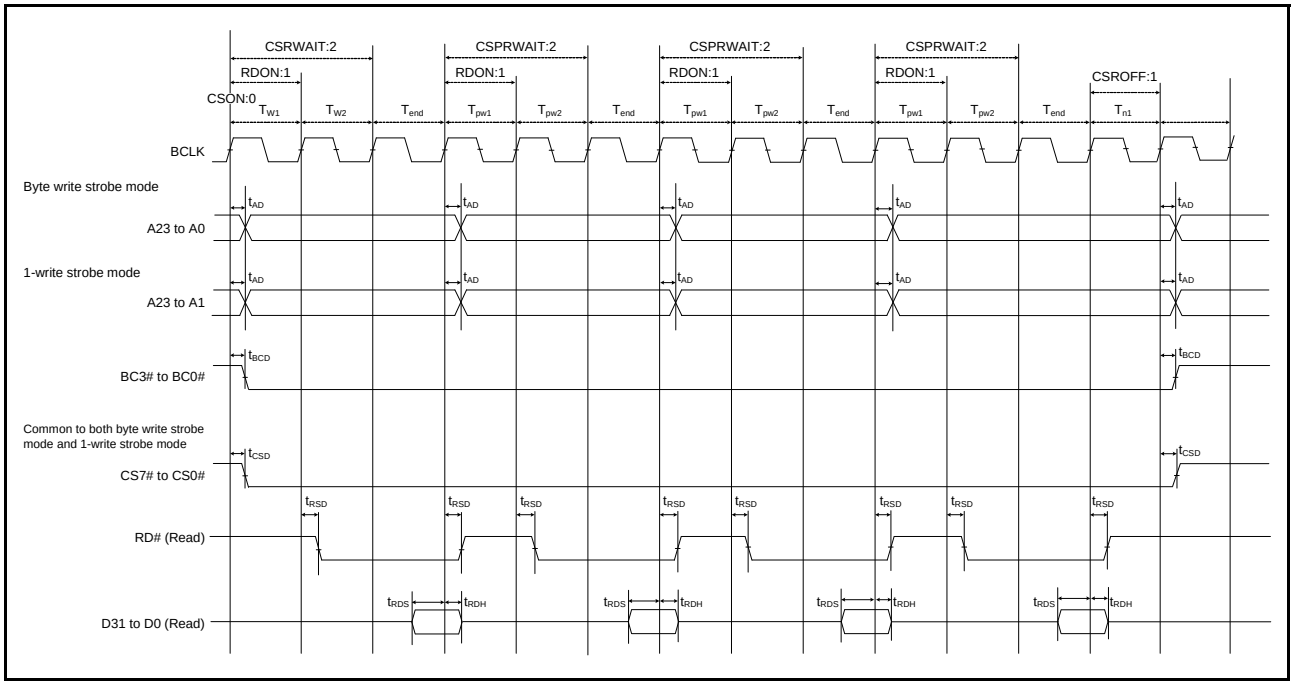


Figure 5.12 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)

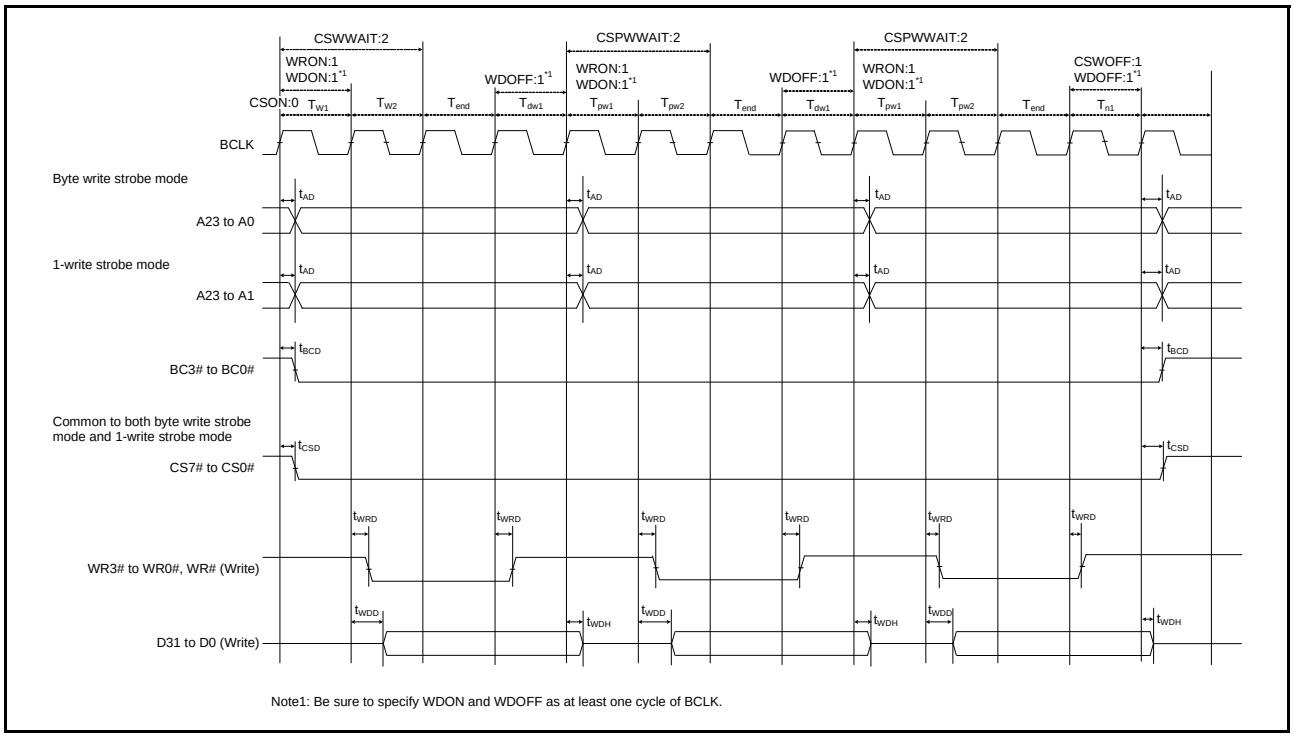
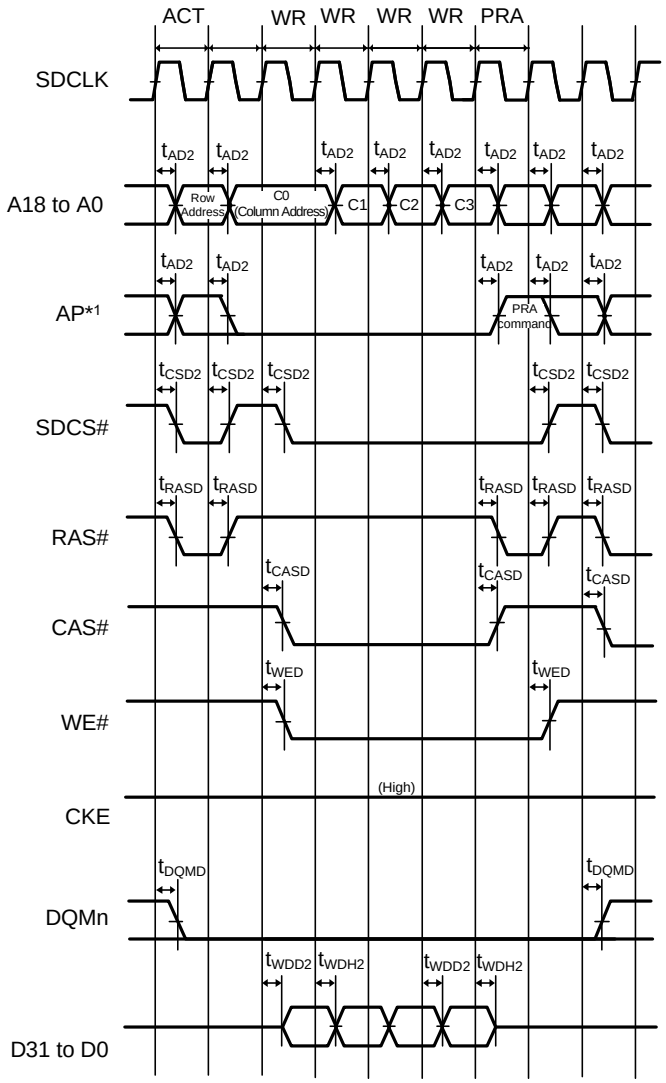


Figure 5.13 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)



Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.18 SDRAM Space Multiple Write Bus Timing

Table 5.14 Timing of On-Chip Peripheral Modules (3)

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
PCLK = 8 to 50 MHz
T_a = -40 to +85°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
CAN	Transmit data delay time		t_{CTXD}	—	40.0	ns	Figure 5.37
	Receive data setup time		t_{CRXS}	40.0	—	ns	
	Receive data hold time		t_{CRXH}	40.0	—	ns	
RSPI	RSPCK clock cycle	Master	t_{SPcyc}	2	4096	t_{Pcyc} *1	Figure 5.38
		Slave		8	4096		
	RSPCK clock high pulse width	Master	t_{SPCKWH}	$(t_{SPcyc}-t_{SPCKR}-t_{SPCKF})$ / 2-3	—	ns	
		Slave		$(t_{SPcyc}-t_{SPCKR}-t_{SPCKF})$ / 2	—		
	RSPCK clock low pulse width	Master	t_{SPCKWL}	$(t_{SPcyc}-t_{SPCKR}-t_{SPCKF})$ / 2-3	—	ns	
		Slave		$(t_{SPcyc}-t_{SPCKR}-t_{SPCKF})$ / 2	—		
	RSPCK clock rise/fall time	Output [176-pin LFBGA/ 145-pin TFLGA/ 144-pin LQFP]	t_{SPCKr}, t_{SPCKf}	—	5	ns	
		Output [100-pin LQFP/ 85-pin TFLGA]		—	10		
		Input		—	1	µs	

Note 1. tPcyc: PCLK cycle

Table 5.14 Timing of On-Chip Peripheral Modules (4)

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
PCLK = 8 to 50 MHz
T_a = -40 to +85°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
RSPI	Data input setup time	Master [176-pin LFBGA/ 145-pin TFLGA/ 144-pin LQFP]	t_{SU}	16	—	ns	Figure 5.39 to Figure 5.42
		Master [100-pin LQFP/ 85-pin TFLGA]		30	—		
		Slave		20-2 × t_{Pcyc}	—		
	Data input hold time	Master	t_H	0	—	ns	
		Slave		20+2 × t_{Pcyc}	—		
	SSL setup time	Master	t_{LEAD}	1	8	t_{SPcyc}	
		Slave		4	—	t_{Pcyc}	
	SSL hold time	Master	t_{LAG}	1	8	t_{SPcyc}	
		Slave		4	—	t_{Pcyc}	
	Data output delay time	Master [176-pin LFBGA/ 145-pin TFLGA/ 144-pin LQFP]	t_{OD}	—	20	ns	
		Master [100-pin LQFP/ 85-pin TFLGA]		—	30		
		Slave [176-pin LFBGA/ 145-pin TFLGA/ 144-pin LQFP]		—	3 × t_{Pcyc}+40		
		Slave [100-pin LQFP/ 85-pin TFLGA]		—	3 × t_{Pcyc}+50		

Note 1. tPcyc: PCLK cycle

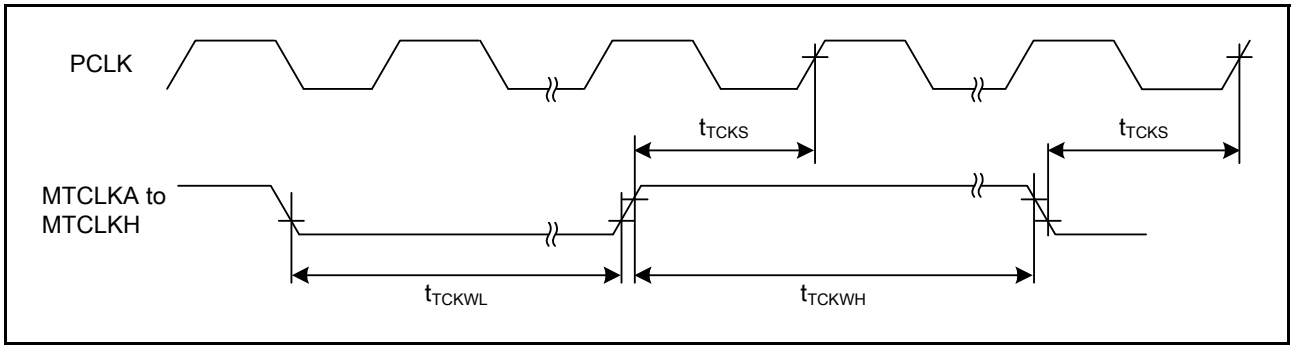


Figure 5.27 MTU2 Clock Input Timing

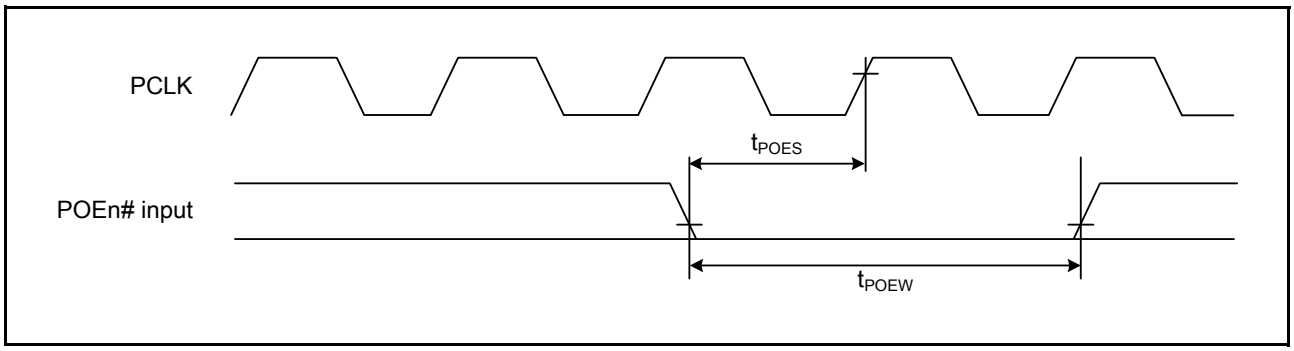


Figure 5.28 POE# Input Timing

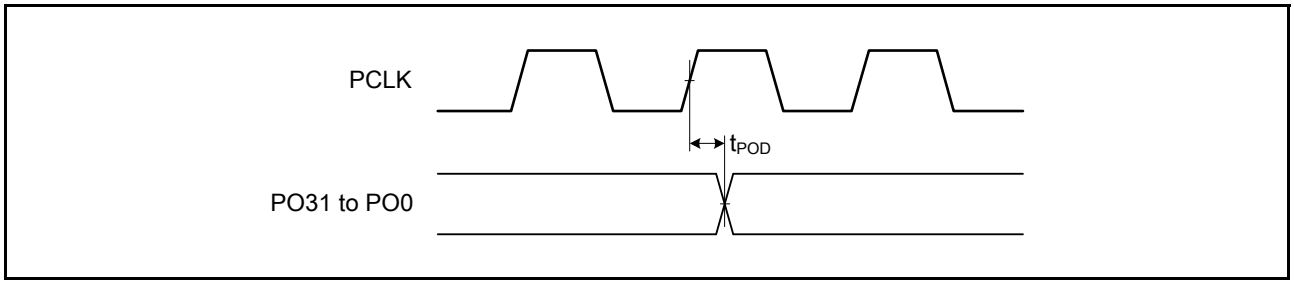


Figure 5.29 PPG Output Timing

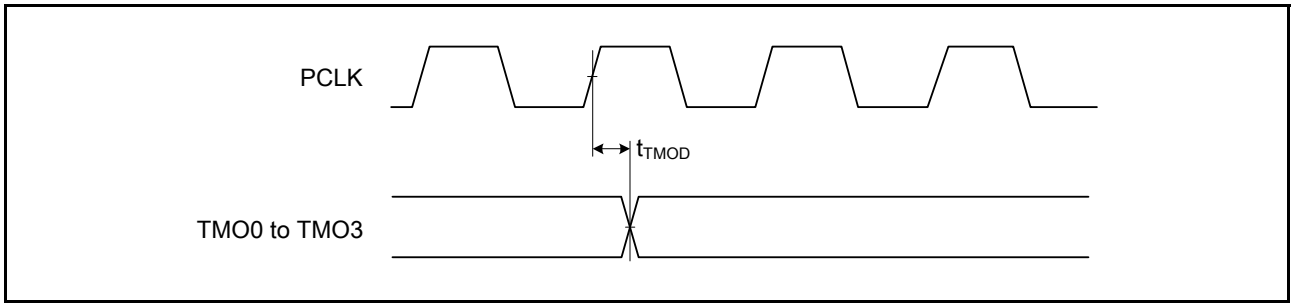


Figure 5.30 8-Bit Timer Output Timing

REVISION HISTORY — RX62N Group, RX621 Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	2011.02.04	—	First Edition issued
1.10	2011.02.10	—	Features reviewed
1.20	2011.06.10		1. Overview
		2 to 5	Table 1.1 Outline of Specification, Description changed
		40 to 46	Table 1.9 Pin Functions, Description changed
			4. I/O Registers
		52 to 86	Table 4.1 List of I/O Registers (Address Order), Description changed
			5. Electrical Characteristics
		90	Table 5.2 DC Characteristics (3) , changed
		111	Figure 5.23 EDACK0 and EDACK1 Single-Address Transfer Timing (for a CS Area), changed
		111	Figure 5.24 EDACK0 and EDACK1 Single-Address Transfer Timing (for SDRAM), changed
1.30	2012.01.11		1. Overview
		2	Table 1.1 Outline of Specifications (1/4), changed, note 1, note 2 deleted
		13	Figure 1.6 Pin Assignment of the 144-Pin LQFP (Assistance Diagram), changed
		15	Figure 1.8 Pin Assignment of the 100-Pin LQFP (Assistance Diagram), changed
		33	Table 1.7 List of Pins and Pin Functions (100-Pin LQFP) (1/4), changed
		37	Table 1.8 List of Pins and Pin Functions (85-Pin TFLGA) (2/3), changed
			4. I/O Registers
		52 to 87	Table 4.1 List of I/O Registers (Address Order), Description changed
			5. Electrical Characteristics
		91	Table 5.4 DC Characteristics (3), specification added
		98	Table 5.9 Control Signal Timing, note changed
		122	Table 5.18 Timing of On-Chip Peripheral Modules (6), conditions changed