Renesas Electronics America Inc - R5F562N8ADFB#V0 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	EBI/EMI, I²C, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	103
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10/12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562n8adfb-v0

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 lists the functions of products.

Table 1.1 Outline of Specifications (1 / 4)

Classification	Module/Function	Description
CPU	CPU	・ Maximum operating frequency: 100 MHz ・ 32-bit RX CPU ・ Minimum instruction execution time: One instruction per state (cycle of the system clock) ・ Address space: 4-Gbyte linear ・ Register set of the CPU General purpose: Sixteen 32-bit registers Control: Nine 32-bit registers Accumulator: One 64-bit register ・ Basic instructions: 73 ・ Floating-point instructions: 8 ・ DSP instructions: 9 ・ Addressing modes: 10 ・ Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian ・ On-chip 32-bit multiplier: 32 x 32 → 64 bits ・ On-chip divider: 32 / 32 → 32 bits ・ Barrel shifter: 32 bits ・ Memory-protection unit (MPU)
	FPU	・ Single precision (32-bit) floating point ・ Data types and floating-point exceptions in conformance with the IEEE754 standard
Memory	ROM	・ ROM capacity: 512 Kbytes (max.) ・ Two on-board programming modes Boot mode (The user MAT is programmable via the SCI and USB.) User program mode ・ Parallel programmer mode (for off-board programming)
	RAM	RAM capacity: 96 Kbytes (max.)
	Data flash	Data flash capacity: 32 Kbytes
MCU operating modes		・ Single-chip mode, on-chip ROM enabled expansion mode, and on-chip ROM disabled expansion mode (software switching)
Clock	Clock generation circuit	・ Two circuits: Main clock oscillator and subclock oscillator ・ Internal oscillator: Low-speed on-chip oscillator ・ Structure of a PLL frequency synthesizer and frequency divider for selectable operating frequency ・ Oscillation stoppage detection ・ Independent frequency-division and multiplication settings for the system clock (ICLK), peripheral module clock (PCLK), and external bus clock (BCLK) The CPU and other bus masters run in synchronization with the system clock (ICLK): 8 to 100 MHz Peripheral modules run in synchronization with the peripheral module clock (PCLK): 8 to 50 MHz ・ Devices connected to the external bus run in synchronization with the external bus clock (BCLK pin): 8 to 50 MHz*1
Reset		・ Pin reset, power-on reset, voltage-monitoring reset, watchdog timer reset, independent watchdog timer reset, and deep software standby reset
Voltage detection circuit		・ When the voltage on VCC falls below the voltage detection level (Vdet), an internal reset or internal interrupt is generated.
Low power consumption	Low power consumption facilities	・ Module stop function ・ Four low power consumption modes Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode

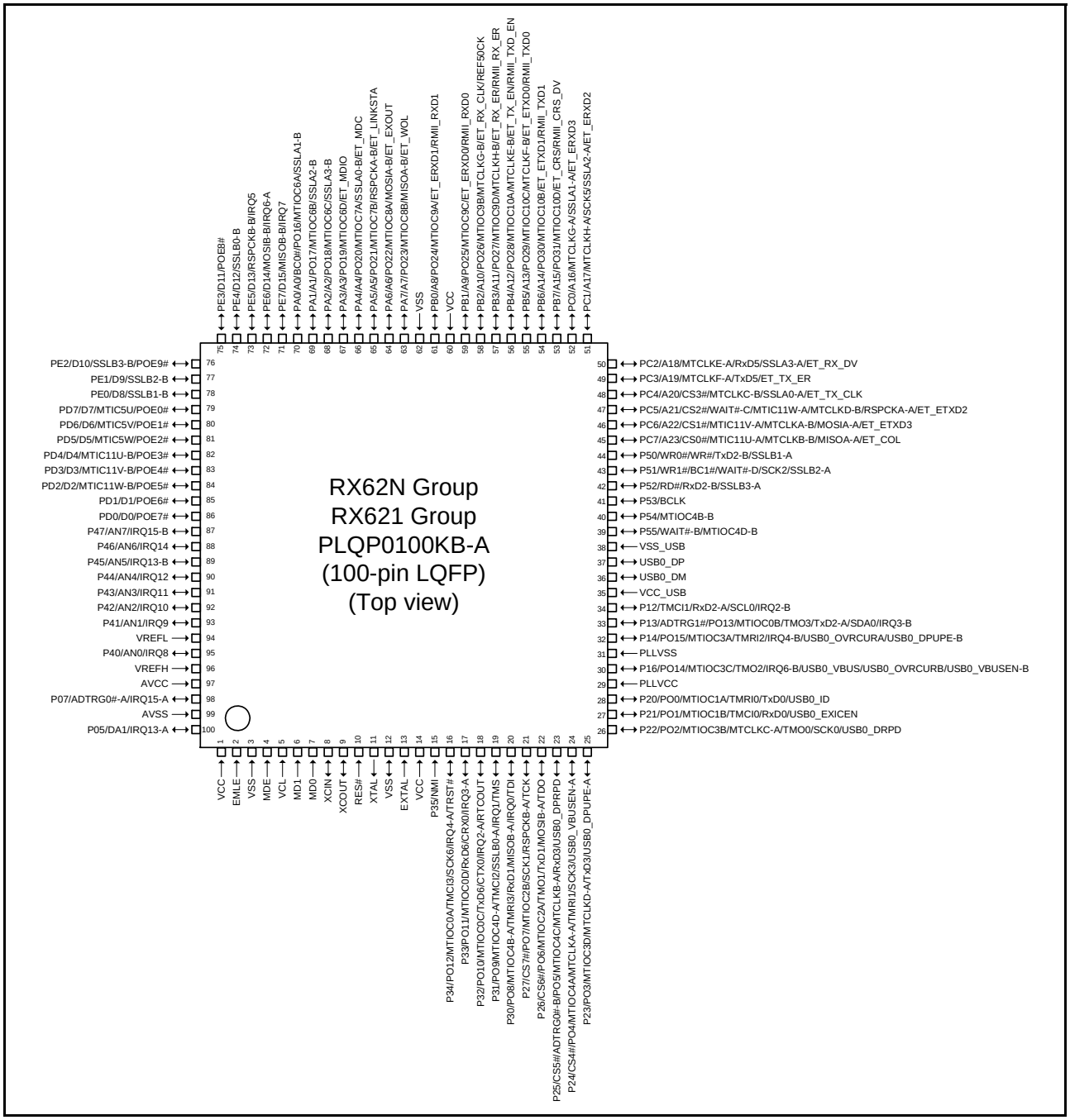


Figure 1.7 Pin Assignment of the 100-Pin LQFP

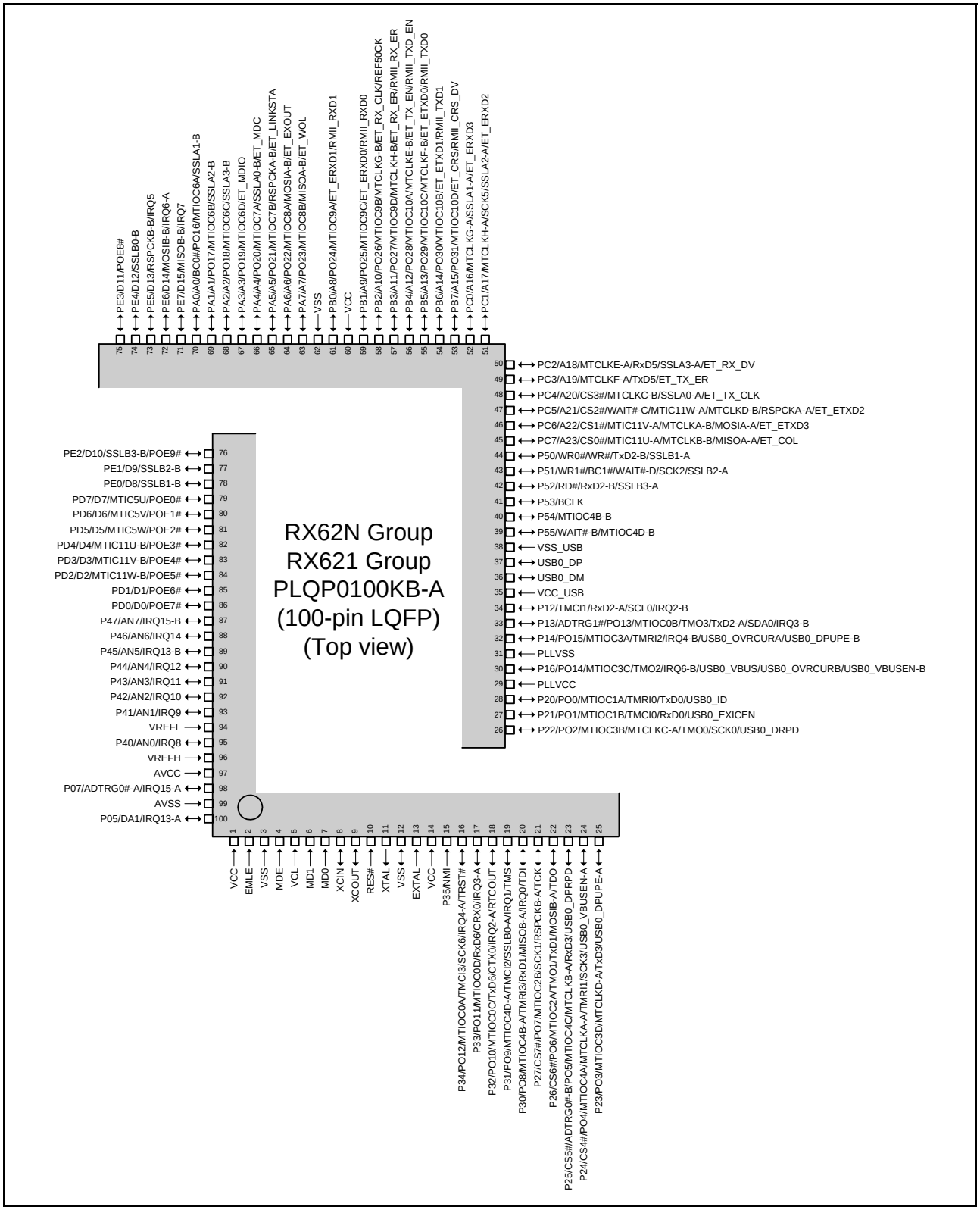


Figure 1.8 Pin Assignment of the 100-Pin LQFP (Assistance Diagram)

Table 1.5 List of Pins and Pin Functions (145-Pin TFLGA) (4 / 5)

Pin No. 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	External Bus EXDMAC	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE, WDT)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
K4		P26	CS6#-C			MTIOC2A/ TMO1/ PO6	MOSIB-A/ TxD1	TDO
K5	BCLK	P53						
K6	VSS							
K7		PC7	A23/ CS0#-B	ET_COL		MTIC11U-A/ MTCLKB-B	MISOA-A	
K8		P82	EDREQ1-A	ET_ETXD1/ RMII_TXD1		MTIOC4A-B		TRSYNC
K9		PC3	A19-A	ET_TX_ER		MTCLKF-A	TxD5	
K10		PB7	A15			MTIOC10D/ PO31		
K11		P73	CS3#-B	ET_WOL				
K12		PC0	A16-A	ET_ERXD3		MTCLKG-A	SSLA1-A	
K13		PB3	A11			MTIOC9D/ MTCLKH-B/ PO27		
L1		P25	CS5#-C/ EDACK1-B		USB0_DPRPD	MTIOC4C-A/ MTCLKB-A/ PO5	RxD3-B	ADTRG0#-B
L2		P22	EDREQ0-B		USB0_DRPD	MTIOC3B-A/ MTCLKC-A/ TMO0/PO2	SCK0	
L3		P17				MTIOC3A/ PO15	TxD3-A	IRQ7-B
L4		P12				TMCI1-B	SCL0/ RxD2-A	IRQ2-B
L5	VCC_USB							
L6		P56	EDACK1-C			MTIOC3C-B		
L7		P52	RD#				SSLB3-A/ RxD2-B	
L8		P83	EDACK1-A	ET_CRS/ RMII_CRS_DV		MTIOC4C-B		TRCLK
L9		P81	EDACK0-A	ET_ETXD0/ RMII_TXD0		MTIOC3D-B		TRDATA1
L10		P77	CS7#-B	ET_RX_ER/ RMII_RX_ER				
L11		P75	CS5#-B	ET_ERXD0/ RMII_RXD0				
L12	VCC							
L13		PB6	A14			MTIOC10B/ PO30		
M1		P23	EDACK0-B		USB0_DPUPE-A	MTIOC3D-A/ MTCLKD-A/ PO3	TxD3-B	
M2		P20			USB0_ID	MTIOC1A/ TMRI0-B/ PO0	SDA1/ TxD0	
M3	PLLVCC							

Table 1.5 List of Pins and Pin Functions (145-Pin TFLGA) (5 / 5)

Pin No. 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	External Bus EXDMAC	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE, WDT)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
M4		P15				MTIOC0B/ TMCI2-A/ PO13	SCK3-A	IRQ5-B
M5		P14			USB0_OVRCURA/ USB0_DPUPE-B	TMRI2		IRQ4-B
M6	VSS_USB							
M7		P55	WAIT#-B/ EDREQ0-C	ET_EXOUT		MTIOC4D-B		TRDATA3
M8		P50	WR0#/ WR#				SSLB1-A/ TxD2-B	
M9		PC6	A22/CS1#-C	ET_ETXD3		MTIC11V-A/ MTCLKA-B	MOSIA-A	
M10		P80	EDREQ0-A	ET_TX_EN/ RMII_TXD_EN		MTIOC3B-B		TRDATA0
M11		PC2	A18-A	ET_RX_DV		MTCLKE-A	SSLA3-A/ RxD5	
M12		PC1	A17-A	ET_ERXD2		MTCLKH-A	SSLA2-A/ SCK5	
M13	VSS							
N1		P21			USB0_EXICEN	MTIOC1B/ TMCI0-B/ PO1	SCL1/RxD0	
N2		P16			USB0_VBUS/ USB0_OVRCURB/ USB0_VBUSEN-B	MTIOC3C-A/ TMO2/ PO14	RxD3-A	IRQ6-B
N3	PLLVSS							
N4		P13				TMO3	SDA0/ TxD2-A	IRQ3-B/ ADTRG1#
N5					USB0_DM			
N6					USB0_DP			
N7		P54	EDACK0-C	ET_LINKSTA		MTIOC4B-B		TRDATA2
N8		P51	WR1#/BC1#/ WAIT#-D				SSLB2-A/ SCK2	
N9	VCC							
N10		PC5	A21/CS2#-C/ WAIT#-C	ET_ETXD2		MTIC11W-A/ MTCLKD-B	RSPCKA-A	
N11		PC4	A20/CS3#-C	ET_TX_CLK		MTCLKC-B	SSLA0-A	
N12		P76	CS6#-B	ET_RX_CLK/ REF50CK				
N13		P74	CS4#-B	ET_ERXD1/ RMII_RXD1				

Table 1.7 List of Pins and Pin Functions (100-Pin LQFP) (1 / 4)

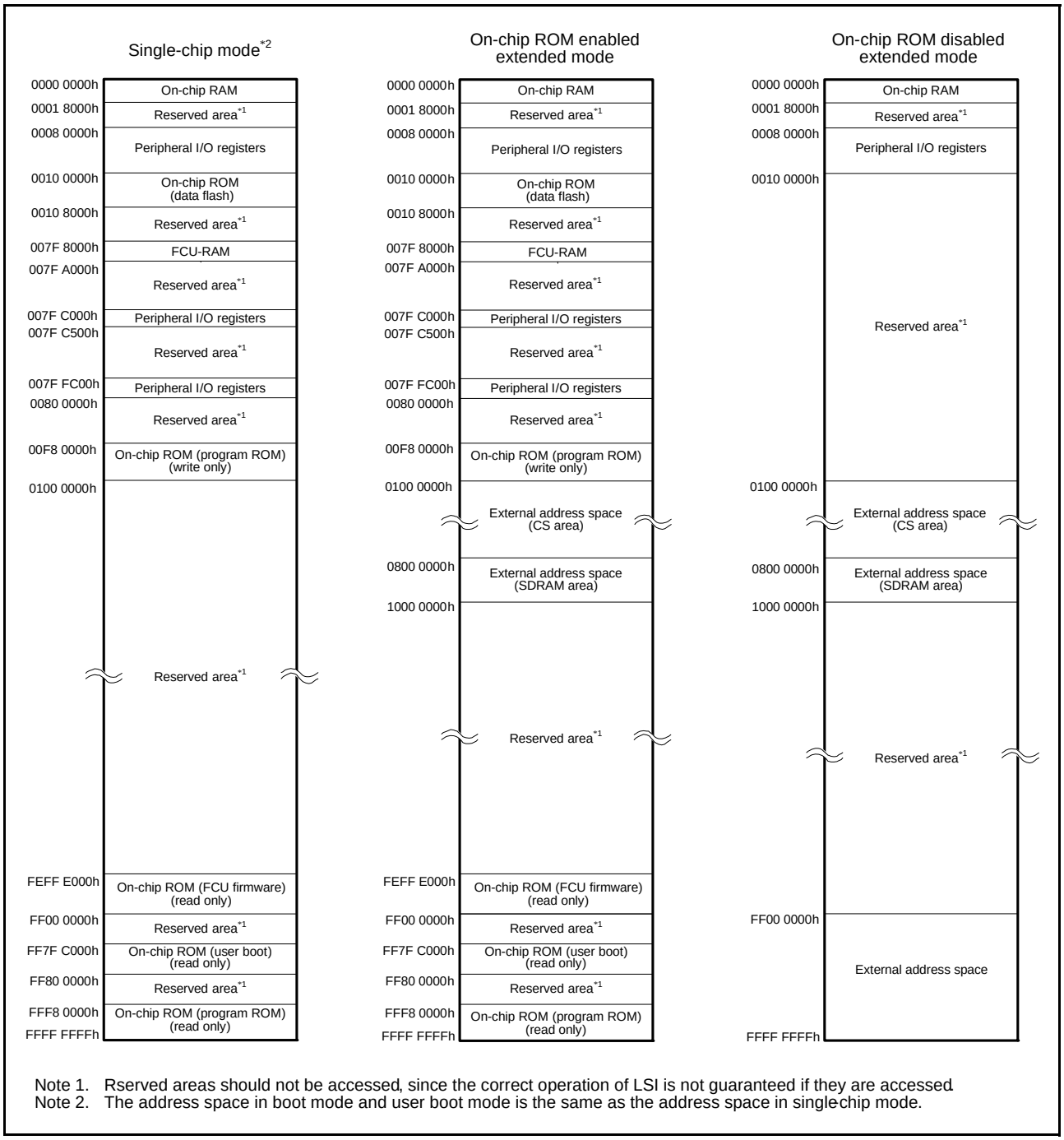
Pin No. 100-Pln LQFP	Power Supply Clock System Control	I/O Port	External Bus	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
1	VCC							
2	EMLE							
3	VSS							
4	MDE							
5	VCL							
6	MD1							
7	MD0							
8	XCIN							
9	XCOUT							
10	RES#							
11	XTAL							
12	VSS							
13	EXTAL							
14	VCC							
15		P35						NMI
16		P34				MTIOC0A/ TMCI3/ PO12	SCK6	IRQ4-A/ TRST#
17		P33				MTIOC0D/ PO11	CRX0/ RxD6	IRQ3-A
18		P32				MTIOC0C/ PO10/ RTCOUT	CTX0/ TxD6	IRQ2-A
19		P31				MTIOC4D-A/ TMCI2/ PO9	SSLB0-A	IRQ1/ TMS
20		P30				MTIOC4B-A/ TMRI3/ PO8	RxD1/ MISOB-A	IRQ0/ TDI
21		P27	CS7#			MTIOC2B/ PO7	RSPCKB-A/ SCK1	TCK
22		P26	CS6#			MTIOC2A/ TMO1/ PO6	MOSIB-A/ TxD1	TDO
23		P25	CS5#		USB0_DPRPD	MTIOC4C/ MTCLKB-A/ PO5	RxD3	ADTRG0#-B
24		P24	CS4#		USB0_VBUSEN-A	MTIOC4A/ MTCLKA-A/ TMRI1/PO4	SCK3	
25		P23			USB0_DPUPE-A	MTIOC3D/ MTCLKD-A/ PO3	TxD3	
26		P22			USB0_DRPD	MTIOC3B/ MTCLKC-A/ TMO0/PO2	SCK0	

3. Address Space

3.1 Address Space

This LSI has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.

Figure 3.1 shows the memory maps in the respective operating modes. Accessible areas will differ according to the operating mode and states of control bits.



Note 1. Rserved areas should not be accessed, since the correct operation of LSI is not guaranteed if they are accessed.
Note 2. The address space in boot mode and user boot mode is the same as the address space in single-chip mode.

Figure 3.1 Memory Map in Each Operating Mode

Table 4.1 List of I/O Registers (Address Order) (11 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 71EFh	ICU	DTC activation enable register 239	DTCER239	8	8	2 ICLK
0008 71F0h	ICU	DTC activation enable register 240	DTCER240	8	8	2 ICLK
0008 71F7h	ICU	DTC activation enable register 247	DTCER247	8	8	2 ICLK
0008 71F8h	ICU	DTC activation enable register 248	DTCER248	8	8	2 ICLK
0008 71FBh	ICU	DTC activation enable register 251	DTCER251	8	8	2 ICLK
0008 71FCh	ICU	DTC activation enable register 252	DTCER252	8	8	2 ICLK
0008 7202h	ICU	Interrupt request enable register 02	IER02	8	8	2 ICLK
0008 7203h	ICU	Interrupt request enable register 03	IER03	8	8	2 ICLK
0008 7204h	ICU	Interrupt request enable register 04	IER04	8	8	2 ICLK
0008 7205h	ICU	Interrupt request enable register 05	IER05	8	8	2 ICLK
0008 7206h	ICU	Interrupt request enable register 06	IER06	8	8	2 ICLK
0008 7207h	ICU	Interrupt request enable register 07	IER07	8	8	2 ICLK
0008 7208h	ICU	Interrupt request enable register 08	IER08	8	8	2 ICLK
0008 7209h	ICU	Interrupt request enable register 09	IER09	8	8	2 ICLK
0008 720Bh	ICU	Interrupt request enable register 0B	IER0B	8	8	2 ICLK
0008 720Ch	ICU	Interrupt request enable register 0C	IER0C	8	8	2 ICLK
0008 720Eh	ICU	Interrupt request enable register 0E	IER0E	8	8	2 ICLK
0008 720Fh	ICU	Interrupt request enable register 0F	IER0F	8	8	2 ICLK
0008 7210h	ICU	Interrupt request enable register 10	IER10	8	8	2 ICLK
0008 7211h	ICU	Interrupt request enable register 11	IER11	8	8	2 ICLK
0008 7212h	ICU	Interrupt request enable register 12	IER12	8	8	2 ICLK
0008 7213h	ICU	Interrupt request enable register 13	IER13	8	8	2 ICLK
0008 7214h	ICU	Interrupt request enable register 14	IER14	8	8	2 ICLK
0008 7215h	ICU	Interrupt request enable register 15	IER15	8	8	2 ICLK
0008 7216h	ICU	Interrupt request enable register 16	IER16	8	8	2 ICLK
0008 7217h	ICU	Interrupt request enable register 17	IER17	8	8	2 ICLK
0008 7218h	ICU	Interrupt request enable register 18	IER18	8	8	2 ICLK
0008 7219h	ICU	Interrupt request enable register 19	IER19	8	8	2 ICLK
0008 721Ah	ICU	Interrupt request enable register 1A	IER1A	8	8	2 ICLK
0008 721Bh	ICU	Interrupt request enable register 1B	IER1B	8	8	2 ICLK
0008 721Ch	ICU	Interrupt request enable register 1C	IER1C	8	8	2 ICLK
0008 721Dh	ICU	Interrupt request enable register 1D	IER1D	8	8	2 ICLK
0008 721Eh	ICU	Interrupt request enable register 1E	IER1E	8	8	2 ICLK
0008 721Fh	ICU	Interrupt request enable register 1F	IER1F	8	8	2 ICLK
0008 72E0h	ICU	Software interrupt activation register	SWINTR	8	8	2 ICLK
0008 72F0h	ICU	Fast interrupt set register	FIR	16	16	2 ICLK
0008 7300h	ICU	Interrupt source priority register 00	IPR00	8	8	2 ICLK
0008 7301h	ICU	Interrupt source priority register 01	IPR01	8	8	2 ICLK
0008 7302h	ICU	Interrupt source priority register 02	IPR02	8	8	2 ICLK
0008 7303h	ICU	Interrupt source priority register 03	IPR03	8	8	2 ICLK
0008 7304h	ICU	Interrupt source priority register 04	IPR04	8	8	2 ICLK
0008 7305h	ICU	Interrupt source priority register 05	IPR05	8	8	2 ICLK
0008 7306h	ICU	Interrupt source priority register 06	IPR06	8	8	2 ICLK
0008 7307h	ICU	Interrupt source priority register 07	IPR07	8	8	2 ICLK
0008 7308h	ICU	Interrupt source priority register 08	IPR08	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (16 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 8209h	TMR1	Timer counter	TCNT	8	8	2 to 3 PCLK*8
0008 820Ah	TMR0	Timer counter control register	TCCR	8	8	2 to 3 PCLK*8
0008 820Bh	TMR1	Timer counter control register	TCCR	8	8	2 to 3 PCLK*8
0008 8204h	TMR01	Time constant register A	TCORA	16	16	2 to 3 PCLK*8
0008 8206h	TMR01	Time constant register B	TCORB	16	16	2 to 3 PCLK*8
0008 8208h	TMR01	Timer counter	TCNT	16	16	2 to 3 PCLK*8
0008 820Ah	TMR01	Timer counter control register	TCCR	16	16	2 to 3 PCLK*8
0008 8210h	TMR2	Timer control register	TCR	8	8	2 to 3 PCLK*8
0008 8211h	TMR3	Timer control register	TCR	8	8	2 to 3 PCLK*8
0008 8212h	TMR2	Timer control/status register	TCSR	8	8	2 to 3 PCLK*8
0008 8213h	TMR3	Timer control/status register	TCSR	8	8	2 to 3 PCLK*8
0008 8214h	TMR2	Time constant register A	TCORA	8	8	2 to 3 PCLK*8
0008 8215h	TMR3	Time constant register A	TCORA	8	8	2 to 3 PCLK*8
0008 8216h	TMR2	Time constant register B	TCORB	8	8	2 to 3 PCLK*8
0008 8217h	TMR3	Time constant register B	TCORB	8	8	2 to 3 PCLK*8
0008 8218h	TMR2	Timer counter	TCNT	8	8	2 to 3 PCLK*8
0008 8219h	TMR3	Timer counter	TCNT	8	8	2 to 3 PCLK*8
0008 821Ah	TMR2	Timer counter control register	TCCR	8	8	2 to 3 PCLK*8
0008 821Bh	TMR3	Timer counter control register	TCCR	8	8	2 to 3 PCLK*8
0008 8214h	TMR23	Time constant register A	TCORA	16	16	2 to 3 PCLK*8
0008 8216h	TMR23	Time constant register B	TCORB	16	16	2 to 3 PCLK*8
0008 8218h	TMR23	Timer counter	TCNT	16	16	2 to 3 PCLK*8
0008 821Ah	TMR23	Timer counter control register	TCCR	16	16	2 to 3 PCLK*8
0008 8240h	SCI0	Serial mode register	SMR	8	8	2 to 3 PCLK*8
0008 8241h	SCI0	Bit rate register	BRR	8	8	2 to 3 PCLK*8
0008 8242h	SCI0	Serial control register	SCR	8	8	2 to 3 PCLK*8
0008 8243h	SCI0	Transmit data register	TDR	8	8	2 to 3 PCLK*8
0008 8244h	SCI0	Serial status register	SSR	8	8	2 to 3 PCLK*8
0008 8245h	SCI0	Receive data register	RDR	8	8	2 to 3 PCLK*8
0008 8246h	SCI0	Smart card mode register	SCMR	8	8	2 to 3 PCLK*8
0008 8247h	SCI0	Serial extended mode register	SEMR	8	8	2 to 3 PCLK*8
0008 8240h	SMCI0	Serial mode register	SMR	8	8	2 to 3 PCLK*8
0008 8241h	SMCI0	Bit rate register	BRR	8	8	2 to 3 PCLK*8
0008 8242h	SMCI0	Serial control register	SCR	8	8	2 to 3 PCLK*8
0008 8243h	SMCI0	Transmit data register	TDR	8	8	2 to 3 PCLK*8
0008 8244h	SMCI0	Serial status register	SSR	8	8	2 to 3 PCLK*8
0008 8245h	SMCI0	Receive data register	RDR	8	8	2 to 3 PCLK*8
0008 8246h	SMCI0	Smart card mode register	SCMR	8	8	2 to 3 PCLK*8
0008 8248h	SCI1	Serial mode register	SMR	8	8	2 to 3 PCLK*8
0008 8249h	SCI1	Bit rate register	BRR	8	8	2 to 3 PCLK*8
0008 824Ah	SCI1	Serial control register	SCR	8	8	2 to 3 PCLK*8
0008 824Bh	SCI1	Transmit data register	TDR	8	8	2 to 3 PCLK*8
0008 824Ch	SCI1	Serial status register	SSR	8	8	2 to 3 PCLK*8
0008 824Dh	SCI1	Receive data register	RDR	8	8	2 to 3 PCLK*8
0008 824Eh	SCI1	Smart card mode register	SCMR	8	8	2 to 3 PCLK*8

Table 4.1 List of I/O Registers (Address Order) (19 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 8310h	RIIC0	I²C bus bit rate low-level register	ICBRL	8	8	2 to 3 PCLK*8
0008 8311h	RIIC0	I²C bus bit rate high-level register	ICBRH	8	8	2 to 3 PCLK*8
0008 8312h	RIIC0	I²C bus transmit data register	ICDRT	8	8	2 to 3 PCLK*8
0008 8313h	RIIC0	I²C bus receive data register	ICDRR	8	8	2 to 3 PCLK*8
0008 8320h	RIIC1	I²C bus control register 1	ICCR1	8	8	2 to 3 PCLK*8
0008 8321h	RIIC1	I²C bus control register 2	ICCR2	8	8	2 to 3 PCLK*8
0008 8322h	RIIC1	I²C bus mode register 1	ICMR1	8	8	2 to 3 PCLK*8
0008 8323h	RIIC1	I²C bus mode register 2	ICMR2	8	8	2 to 3 PCLK*8
0008 8324h	RIIC1	I²C bus mode register 3	ICMR3	8	8	2 to 3 PCLK*8
0008 8325h	RIIC1	I²C bus function enable register	ICFER	8	8	2 to 3 PCLK*8
0008 8326h	RIIC1	I²C bus status enable register	ICSER	8	8	2 to 3 PCLK*8
0008 8327h	RIIC1	I²C bus interrupt enable register	ICIER	8	8	2 to 3 PCLK*8
0008 8328h	RIIC1	I²C bus status register 1	ICSR1	8	8	2 to 3 PCLK*8
0008 8329h	RIIC1	I²C bus status register 2	ICSR2	8	8	2 to 3 PCLK*8
0008 832Ah	RIIC1	Slave address register L0	SARL0	8	8	2 to 3 PCLK*8
0008 832Ah	RIIC1	Timeout internal counter	TMOCNT	16	16	2 to 3 PCLK*8
0008 832Ah	RIIC1	Timeout internal counter L	TMOCNTL	8	8	2 to 3 PCLK*8
0008 832Bh	RIIC1	Slave address register U0	SARU0	8	8	2 to 3 PCLK*8
0008 832Bh	RIIC1	Timeout internal counter U	TMOCNTU		8	2 to 3 PCLK*8
0008 832Ch	RIIC1	Slave address register L1	SARL1	8	8	2 to 3 PCLK*8
0008 832Dh	RIIC1	Slave address register U1	SARU1	8	8	2 to 3 PCLK*8
0008 832Eh	RIIC1	Slave address register L2	SARL2	8	8	2 to 3 PCLK*8
0008 832Fh	RIIC1	Slave address register U2	SARU2	8	8	2 to 3 PCLK*8
0008 8330h	RIIC1	I²C bus bit rate low-level register	ICBRL	8	8	2 to 3 PCLK*8
0008 8331h	RIIC1	I²C bus bit rate high-level register	ICBRH	8	8	2 to 3 PCLK*8
0008 8332h	RIIC1	I²C bus transmit data register	ICDRT	8	8	2 to 3 PCLK*8
0008 8333h	RIIC1	I²C bus receive data register	ICDRR	8	8	2 to 3 PCLK*8
0008 8380h	RSPI0	RSPI control register	SPCR	8	8	2 to 3 PCLK*8
0008 8381h	RSPI0	RSPI slave select polarity register	SSLP	8	8	2 to 3 PCLK*8
0008 8382h	RSPI0	RSPI pin control register	SPPCR	8	8	2 to 3 PCLK*8
0008 8383h	RSPI0	RSPI status register	SPSR	8	8	2 to 3 PCLK*8
0008 8384h	RSPI0	RSPI data register	SPDR	32	16, 32	2 to 3 PCLK*8
0008 8388h	RSPI0	RSPI sequence control register	SPSCR	8	8	2 to 3 PCLK*8
0008 8389h	RSPI0	RSPI sequence status register	SPSSR	8	8	2 to 3 PCLK*8
0008 838Ah	RSPI0	RSPI bit rate register	SPBR	8	8	2 to 3 PCLK*8
0008 838Bh	RSPI0	RSPI data control register	SPDCR	8	8	2 to 3 PCLK*8
0008 838Ch	RSPI0	RSPI clock delay register	SPCKD	8	8	2 to 3 PCLK*8
0008 838Dh	RSPI0	RSPI slave select negation delay register	SSLND	8	8	2 to 3 PCLK*8
0008 838Eh	RSPI0	RSPI next-access delay register	SPND	8	8	2 to 3 PCLK*8
0008 838Fh	RSPI0	RSPI control register 2	SPCR2	8	8	2 to 3 PCLK*8
0008 8390h	RSPI0	RSPI command register 0	SPCMD0	16	16	2 to 3 PCLK*8
0008 8392h	RSPI0	RSPI command register 1	SPCMD1	16	16	2 to 3 PCLK*8
0008 8394h	RSPI0	RSPI command register 2	SPCMD2	16	16	2 to 3 PCLK*8
0008 8396h	RSPI0	RSPI command register 3	SPCMD3	16	16	2 to 3 PCLK*8
0008 8398h	RSPI0	RSPI command register 4	SPCMD4	16	16	2 to 3 PCLK*8

Table 4.1 List of I/O Registers (Address Order) (32 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000A 00D4h	USB0	Device address 2 configuration register	DEVADD2	16	16	at least 9 PCLK*9
000A 00D6h	USB0	Device address 3 configuration register	DEVADD3	16	16	at least 9 PCLK*9
000A 00D8h	USB0	Device address 4 configuration register	DEVADD4	16	16	at least 9 PCLK*9
000A 00DAh	USB0	Device address 5 configuration register	DEVADD5	16	16	at least 9 PCLK*9
000A 0200h	USB1	System configuration control register	SYSCFG	16	16	3 to 4 PCLK*8
000A 0204h	USB1	System configuration status register 0	SYSSTS0	16	16	at least 9 PCLK*9
000A 0208h	USB1	Device state control register 0	DVSTCTR0	16	16	at least 9 PCLK*9
000A 0214h	USB1	CFIFO port register	CFIFO	16	8, 16	3 to 4 PCLK*8
000A 0218h	USB1	D0FIFO port register	D0FIFO	16	8, 16	3 to 4 PCLK*8
000A 021Ch	USB1	D1FIFO port register	D1FIFO	16	8, 16	3 to 4 PCLK*8
000A 0220h	USB1	CFIFO port select register	CFIFOSEL	16	16	3 to 4 PCLK*8
000A 0222h	USB1	CFIFO port control register	CFIFOCTR	16	16	3 to 4 PCLK*8
000A 0228h	USB1	D0FIFO port select register	D0FIFOSEL	16	16	3 to 4 PCLK*8
000A 022Ah	USB1	D0FIFO port control register	D0FIFOCTR	16	16	3 to 4 PCLK*8
000A 022Ch	USB1	D1FIFO port select register	D1FIFOSEL	16	16	3 to 4 PCLK*8
000A 022Eh	USB1	D1FIFO port control register	D1FIFOCTR	16	16	3 to 4 PCLK*8
000A 0230h	USB1	Interrupt enable register 0	INTENB0	16	16	at least 9 PCLK*9
000A 0232h	USB1	Interrupt enable register 1	INTENB1	16	16	at least 9 PCLK*9
000A 0236h	USB1	BRDY interrupt enable register	BRDYENB	16	16	at least 9 PCLK*9
000A 0238h	USB1	NRDY interrupt enable register	NRDYENB	16	16	at least 9 PCLK*9
000A 023Ah	USB1	BEMP interrupt enable register	BEMPENB	16	16	at least 9 PCLK*9
000A 023Ch	USB1	SOF output configuration register	SOFCFG	16	16	at least 9 PCLK*9
000A 0240h	USB1	Interrupt status register 0	INTSTS0	16	16	at least 9 PCLK*9
000A 0242h	USB1	Interrupt status register 1	INTSTS1	16	16	at least 9 PCLK*9
000A 0246h	USB1	BRDY interrupt status register	BRDYSTS	16	16	at least 9 PCLK*9
000A 0248h	USB1	NRDY interrupt status register	NRDYSTS	16	16	at least 9 PCLK*9
000A 024Ah	USB1	BEMP interrupt status register	BEMPSTS	16	16	at least 9 PCLK*9
000A 024Ch	USB1	Frame number register	FRMNUM	16	16	at least 9 PCLK*9
000A 024Eh	USB1	Device state change register	DVCHGR	16	16	at least 9 PCLK*9
000A 0250h	USB1	USB address register	USBADDR	16	16	at least 9 PCLK*9

Table 5.4 DC Characteristics (3)

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
T_a = -40 to +85°C

Item					Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Supply current*2	In operation	Max.*3			I_{CC}*4	—	—	100	mA	ICLK = 100 MHz PCLK = 50 MHz BCLK = 50 MHz
		Normal operation	Peripheral function: Clocks supplied*5			—	48	—		
			Peripheral function: Clocks not supplied*5			—	35	—		
		Increased by BGO operation*6				—	15	—		
	Sleep					—	20	60		
	All-module-clock-stop mode*7					—	14	28		
	Standby mode	Software standby mode				—	0.12	3.0	mA	
		Deep software standby mode	RTC in operation	RAM, USB retained		—	30	206	µA	
				RAM, USB power supply halted		—	26	66	µA	
			RTC halted	RAM, USB retained		—	25	200	µA	
				RAM, USB power supply halted		—	21	60	µA	
Analog power supply current	During 12-bit A/D conversion (per unit)				AI_{CC}	—	2.5	3.0	mA	
	During 10-bit A/D conversion (per unit)					—	0.8	1.2	mA	
	During D/A conversion (per channel)					—	0.3	2.0	µA	
	Idle (all units)					—	30	35	µA	
	During A/D or D/A standby (all units)					—	0.1	4.0	µA	
Reference power supply current	During 12-bit A/D conversion (per unit)				AI_{CC}	—	0.5	0.7	mA	
	During 10-bit A/D conversion (per unit)					—	0.06	0.1	mA	
	During D/A conversion (per channel)					—	0.6	1.0	mA	
	Idle (all units)					—	0.4	0.6	mA	
	During A/D or D/A standby (all units)					—	0.1	2.0	µA	
RAM standby voltage					V_{RAM}	2.48	—	—	V	
VCC rising gradient					SVCC	—	—	20	ms/V	

Note 1. The V_{IH} characteristic of the pins multiplexed with 5-V tolerant ports 00 to 02, 07, 12, 13, 16, 17, 20, 21, and 33 is the same as the V_{IH} characteristic of 5-V tolerant ports.
Note 2. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 3. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
Note 4. ICC depends on f (ICLK) as follows. (ICLK: PCLK: BCLK: BCLK pin = 8 : 4: 8: 4)
ICC max. = 0.89 x f + 11 (max.)
ICC typ. = 0.43 x f + 5 (normal operation, peripheral function: clocks supplied)
ICC typ. = 0.30 x f + 5 (normal operation, peripheral function: clocks not supplied)
ICC max. = 0.48 x f + 12 (sleep mode)
Note 5. This does not include the BGO operation.
Note 6. Incremented if data is written to or erased from the ROM or data flash for data storage during the program execution.
Note 7. The values are for reference.

5.3.1 Clock Timing

Table 5.8 Clock Timing

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
T_a = -40 to +85°C

Item	Symbol	Min.	Max.	Unit	Test Conditions
BCLK pin output cycle time [176-pin LFBGA/145-pin TFLGA/144-pin LQFP]	t_{Bcyc}	20	125	ns	Figure 5.1
BCLK pin output cycle time [100-pin LQFP/85-pin TFLGA]	t_{Bcyc}	40	125	ns	
BCLK pin output high pulse width	t_{CH}	5	—	ns	
BCLK pin output low pulse width	t_{CL}	5	—	ns	
BCLK pin output rising time	t_{Cr}	—	5	ns	
BCLK pin output falling time	t_{Cf}	—	5	ns	
SDCLK pin output cycle time	t_{SDcyc}	20	125	ns	
SDCLK pin output high pulse width	t_{CH}	5	—	ns	
SDCLK pin output low pulse width	t_{CL}	5	—	ns	
SDCLK pin output rising time	t_{Cr}	—	5	ns	
SDCLK pin output falling time	t_{Cf}	—	5	ns	
Oscillation settling time after reset (crystal)	t_{OSC1}	10	—	ms	Figure 5.2
Oscillation settling time after leaving software standby mode (crystal)	t_{OSC2}	10	—	ms	Figure 5.3
Oscillation settling time after leaving deep software standby mode (crystal)	t_{OSC3}	10	—	ms	Figure 5.4
EXTAL external clock output delay settling time	t_{DEXT}	1	—	ms	Figure 5.2
EXTAL external clock input low pulse width	t_{EXL}	30.71	—	ns	Figure 5.5
EXTAL external clock input high pulse width	t_{EXH}	30.71	—	ns	
EXTAL external clock rising time	t_{EXr}	—	5	ns	
EXTAL external clock falling time	t_{EXf}	—	5	ns	
XCIN sub-clock oscillation settling time	t_{SUBOSC}	2	—	s	Figure 5.6
XCIN sub-clock oscillation frequency	f_{SUB}	32.768	—	kHz	
On-chip oscillator (IWDTCLK) oscillation frequency	$f_{IWDTCLK}$	62.5	187.5	kHz	

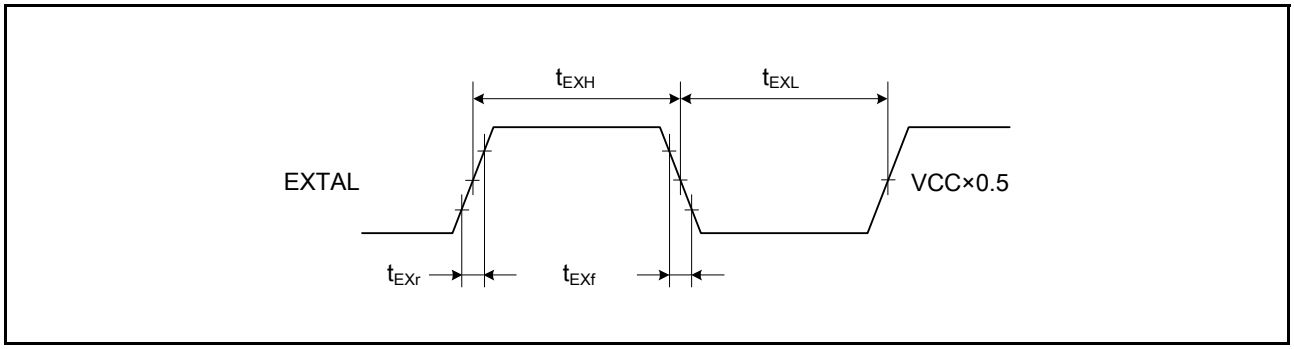


Figure 5.5 EXTAL External Input Clock Timing

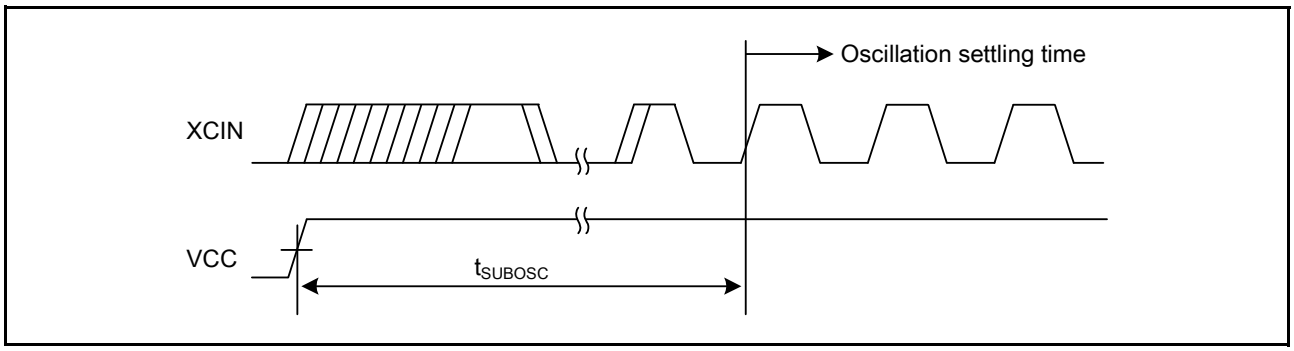


Figure 5.6 XCIN Sub-Clock Oscillation Settling Time

5.5 A/D Conversion Characteristics

Table 5.20 10-Bit A/D Conversion Characteristics

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
PCLK = 8 to 50 MHz
T_a = -40 to +85°C

Item			Min.	Typ.	Max.	Unit	Test Conditions
Resolution			10	10	10	bits	
Conversion time*1 (PCLK = 50-MHz operation)	With 0.1-µF external capacitor	When the capacitor is charged enough*2	0.8 (0.3)*3	—	—	µs	Sampling 15 states
	Without external capacitor	Permissible signal source impedance (max.) = 1.0 kΩ	1.0 (0.5)*3	—	—		Sampling 25 states
		Permissible signal source impedance (max.) = 5.0 kΩ	2.6 (2.1)*3	—	—		Sampling 105 states
Analog input capacitance			—	—	6.0	pF	
INL integral nonlinearity error			—	±1.5	±3.0	LSB	
Offset error			—	±1.5	±3.0	LSB	
Full-scale error			—	±1.5	±3.0	LSB	
Quantization error			—	±0.5	—	LSB	
Absolute accuracy			—	±1.5	±3.0	LSB	
DNL differential nonlinearity error			—	±0.5	±1.0	LSB	

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.
Note 2. The scanning is not supported.
Note 3. The value in parentheses indicates the sampling time.

Table 5.21 12-Bit A/D Conversion Characteristics

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
PCLK = 8 to 50 MHz
T_a = -40 to +85°C

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	12	12	12	bits	
Conversion time*1	1.0	—	—	µs	AVCC ≥ 3.0
	2.0	—	—	µs	AVCC ≥ 2.7
Analog input capacitance	—	—	30	pF	
Offset error	—	±2.0	±7.5	LSB	
Full-scale error	—	±2.0	±7.5	LSB	
Quantization error	—	±0.5	—	LSB	
Absolute accuracy	—	±2.5	±8.0	LSB	
Nonlinearity error	—	±2.0	±4.0	LSB	

Note 1. The time conversion takes is the sum of the sampling interval and the time comparison takes (permissible signal-source impedance is up to 1.0 kΩ)

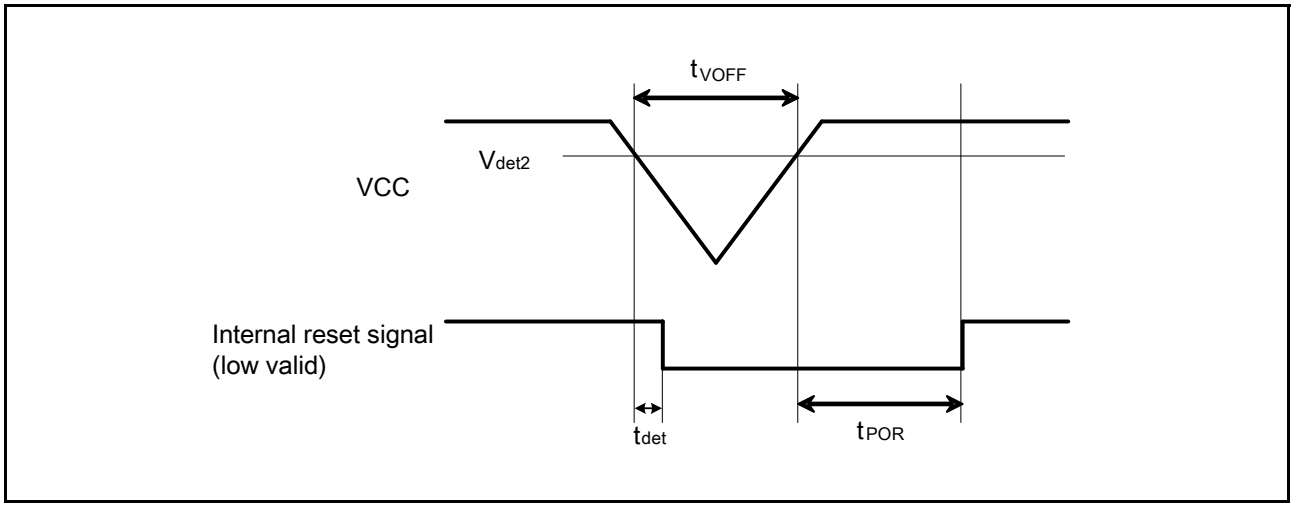


Figure 5.65 Voltage Detection Circuit Timing (Vdet2)

5.9 ROM (Flash Memory for Code Storage) Characteristics

Table 5.25 ROM (Flash Memory for Code Storage) Characteristics (1)

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
Temperature range for the programming/erasure operation: T_a = -40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Rewrite/erase cycle*1	N_{PEC}	1000	—	—	Times	
Data hold time	t_{DRP}	30*2	—	—	Year	T_a = +85°C

Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 256-byte programming is performed 16 times for different addresses in 4-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. The result obtained from the reliability test.

Table 5.26 ROM (Flash Memory for Code Storage) Characteristics (2)

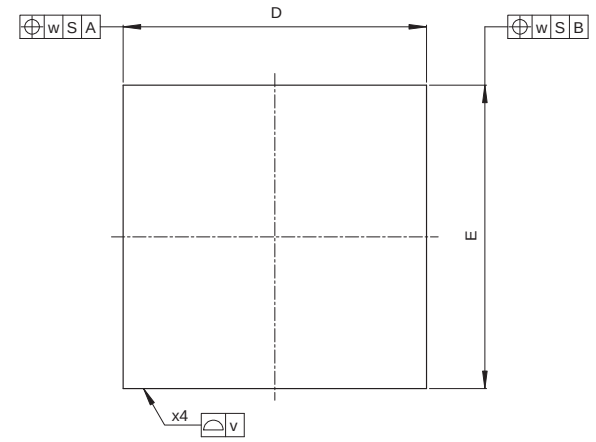
Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
Temperature range for the programming/erasure operation: T_a = -40 to +85°C

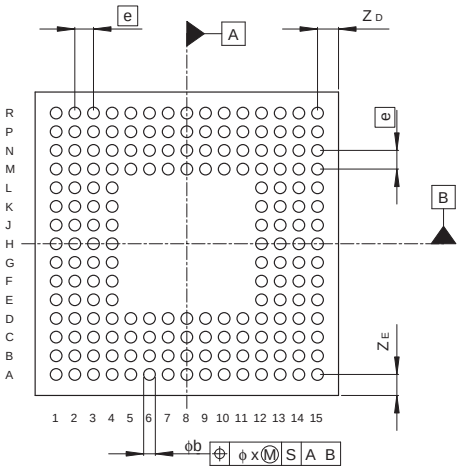
Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Programming time	256 bytes	t_{P256}	—	2	12	ms	PCLK = 50 MHz $N_{PEC} \leq 100$
	4 Kbytes	t_{P4K}	—	23	50	ms	
	16 Kbytes	t_{P16K}	—	90	200	ms	
	256 byte	t_{P256}	—	2.4	14.4	ms	PCLK = 50 MHz $N_{PEC} > 100$
	4 Kbytes	t_{P4K}	—	27.6	60	ms	
	16 Kbytes	t_{P16K}	—	108	240	ms	
Erasure time	4 Kbytes	t_{E4K}	—	25	60	ms	PCLK = 50 MHz $N_{PEC} \leq 100$
	16 Kbytes	t_{E16K}	—	100	240	ms	
	4 Kbytes	t_{E4K}	—	30	72	ms	PCLK = 50 MHz $N_{PEC} > 100$
	16 Kbytes	t_{E16K}	—	120	288	ms	
Suspend delay time during writing		t_{SPD}	—	—	120	µs	Figure 5.67 PCLK = 50-MHz operation
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	120	µs	
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	1.7	ms	
Suspend delay time during erasing (in erasure priority mode)		t_{SEED}	—	—	1.7	ms	

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in "Packages" on Renesas Electronics Corp website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFBGA176-13x13-0.80	PLBG0176GA-A	BP-176/BP-176V	0.45g





Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	13.0	—
E	—	13.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.40
A_1	0.35	0.40	0.45
e	—	0.80	—
b	0.45	0.50	0.55
x	—	—	0.08
y	—	—	0.10
y_1	—	—	0.2
S_D	—	—	—
S_E	—	—	—
Z_D	—	0.90	—
Z_E	—	0.90	—

Figure A 176-Pin LFBGA (PLBG0176GA-A) Package Dimensions

REVISION HISTORY — RX62N Group, RX621 Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	2011.02.04	—	First Edition issued
1.10	2011.02.10	—	Features reviewed
1.20	2011.06.10		1. Overview
		2 to 5	Table 1.1 Outline of Specification, Description changed
		40 to 46	Table 1.9 Pin Functions, Description changed
			4. I/O Registers
		52 to 86	Table 4.1 List of I/O Registers (Address Order), Description changed
			5. Electrical Characteristics
		90	Table 5.2 DC Characteristics (3) , changed
		111	Figure 5.23 EDACK0 and EDACK1 Single-Address Transfer Timing (for a CS Area), changed
		111	Figure 5.24 EDACK0 and EDACK1 Single-Address Transfer Timing (for SDRAM), changed
1.30	2012.01.11		1. Overview
		2	Table 1.1 Outline of Specifications (1/4), changed, note 1, note 2 deleted
		13	Figure 1.6 Pin Assignment of the 144-Pin LQFP (Assistance Diagram), changed
		15	Figure 1.8 Pin Assignment of the 100-Pin LQFP (Assistance Diagram), changed
		33	Table 1.7 List of Pins and Pin Functions (100-Pin LQFP) (1/4), changed
		37	Table 1.8 List of Pins and Pin Functions (85-Pin TFLGA) (2/3), changed
			4. I/O Registers
		52 to 87	Table 4.1 List of I/O Registers (Address Order), Description changed
			5. Electrical Characteristics
		91	Table 5.4 DC Characteristics (3), specification added
		98	Table 5.9 Control Signal Timing, note changed
		122	Table 5.18 Timing of On-Chip Peripheral Modules (6), conditions changed

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.