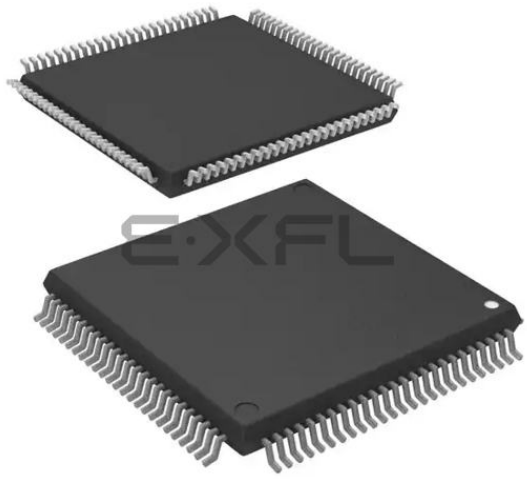
Renesas Electronics America Inc - R5F562N8ADFP#V0 Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	EBI/EMI, I²C, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	72
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562n8adfp-v0

Table 1.1 Outline of Specifications (4 / 4)

Classification	Module/Function	Description
Communication function	I²C bus interfaces	・ 2 channels (100-pin version: 1 channel) ・ Communications formats I²C bus format/SMBus format Master/slave selectable (For multi-master operation)
	CAN module	・ 1 channel ・ 32 mailboxes
	Serial peripheral interfaces	・ 2 channels ・ RSPI transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPI clock (RSPCK) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) Capable of handling serial transfer as a master or slave ・ Data formats Switching between MSB first and LSB first The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) ・ Buffered structure ・ Double buffers for both transmission and reception ・ Max. transfer rate In master mode: 18 Mbps In slave mode: 6.25 Mbps
12-bit A/D converter 10-bit A/D converter		・ 12 bits x 1 unit (1 unit x 8 channels) or 10 bits x 2 units (2 units x 4 channels); 12- and 10-bit A/D converters can be exclusively used. ・ 10- or 12-bit resolution ・ Conversion time: 1.0 μs per channel (in operation with PCLK at 50 MHz) ・ Two operating modes Single mode Scan mode (one-cycle scan mode or continuous scan mode) ・ Sample-and-hold function ・ Three ways to start A/D conversion Conversion can be started by software, a conversion start trigger from a timer (MTU or TMR), or an external trigger signal. ・ Self-diagnostic functions
D/A converter		・ 2 channels (1 channel for 100-pin products) ・ 10-bit resolution ・ Output voltage: 0 V to VREFH
CRC calculator		・ CRC code generation for arbitrary amounts of data in 8-bit units ・ Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$. ・ Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
Operating frequency		8 to 100 MHz
Power supply voltage		VCC = PLLVCC = AVCC = 2.7 to 3.6V, VREFH = 2.7 to AVCC
Operating temperature		–40 to +85°C
Package		176-pin LFBGA (PLBG0176GA-A), 145-pin TFLGA (PTLG0145JB-A), 144-pin LQFP (PLQP0144KA-A), 100-pin LQFP (PLQP0100KB-A)*2 85-pin TFLGA (PTLG0085JA-A)*2,*3

Note 1. For products in the 100-pin LQFP and 85-pin TFLGA, the synchronizing frequency is 8 to 25 MHz.
Note 2. The 100-pin LQFP and 85-pin TFLGA do not support the SDRAM area controller and EXDMA controller.
Note 3. The 85-pin TFLGA does not support the port-output enabling.

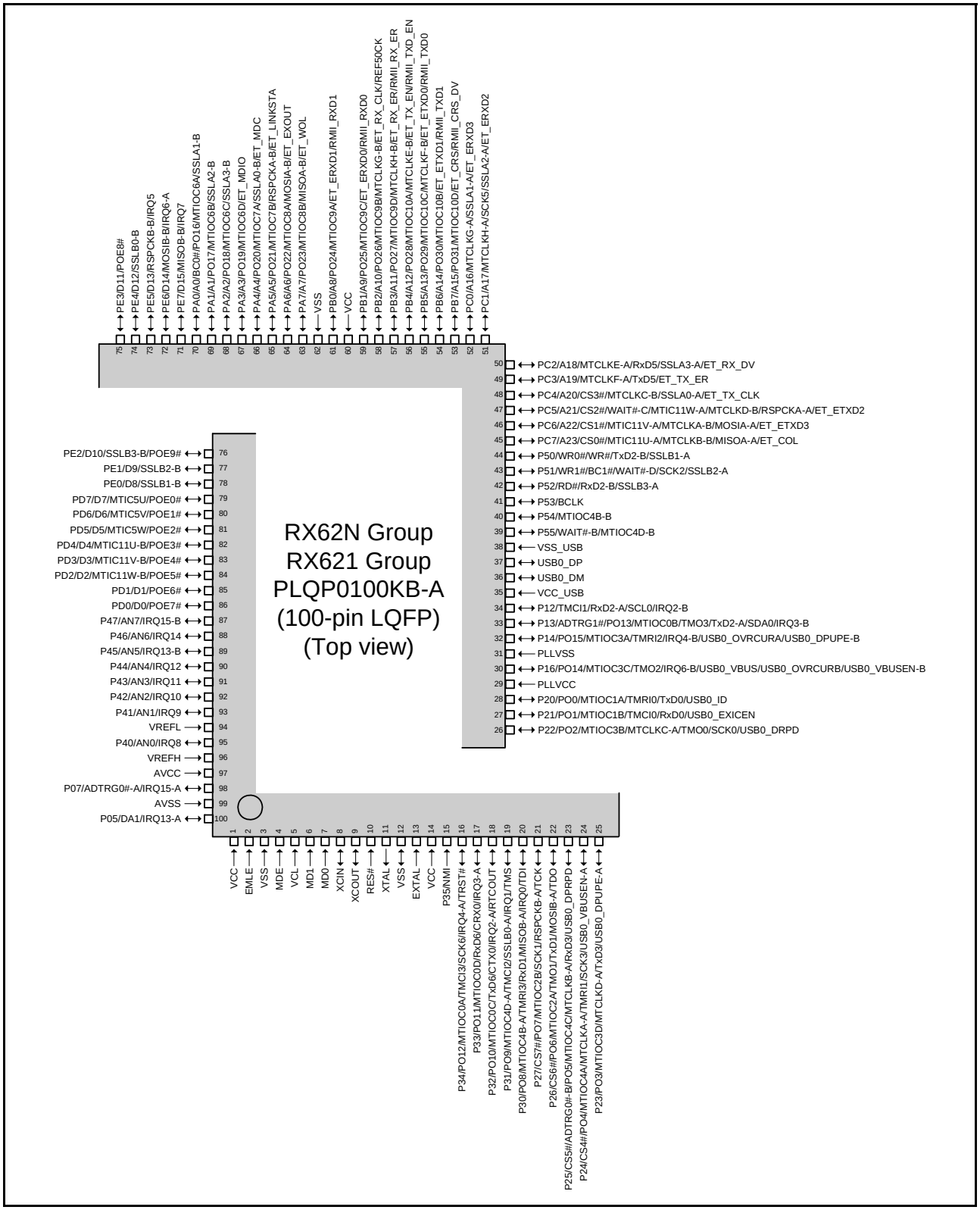


Figure 1.8 Pin Assignment of the 100-Pin LQFP (Assistance Diagram)

Table 1.4 List of Pins and Pin Functions (176-Pin LFBGA) (5 / 6)

Pin No. 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	External Bus EXDMAC	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE, WDT)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
N2		P23	EDACK0-B		USB0_DPUPE-A	MTIOC3D-A/ MTCLKD-A/ PO3	TxD3-B	
N3		P20			USB0_ID	MTIOC1A/ TMRI0-B/ PO0	SDA1/ TxD0	
N4		P17			USB1_VBUS/ USB1_OVRCURB/ USB1_VBUSEN-B	MTIOC3A/ PO15	TxD3-A	IRQ7-B
N5		P15			USB1_OVRCURA/ USB1_DPUPE-B	MTIOC0B/ TMCI2-A/ PO13	SCK3-A	IRQ5-B
N6		P57	WAIT#-A/ WR3#/ BC3#/ EDREQ1-C					
N7		P10			USB1_DPUPE-A	MTIC5W-A/ TMRI3-A		IRQ0-B
N8		P52	RD#				SSLB3-A/ RxD2-B	
N9	VCC							
N10		PC5	A21-A/ CS2#-C/ WAIT#-C	ET_ETXD2		MTIC11W-A/ MTCLKD-B	RSPCKA-A	
N11		PC3	A19-A	ET_TX_ER		MTCLKF-A	TxD5	
N12		PC2	A18-A	ET_RX_DV		MTCLKE-A	SSLA3-A/ RxD5	
N13		P74	CS4#-B	ET_ERXD1/ RMII_RXD1				
N14		P73	CS3#-B	ET_WOL				
N15		PB5	A13			MTIOC10C/ MTCLKF-B/ PO29		
P1		P24	CS4#-C/ EDREQ1-B		USB0_VBUSEN-A	MTIOC4A-A/ MTCLKA-A/ TMRI1/ PO4	SCK3-B	
P2	PLLVCC							
P3		P16			USB0_VBUS/ USB0_OVRCURB/ USB0_VBUSEN-B	MTIOC3C-A/ TMO2/ PO14	RxD3-A	IRQ6-B
P4		P14			USB0_OVRCURA/ USB0_DPUPE-B	TMRI2		IRQ4-B
P5		P13				TMO3	SDA0/ TxD2-A	IRQ3-B/ ADTRG1#
P6	VCC_USB							

Table 1.5 List of Pins and Pin Functions (145-Pin TFLGA) (1 / 5)

Pin No. 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	External Bus EXDMAC	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE, WDT)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
A1	AVSS							
A2	AVCC							
A3	VREFL							
A4		P42						IRQ10-B/AN2
A5		P44						IRQ12/AN4
A6		P47						IRQ15-B/AN7
A7		P91	A17-B					
A8		PD0	D0			POE7#		
A9		PD3	D3			MTIC11V-B/ POE4#		
A10		PD6	D6			MTIC5V/ POE1#		
A11		P60	CS0#-A					
A12		P62	CS2#-A/ RAS#					
A13		P64	CS4#-A/ WE#					
B1		P03						IRQ11-A/DA0
B2		P07						IRQ15-A/ ADTRG0#-A
B3	VREFH							
B4		P40						IRQ8-B/AN0
B5		P45						IRQ13-B/AN5
B6		P90	A16-B					
B7		PD1	D1			POE6#		
B8		PD5	D5			MTIC5W/ POE2#		
B9	VSS							
B10		PE0	D8				SSLB1-B	
B11		PE2	D10			POE9#	SSLB3-B	
B12		PE1	D9				SSLB2-B	
B13		PE4	D12				SSLB0-B	
C1		P01				TMCI0-A	RxD6-A	IRQ9-A
C2		P05						IRQ13-A/DA1
C3	VSS							
C4		P41						IRQ9-B/AN1
C5		P46						IRQ14/AN6
C6		P92	A18-B					
C7		PD2	D2			MTIC11W-B/ POE5#		
C8		PD7	D7			MTIC5U/ POE0#		
C9		P61	CS1#-A/ SDCS#					

Table 1.5 List of Pins and Pin Functions (145-Pin TFLGA) (5 / 5)

Pin No. 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	External Bus EXDMAC	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE, WDT)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
M4		P15				MTIOC0B/ TMCI2-A/ PO13	SCK3-A	IRQ5-B
M5		P14			USB0_OVRCURA/ USB0_DPUPE-B	TMRI2		IRQ4-B
M6	VSS_USB							
M7		P55	WAIT#-B/ EDREQ0-C	ET_EXOUT		MTIOC4D-B		TRDATA3
M8		P50	WR0#/ WR#				SSLB1-A/ TxD2-B	
M9		PC6	A22/CS1#-C	ET_ETXD3		MTIC11V-A/ MTCLKA-B	MOSIA-A	
M10		P80	EDREQ0-A	ET_TX_EN/ RMII_TXD_EN		MTIOC3B-B		TRDATA0
M11		PC2	A18-A	ET_RX_DV		MTCLKE-A	SSLA3-A/ RxD5	
M12		PC1	A17-A	ET_ERXD2		MTCLKH-A	SSLA2-A/ SCK5	
M13	VSS							
N1		P21			USB0_EXICEN	MTIOC1B/ TMCI0-B/ PO1	SCL1/RxD0	
N2		P16			USB0_VBUS/ USB0_OVRCURB/ USB0_VBUSEN-B	MTIOC3C-A/ TMO2/ PO14	RxD3-A	IRQ6-B
N3	PLLVSS							
N4		P13				TMO3	SDA0/ TxD2-A	IRQ3-B/ ADTRG1#
N5					USB0_DM			
N6					USB0_DP			
N7		P54	EDACK0-C	ET_LINKSTA		MTIOC4B-B		TRDATA2
N8		P51	WR1#/BC1#/ WAIT#-D				SSLB2-A/ SCK2	
N9	VCC							
N10		PC5	A21/CS2#-C/ WAIT#-C	ET_ETXD2		MTIC11W-A/ MTCLKD-B	RSPCKA-A	
N11		PC4	A20/CS3#-C	ET_TX_CLK		MTCLKC-B	SSLA0-A	
N12		P76	CS6#-B	ET_RX_CLK/ REF50CK				
N13		P74	CS4#-B	ET_ERXD1/ RMII_RXD1				

Table 1.6 List of Pins and Pin Functions (144-Pin LQFP) (3 / 5)

Pin No. 144-Pin LQFP	Power Supply Clock System Control	I/O Port	External Bus EXDMAC	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE, WDT)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
55		P51	WR1#/BC1#/ WAIT#-D				SSLB2-A/ SCK2	
56		P50	WR0#/ WR#				SSLB1-A/ TxD2-B	
57	VSS							
58		P83	EDACK1-A	ET_CRS/ RMII_CRS_DV		MTIOC4C-B		TRCLK
59	VCC							
60		PC7	A23/ CS0#-B	ET_COL		MTIC11U-A/ MTCLKB-B	MISOA-A	
61		PC6	A22/ CS1#-C	ET_ETXD3		MTIC11V-A/ MTCLKA-B	MOSIA-A	
62		PC5	A21/CS2#-C/ WAIT#-C	ET_ETXD2		MTIC11W-A/ MTCLKD-B	RSPCKA-A	
63		P82	EDREQ1-A	ET_ETXD1/ RMII_TXD1		MTIOC4A-B		TRSYNC
64		P81	EDACK0-A	ET_ETXD0/ RMII_TXD0		MTIOC3D-B		TRDATA1
65		P80	EDREQ0-A	ET_TX_EN/ RMII_TXD_EN		MTIOC3B-B		TRDATA0
66		PC4	A20/CS3#-C	ET_TX_CLK		MTCLKC-B	SSLA0-A	
67		PC3	A19-A	ET_TX_ER		MTCLKF-A	TxD5	
68		P77	CS7#-B	ET_RX_ER/ RMII_RX_ER				
69		P76	CS6#-B	ET_RX_CLK/ REF50CK				
70		PC2	A18-A	ET_RX_DV		MTCLKE-A	SSLA3-A/ RxD5	
71		P75	CS5#-B	ET_ERXD0/ RMII_RXD0				
72		P74	CS4#-B	ET_ERXD1/ RMII_RXD1				
73		PC1	A17-A	ET_ERXD2		MTCLKH-A	SSLA2-A/ SCK5	
74	VCC							
75		PC0	A16-A	ET_ERXD3		MTCLKG-A	SSLA1-A	
76	VSS							
77		P73	CS3#-B	ET_WOL				
78		PB7	A15			MTIOC10D/ PO31		
79		PB6	A14			MTIOC10B/ PO30		
80		PB5	A13			MTIOC10C/ MTCLKF-B/ PO29		
81		PB4	A12			MTIOC10A/ MTCLKE-B/ PO28		

Table 1.7 List of Pins and Pin Functions (100-Pin LQFP) (3 / 4)

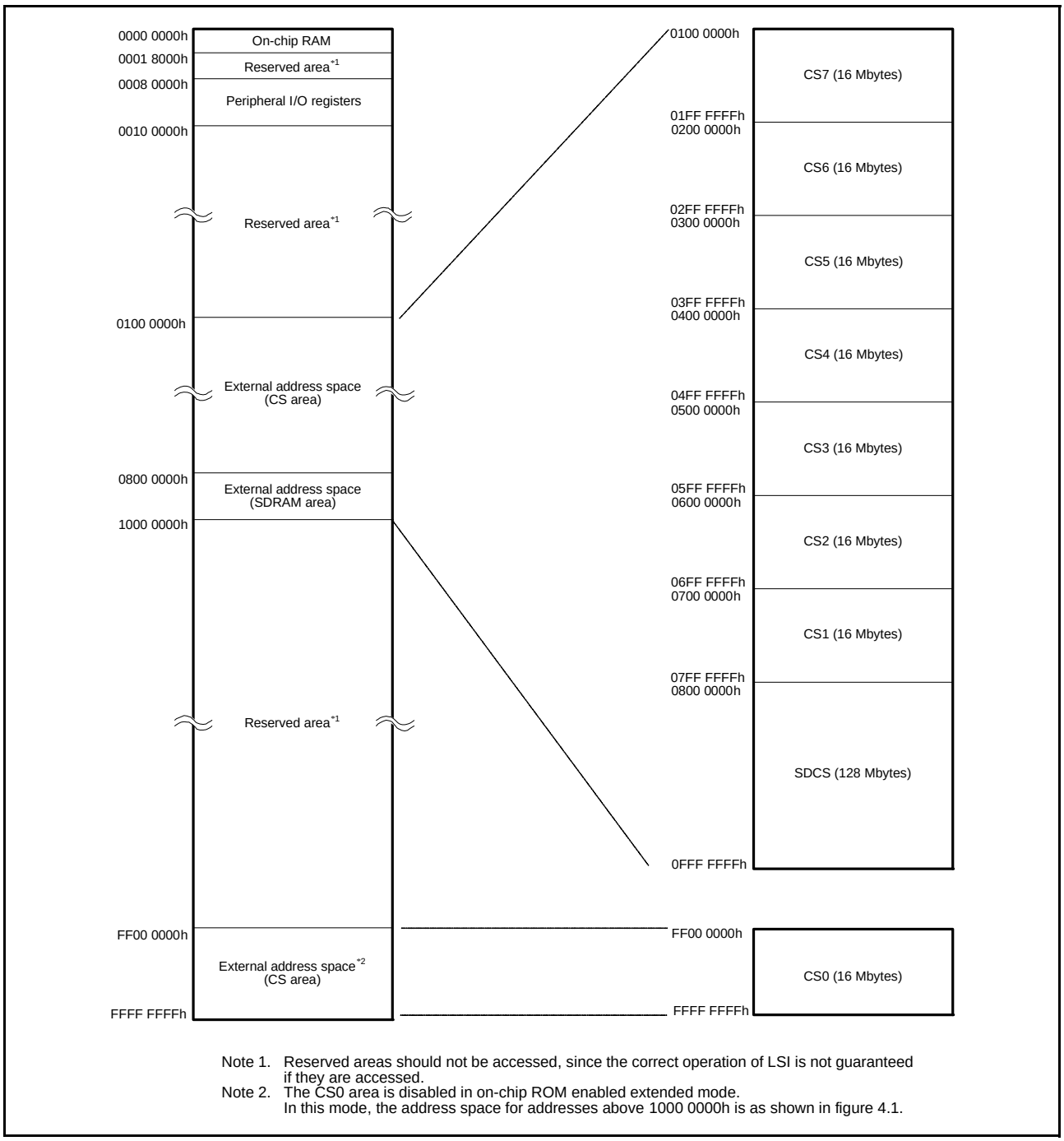
Pin No. 100-Pin LQFP	Power Supply Clock System Control	I/O Port	External Bus	ETHERC EDMAC	USB	Timers (MTU, TMR, PPG, POE)	Communi-cation (SCI, CAN, RSPI, RIIC)	Others
53		PB7	A15	ET_CRS/ RMII_CRS_DV		MTIOC10D/ PO31		
54		PB6	A14	ET_ETXD1/ RMII_TXD1		MTIOC10B/ PO30		
55		PB5	A13	ET_ETXD0/ RMII_TXD0		MTIOC10C/ MTCLKF-B/ PO29		
56		PB4	A12	ET_TX_EN/ RMII_TXD_EN		MTIOC10A/ MTCLKE-B/ PO28		
57		PB3	A11	ET_RX_ER/ RMII_RX_ER		MTIOC9D/ MTCLKH-B/ PO27		
58		PB2	A10	ET_RX_CLK/ REF50CK		MTIOC9B/ MTCLKG-B/ PO26		
59		PB1	A9	ET_ERXD0/ RMII_RXD0		MTIOC9C/ PO25		
60	VCC							
61		PB0	A8	ET_ERXD1/ RMII_RXD1		MTIOC9A/ PO24		
62	VSS							
63		PA7	A7	ET_WOL		MTIOC8B/ PO23	MISOA-B	
64		PA6	A6	ET_EXOUT		MTIOC8A/ PO22	MOSIA-B	
65		PA5	A5	ET_LINKSTA		MTIOC7B/ PO21	RSPCKA-B	
66		PA4	A4	ET_MDC		MTIOC7A/ PO20	SSLA0-B	
67		PA3	A3	ET_MDIO		MTIOC6D/ PO19		
68		PA2	A2			MTIOC6C/ PO18	SSLA3-B	
69		PA1	A1			MTIOC6B/ PO17	SSLA2-B	
70		PA0	A0/BC0#			MTIOC6A/ PO16	SSLA1-B	
71		PE7	D15				MISOB-B	IRQ7
72		PE6	D14				MOSIB-B	IRQ6-A
73		PE5	D13				RSPCKB-B	IRQ5
74		PE4	D12				SSLB0-B	
75		PE3	D11			POE8#		
76		PE2	D10			POE9#	SSLB3-B	
77		PE1	D9				SSLB2-B	
78		PE0	D8				SSLB1-B	
79		PD7	D7			MTIC5U/ POE0#		

3.2 External Address Space

The external address space is classified into CS areas (CS0 to CS7) and SDRAM area (SDCS).

The CS area is divided into up to 8 areas (CS0 to CS7), each corresponding to the CSi# signal output from a CSi# (i = 0 to 7) pin.

Figure 3.2 shows the address ranges corresponding to the individual CS areas (CS0 to CS7) and SDRAM area (SDCS) in on-chip ROM disabled extended mode.



Note 1. Reserved areas should not be accessed, since the correct operation of LSI is not guaranteed if they are accessed.
Note 2. The CS0 area is disabled in on-chip ROM enabled extended mode.
In this mode, the address space for addresses above 1000 0000h is as shown in figure 4.1.

Figure 3.2 Correspondence between External Address Spaces, CS Areas (CS0 to CS7), and SDRAM area (SDCS) (In On-Chip ROM Disabled Extended Mode)

Table 4.1 List of I/O Registers (Address Order) (12 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 730Ch	ICU	Interrupt source priority register 0C	IPR0C	8	8	2 ICLK
0008 730Dh	ICU	Interrupt source priority register 0D	IPR0D	8	8	2 ICLK
0008 730Eh	ICU	Interrupt source priority register 0E	IPR0E	8	8	2 ICLK
0008 7310h	ICU	Interrupt source priority register 10	IPR10	8	8	2 ICLK
0008 7311h	ICU	Interrupt source priority register 11	IPR11	8	8	2 ICLK
0008 7312h	ICU	Interrupt source priority register 12	IPR12	8	8	2 ICLK
0008 7314h	ICU	Interrupt source priority register 14	IPR14	8	8	2 ICLK
0008 7315h	ICU	Interrupt source priority register 15	IPR15	8	8	2 ICLK
0008 7318h	ICU	Interrupt source priority register 18	IPR18	8	8	2 ICLK
0008 731Eh	ICU	Interrupt source priority register 1E	IPR1E	8	8	2 ICLK
0008 731Fh	ICU	Interrupt source priority register 1F	IPR1F	8	8	2 ICLK
0008 7320h	ICU	Interrupt source priority register 20	IPR20	8	8	2 ICLK
0008 7321h	ICU	Interrupt source priority register 21	IPR21	8	8	2 ICLK
0008 7322h	ICU	Interrupt source priority register 22	IPR22	8	8	2 ICLK
0008 7323h	ICU	Interrupt source priority register 23	IPR23	8	8	2 ICLK
0008 7324h	ICU	Interrupt source priority register 24	IPR24	8	8	2 ICLK
0008 7325h	ICU	Interrupt source priority register 25	IPR25	8	8	2 ICLK
0008 7326h	ICU	Interrupt source priority register 26	IPR26	8	8	2 ICLK
0008 7327h	ICU	Interrupt source priority register 27	IPR27	8	8	2 ICLK
0008 7328h	ICU	Interrupt source priority register 28	IPR28	8	8	2 ICLK
0008 7329h	ICU	Interrupt source priority register 29	IPR29	8	8	2 ICLK
0008 732Ah	ICU	Interrupt source priority register 2A	IPR2A	8	8	2 ICLK
0008 732Bh	ICU	Interrupt source priority register 2B	IPR2B	8	8	2 ICLK
0008 732Ch	ICU	Interrupt source priority register 2C	IPR2C	8	8	2 ICLK
0008 732Dh	ICU	Interrupt source priority register 2D	IPR2D	8	8	2 ICLK
0008 732Eh	ICU	Interrupt source priority register 2E	IPR2E	8	8	2 ICLK
0008 732Fh	ICU	Interrupt source priority register 2F	IPR2F	8	8	2 ICLK
0008 733Ah	ICU	Interrupt source priority register 3A	IPR3A	8	8	2 ICLK
0008 733Bh	ICU	Interrupt source priority register 3B	IPR3B	8	8	2 ICLK
0008 733Ch	ICU	Interrupt source priority register 3C	IPR3C	8	8	2 ICLK
0008 7340h	ICU	Interrupt source priority register 40	IPR40	8	8	2 ICLK
0008 7344h	ICU	Interrupt source priority register 44	IPR44	8	8	2 ICLK
0008 7345h	ICU	Interrupt source priority register 45	IPR45	8	8	2 ICLK
0008 7348h	ICU	Interrupt source priority register 48	IPR48	8	8	2 ICLK
0008 7351h	ICU	Interrupt source priority register 51	IPR51	8	8	2 ICLK
0008 7352h	ICU	Interrupt source priority register 52	IPR52	8	8	2 ICLK
0008 7353h	ICU	Interrupt source priority register 53	IPR53	8	8	2 ICLK
0008 7354h	ICU	Interrupt source priority register 54	IPR54	8	8	2 ICLK
0008 7355h	ICU	Interrupt source priority register 55	IPR55	8	8	2 ICLK
0008 7356h	ICU	Interrupt source priority register 56	IPR56	8	8	2 ICLK
0008 7357h	ICU	Interrupt source priority register 57	IPR57	8	8	2 ICLK
0008 7358h	ICU	Interrupt source priority register 58	IPR58	8	8	2 ICLK
0008 7359h	ICU	Interrupt source priority register 59	IPR59	8	8	2 ICLK
0008 735Ah	ICU	Interrupt source priority register 5A	IPR5A	8	8	2 ICLK
0008 735Bh	ICU	Interrupt source priority register 5B	IPR5B	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (22 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 8726h	MTU0	Timer buffer operation transfer mode register	TBTM	8	8	2 to 3 PCLK*8
0008 8780h	MTU1	Timer control register	TCR	8	8	2 to 3 PCLK*8
0008 8781h	MTU1	Timer mode register	TMDR	8	8	2 to 3 PCLK*8
0008 8782h	MTU1	Timer I/O control register	TIOR	8	8	2 to 3 PCLK*8
0008 8784h	MTU1	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK*8
0008 8785h	MTU1	Timer status register	TSR	8	8	2 to 3 PCLK*8
0008 8786h	MTU1	Timer counter	TCNT	16	16	2 to 3 PCLK*8
0008 8788h	MTU1	Timer general register A	TGRA	16	16	2 to 3 PCLK*8
0008 878Ah	MTU1	Timer general register B	TGRB	16	16	2 to 3 PCLK*8
0008 8790h	MTU1	Timer input capture control register	TICCR	8	8	2 to 3 PCLK*8
0008 8800h	MTU2	Timer control register	TCR	8	8	2 to 3 PCLK*8
0008 8801h	MTU2	Timer mode register	TMDR	8	8	2 to 3 PCLK*8
0008 8802h	MTU2	Timer I/O control register	TIOR	8	8	2 to 3 PCLK*8
0008 8804h	MTU2	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK*8
0008 8805h	MTU2	Timer status register	TSR	8	8	2 to 3 PCLK*8
0008 8806h	MTU2	Timer counter	TCNT	16	16	2 to 3 PCLK*8
0008 8808h	MTU2	Timer general register A	TGRA	16	16	2 to 3 PCLK*8
0008 880Ah	MTU2	Timer general register B	TGRB	16	16	2 to 3 PCLK*8
0008 8880h	MTU5	Timer counter U	TCNTU	16	16	2 to 3 PCLK*8
0008 8882h	MTU5	Timer general register U	TGRU	16	16	2 to 3 PCLK*8
0008 8884h	MTU5	Timer control register U	TCRU	8	8	2 to 3 PCLK*8
0008 8886h	MTU5	Timer I/O control register U	TIORU	8	8	2 to 3 PCLK*8
0008 8890h	MTU5	Timer counter V	TCNTV	16	16	2 to 3 PCLK*8
0008 8892h	MTU5	Timer general register V	TGRV	16	16	2 to 3 PCLK*8
0008 8894h	MTU5	Timer control register V	TCRV	8	8	2 to 3 PCLK*8
0008 8896h	MTU5	Timer I/O control register V	TIORV	8	8	2 to 3 PCLK*8
0008 88A0h	MTU5	Timer counter W	TCNTW	16	16	2 to 3 PCLK*8
0008 88A2h	MTU5	Timer general register W	TGRW	16	16	2 to 3 PCLK*8
0008 88A4h	MTU5	Timer control register W	TCRW	8	8	2 to 3 PCLK*8
0008 88A6h	MTU5	Timer I/O control register W	TIORW	8	8	2 to 3 PCLK*8
0008 88B2h	MTU5	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK*8
0008 88B4h	MTU5	Timer start register	TSTR	8	8	2 to 3 PCLK*8
0008 88B6h	MTU5	Timer compare match clear register	TCNTCMPCLR	8	8	2 to 3 PCLK*8
0008 8900h	POE	Input level control/status register 1	ICSR1	16	16	2 to 3 PCLK*8
0008 8902h	POE	Output level control/status register 1	OCSR1	16	16	2 to 3 PCLK*8
0008 8904h	POE	Input level control/status register 2	ICSR2	16	16	2 to 3 PCLK*8
0008 8906h	POE	Output level control/status register 2	OCSR2	16	16	2 to 3 PCLK*8
0008 8908h	POE	Input level control/status register 3	ICSR3	16	16	2 to 3 PCLK*8
0008 890Ah	POE	Software port output enable register	SPOER	8	8	2 to 3 PCLK*8
0008 890Bh	POE	Port output enable control register 1	POECR1	8	8	2 to 3 PCLK*8
0008 890Ch	POE	Port output enable control register 2	POECR2	16	16	2 to 3 PCLK*8
0008 890Eh	POE	Input level control/status register 4	ICSR4	16	16	2 to 3 PCLK*8
0008 8A00h	MTU9	Timer control register	TCR	8	8	2 to 3 PCLK*8

Table 4.1 List of I/O Registers (Address Order) (23 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 8A01h	MTU10	Timer control register	TCR	8	8	2 to 3 PCLK*8
0008 8A02h	MTU9	Timer mode register	TMDR	8	8	2 to 3 PCLK*8
0008 8A03h	MTU10	Timer mode register	TMDR	8	8	2 to 3 PCLK*8
0008 8A04h	MTU9	Timer I/O control register H	TIORH	8	8	2 to 3 PCLK*8
0008 8A05h	MTU9	Timer I/O control register L	TIORL	8	8	2 to 3 PCLK*8
0008 8A06h	MTU10	Timer I/O control register H	TIORH	8	8	2 to 3 PCLK*8
0008 8A07h	MTU10	Timer I/O control register L	TIORL	8	8	2 to 3 PCLK*8
0008 8A08h	MTU9	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK*8
0008 8A09h	MTU10	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK*8
0008 8A0Ah	MTUB	Timer output master enable register	TOER	8	8	2 to 3 PCLK*8
0008 8A0Dh	MTUB	Timer gate control register	TGCR	8	8	2 to 3 PCLK*8
0008 8A0Eh	MTUB	Timer output control register 1	TOCR1	8	8	2 to 3 PCLK*8
0008 8A0Fh	MTUB	Timer output control register 2	TOCR2	8	8	2 to 3 PCLK*8
0008 8A10h	MTU9	Timer counter	TCNT	16	16	2 to 3 PCLK*8
0008 8A12h	MTU10	Timer counter	TCNT	16	16	2 to 3 PCLK*8
0008 8A14h	MTUB	Timer cycle data register	TCDR	16	16	2 to 3 PCLK*8
0008 8A16h	MTUB	Timer dead time data register	TDDR	16	16	2 to 3 PCLK*8
0008 8A18h	MTU9	Timer general register A	TGRA	16	16	2 to 3 PCLK*8
0008 8A1Ah	MTU9	Timer general register B	TGRB	16	16	2 to 3 PCLK*8
0008 8A1Ch	MTU10	Timer general register A	TGRA	16	16	2 to 3 PCLK*8
0008 8A1Eh	MTU10	Timer general register B	TGRB	16	16	2 to 3 PCLK*8
0008 8A20h	MTUB	Timer subcounter	TCNTS	16	16	2 to 3 PCLK*8
0008 8A22h	MTUB	MTUB Timer cycle buffer register	TCBR	16	16	2 to 3 PCLK*8
0008 8A24h	MTU9	Timer general register C	TGRC	16	16	2 to 3 PCLK*8
0008 8A26h	MTU9	Timer general register D	TGRD	16	16	2 to 3 PCLK*8
0008 8A28h	MTU10	Timer general register C	TGRC	16	16	2 to 3 PCLK*8
0008 8A2Ah	MTU10	Timer general register D	TGRD	16	16	2 to 3 PCLK*8
0008 8A2Ch	MTU9	Timer status register	TSR	8	8	2 to 3 PCLK*8
0008 8A2Dh	MTU10	Timer status register	TSR	8	8	2 to 3 PCLK*8
0008 8A30h	MTUB	Timer interrupt skipping set register	TITCR	8	8	2 to 3 PCLK*8
0008 8A31h	MTUB	Timer interrupt skipping counter	TITCNT	8	8	2 to 3 PCLK*8
0008 8A32h	MTUB	TUB Timer dead time enable register	TBTER	8	8	2 to 3 PCLK*8
0008 8A34h	MTUB	Timer dead time enable register	TDER	8	8	2 to 3 PCLK*8
0008 8A36h	MTUB	Timer output level buffer register	TOLBR	8	8	2 to 3 PCLK*8
0008 8A38h	MTU9	Timer buffer operation transfer mode register	TBTM	8	8	2 to 3 PCLK*8
0008 8A39h	MTU10	Timer buffer operation transfer mode register	TBTM	8	8	2 to 3 PCLK*8
0008 8A40h	MTU10	Timer A/D converter start request control register	TADCR	16	16	2 to 3 PCLK*8
0008 8A44h	MTU10	Timer A/D converter start request cycle set register A	TADCORA	16	16	2 to 3 PCLK*8
0008 8A46h	MTU10	Timer A/D converter start request cycle set register B	TADCORB	16	16	2 to 3 PCLK*8
0008 8A48h	MTU10	Timer A/D converter start request cycle set buffer register A	TADCOBRA	16	16	2 to 3 PCLK*8

Table 4.1 List of I/O Registers (Address Order) (24 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 8A4Ah	MTU10	Timer A/D converter start request cycle set buffer register B	TADCOBRB	16	16	2 to 3 PCLK*8
0008 8A60h	MTUB	Timer waveform control register	TWCR	8	8	2 to 3 PCLK*8
0008 8A80h	MTUB	Timer start register	TSTR	8	8	2 to 3 PCLK*8
0008 8A81h	MTUB	MTUB Timer synchronous register	TSYR	8	8	2 to 3 PCLK*8
0008 8A84h	MTUB	MTUB Timer read/write enable register	TRWER	8	8	2 to 3 PCLK*8
0008 8B00h	MTU6	Timer control register	TCR	8	8	2 to 3 PCLK*8
0008 8B01h	MTU6	Timer mode register	TMDR	8	8	2 to 3 PCLK*8
0008 8B02h	MTU6	Timer I/O control register H	TIORH	8	8	2 to 3 PCLK*8
0008 8B03h	MTU6	Timer I/O control register L	TIORL	8	8	2 to 3 PCLK*8
0008 8B04h	MTU6	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK*8
0008 8B05h	MTU6	Timer status register	TSR	8	8	2 to 3 PCLK*8
0008 8B06h	MTU6	Timer counter	TCNT	16	16	2 to 3 PCLK*8
0008 8B08h	MTU6	Timer general register A	TGRA	16	16	2 to 3 PCLK*8
0008 8B0Ah	MTU6	Timer general register B	TGRB	16	16	2 to 3 PCLK*8
0008 8B0Ch	MTU6	Timer general register C	TGRC	16	16	2 to 3 PCLK*8
0008 8B0Eh	MTU6	Timer general register D	TGRD	16	16	2 to 3 PCLK*8
0008 8B20h	MTU6	Timer general register E	TGRE	16	16	2 to 3 PCLK*8
0008 8B22h	MTU6	Timer general register F	TGRF	16	16	2 to 3 PCLK*8
0008 8B24h	MTU6	Timer interrupt enable register 2	TIER2	8	8	2 to 3 PCLK*8
0008 8B26h	MTU6	Timer buffer operation transfer mode register	TBTM	8	8	2 to 3 PCLK*8
0008 8B80h	MTU7	Timer control register	TCR	8	8	2 to 3 PCLK*8
0008 8B81h	MTU7	Timer mode register	TMDR	8	8	2 to 3 PCLK*8
0008 8B82h	MTU7	Timer I/O control register	TIOR	8	8	2 to 3 PCLK*8
0008 8B84h	MTU7	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK*8
0008 8B85h	MTU7	Timer status register	TSR	8	8	2 to 3 PCLK*8
0008 8B86h	MTU7	Timer counter	TCNT	16	16	2 to 3 PCLK*8
0008 8B88h	MTU7	Timer general register A	TGRA	16	16	2 to 3 PCLK*8
0008 8B8Ah	MTU7	Timer general register B	TGRB	16	16	2 to 3 PCLK*8
0008 8B90h	MTU7	Timer input capture control register	TICCR	8	8	2 to 3 PCLK*8
0008 8C00h	MTU8	Timer control register	TCR	8	8	2 to 3 PCLK*8
0008 8C01h	MTU8	Timer mode register	TMDR	8	8	2 to 3 PCLK*8
0008 8C02h	MTU8	Timer I/O control register	TIOR	8	8	2 to 3 PCLK*8
0008 8C04h	MTU8	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK*8
0008 8C05h	MTU8	Timer status register	TSR	8	8	2 to 3 PCLK*8
0008 8C06h	MTU8	Timer counter	TCNT	16	16	2 to 3 PCLK*8
0008 8C08h	MTU8	Timer general register A	TGRA	16	16	2 to 3 PCLK*8
0008 8C0Ah	MTU8	Timer general register B	TGRB	16	16	2 to 3 PCLK*8
0008 8C80h	MTU11	Timer counter U	TCNTU	16	16	2 to 3 PCLK*8
0008 8C82h	MTU11	Timer general register U	TGRU	16	16	2 to 3 PCLK*8
0008 8C84h	MTU11	Timer control register U	TCRU	8	8	2 to 3 PCLK*8
0008 8C86h	MTU11	Timer I/O control register U	TIORU	8	8	2 to 3 PCLK*8
0008 8C90h	MTU11	Timer counter V	TCNTV	16	16	2 to 3 PCLK*8
0008 8C92h	MTU11	Timer general register V	TGRV	16	16	2 to 3 PCLK*8

Table 4.1 List of I/O Registers (Address Order) (30 / 36)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000A 0008h	USB0	Device state control register 0	DVSTCTR0	16	16	at least 9 PCLK*9
000A 0014h	USB0	CFIFO port register	CFIFO	16	8, 16	3 to 4 PCLK*8
000A 0018h	USB0	D0FIFO port register	D0FIFO	16	8, 16	3 to 4 PCLK*8
000A 001Ch	USB0	D1FIFO port register	D1FIFO	16	8, 16	3 to 4 PCLK*8
000A 0020h	USB0	CFIFO port select register	CFIFOSEL	16	16	3 to 4 PCLK*8
000A 0022h	USB0	CFIFO port control register	CFIFOCTR	16	16	3 to 4 PCLK*8
000A 0028h	USB0	D0FIFO port select register	D0FIFOSEL	16	16	3 to 4 PCLK*8
000A 002Ah	USB0	D0FIFO port control register	D0FIFOCTR	16	16	3 to 4 PCLK*8
000A 002Ch	USB0	D1FIFO port select register	D1FIFOSEL	16	16	3 to 4 PCLK*8
000A 002Eh	USB0	D1FIFO port control register	D1FIFOCTR	16	16	3 to 4 PCLK*8
000A 0030h	USB0	Interrupt enable register 0	INTENB0	16	16	at least 9 PCLK*9
000A 0032h	USB0	Interrupt enable register 1	INTENB1	16	16	at least 9 PCLK*9
000A 0036h	USB0	BRDY interrupt enable register	BRDYENB	16	16	at least 9 PCLK*9
000A 0038h	USB0	NRDY interrupt enable register	NRDYENB	16	16	at least 9 PCLK*9
000A 003Ah	USB0	BEMP interrupt enable register	BEMPENB	16	16	at least 9 PCLK*9
000A 003Ch	USB0	SOF output configuration register	SOFCFG	16	16	at least 9 PCLK*9
000A 0040h	USB0	Interrupt status register 0	INTSTS0	16	16	at least 9 PCLK*9
000A 0042h	USB0	Interrupt status register 1	INTSTS1	16	16	at least 9 PCLK*9
000A 0046h	USB0	BRDY interrupt enable register	BRDYSTS	16	16	at least 9 PCLK*9
000A 0048h	USB0	NRDY interrupt status register	NRDYSTS	16	16	at least 9 PCLK*9
000A 004Ah	USB0	BEMP interrupt status register	BEMPSTS	16	16	at least 9 PCLK*9
000A 004Ch	USB0	Frame number register	FRMNUM	16	16	at least 9 PCLK*9
000A 004Eh	USB0	Device state change register	DVCHGR	16	16	at least 9 PCLK*9
000A 0050h	USB0	USB address register	USBADDR	16	16	at least 9 PCLK*9
000A 0054h	USB0	USB request type register	USBREQ	16	16	at least 9 PCLK*9
000A 0056h	USB0	USB request value register	USBVAL	16	16	at least 9 PCLK*9
000A 0058h	USB0	USB request index register	USBINDX	16	16	at least 9 PCLK*9
000A 005Ah	USB0	USB request length register	USBLENG	16	16	at least 9 PCLK*9
000A 005Ch	USB0	DCP configuration register	DCPCFG	16	16	at least 9 PCLK*9
000A 005Eh	USB0	DCP maximum packet size register	DCPMAXP	16	16	at least 9 PCLK*9

5.3.2 Control Signal Timing

Table 5.9 Control Signal Timing

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
T_a = -40 to +85°C

Item	Symbol	Min.	Max.	Unit	Test Conditions
RES# pulse width (except for programming or erasure of the ROM or data-flash memory or blank checking of the data-flash memory)	t_{RESW}*1	20	—	t_{Icyc}*3	Figure 5.7
		1.5	—	µs	
Internal reset time*2	t_{RESW2}	35	—	µs	
NMI pulse width	t_{NMIW}	200	—	ns	Figure 5.8
IRQ pulse width	t_{IRQW}	200	—	ns	Figure 5.9

Note 1. Both the time and the number of cycles should satisfy the specifications.
Note 2. This is to specify the FCU reset.
Note 3. t_{Icyc}: ICLK cycles

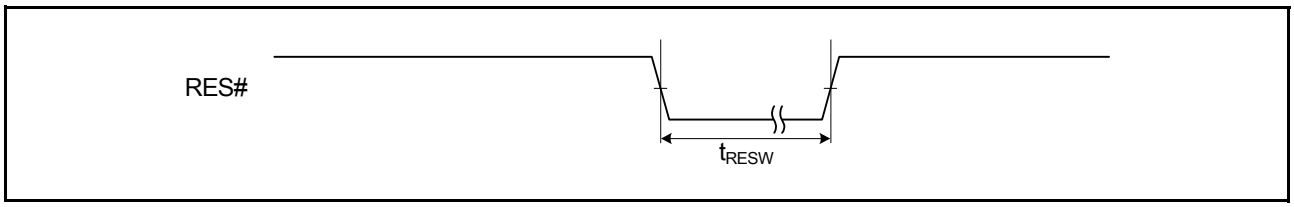


Figure 5.7 Reset Input Timing

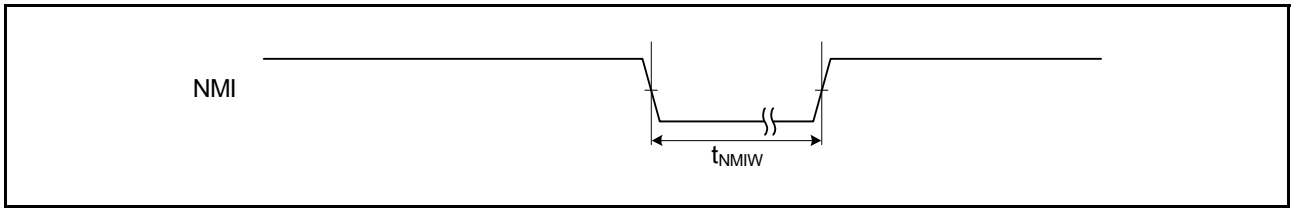


Figure 5.8 NMI Interrupt Input Timing

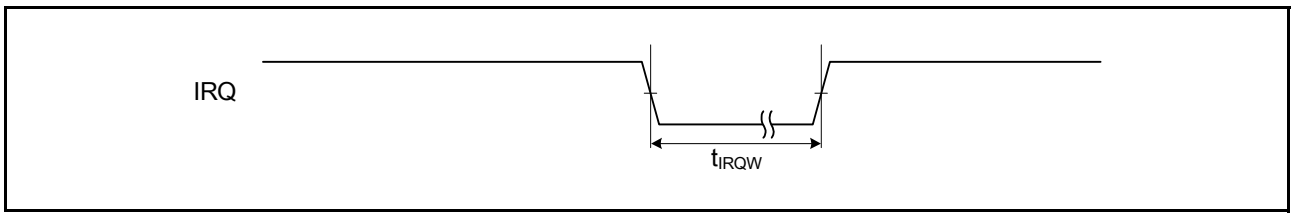


Figure 5.9 IRQ Interrupt Input Timing

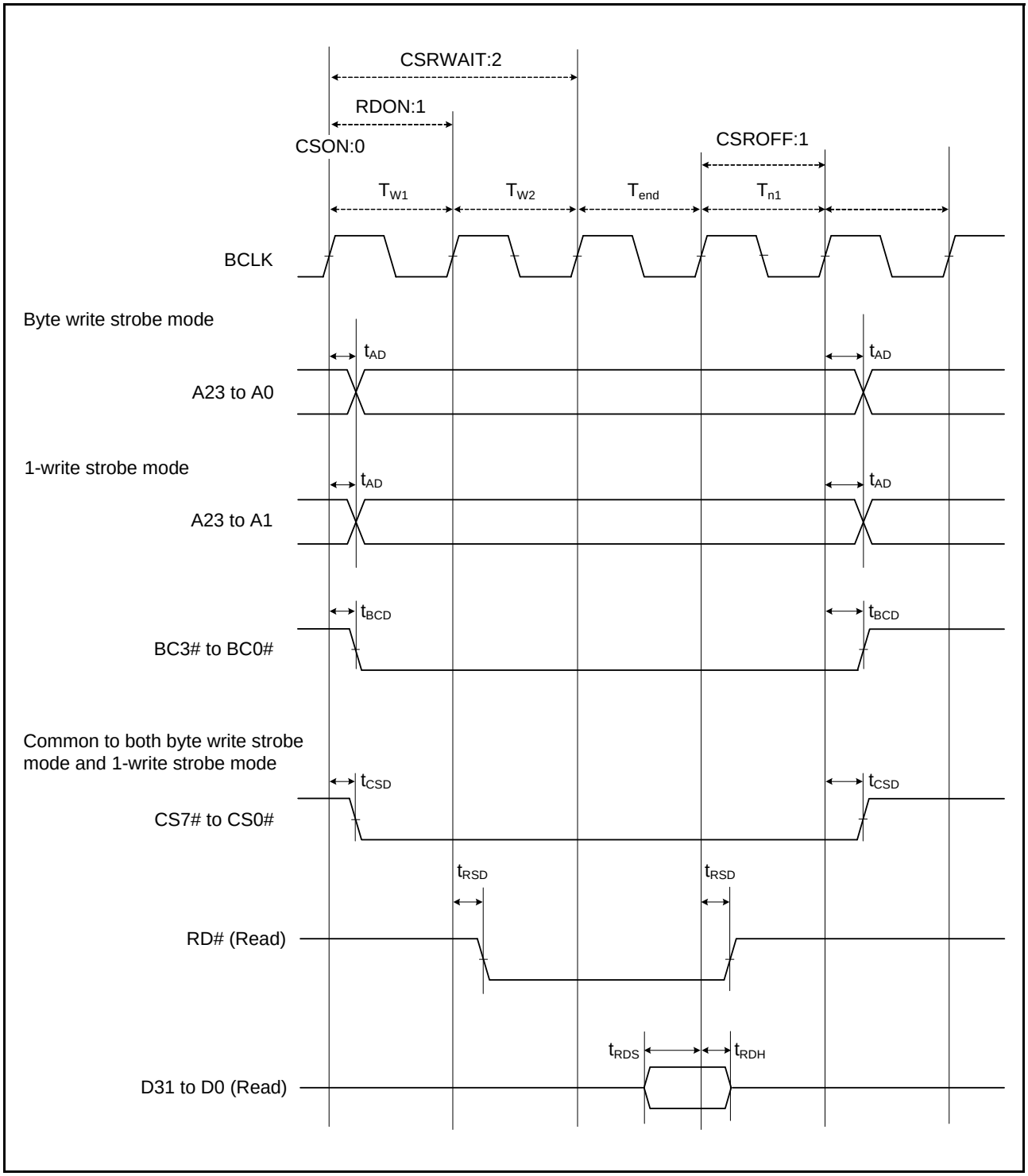
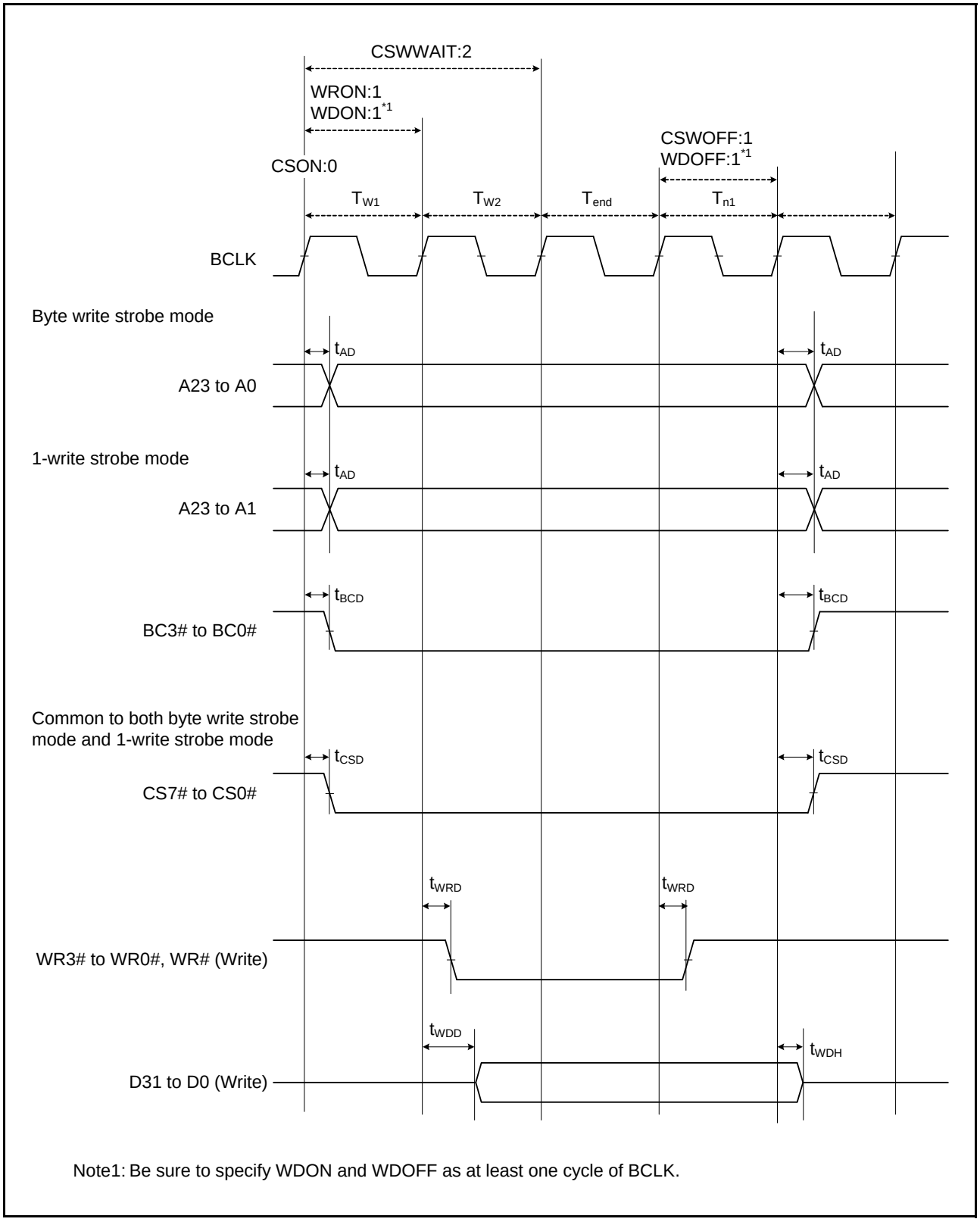


Figure 5.10 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)



Note1: Be sure to specify WDON and WDOFF as at least one cycle of BCLK.

Figure 5.11 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized)

5.3.4 EXDMAC Timing

Table 5.12 EXDMAC Timing

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
ICLK = 8 to 100 MHz, PCLK = 8 to 50 MHz, BCLK = 8 to 100 MHz, SDCLK = 8 to 50 MHz
T_a = -40 to +85°C

Item		Symbol	Min.	Max.	Unit	Test Conditions
EXDMAC	EDREQ setup time	t_{EDRQS}	20	—	ns	Figure 5.22
	EDREQ hold time	t_{EDRQH}	5	—	ns	
	EDACK delay time	t_{EDACD}	—	15	ns	Figure 5.23 and Figure 5.24

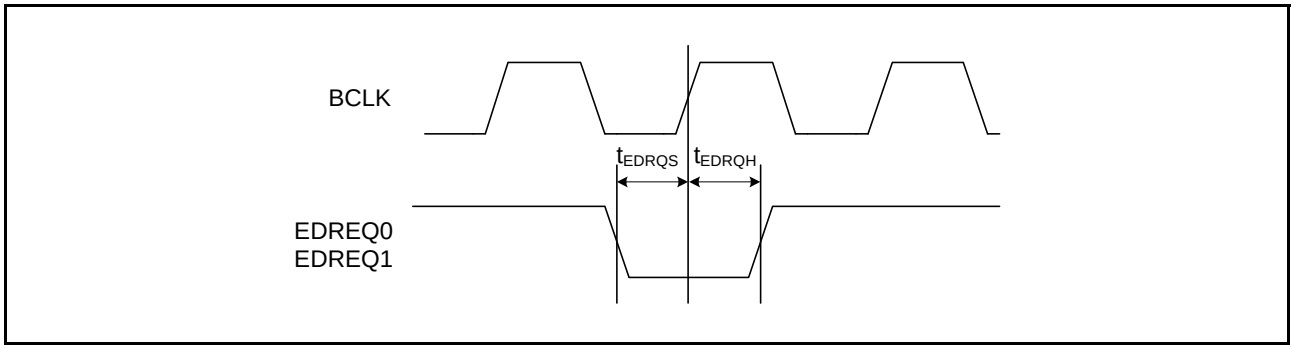


Figure 5.22 EDREQ0 and EDREQ1 Input Timing

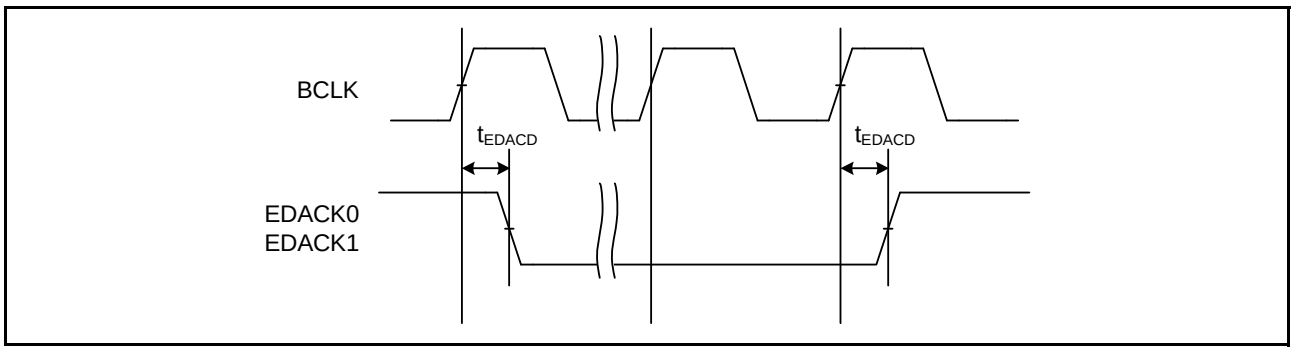


Figure 5.23 EDACK0 and EDACK1 Single-Address Transfer Timing (for a CS Area)

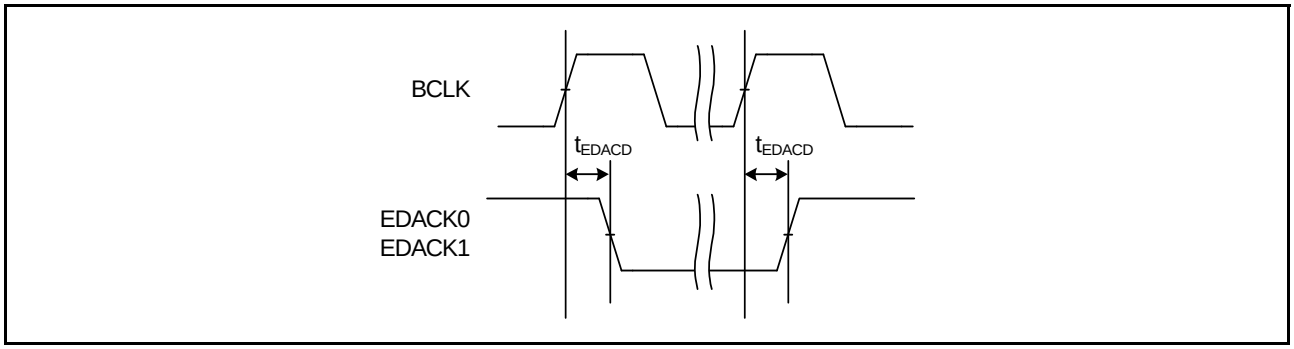


Figure 5.24 EDACK0 and EDACK1 Single-Address Transfer Timing (for SDRAM)

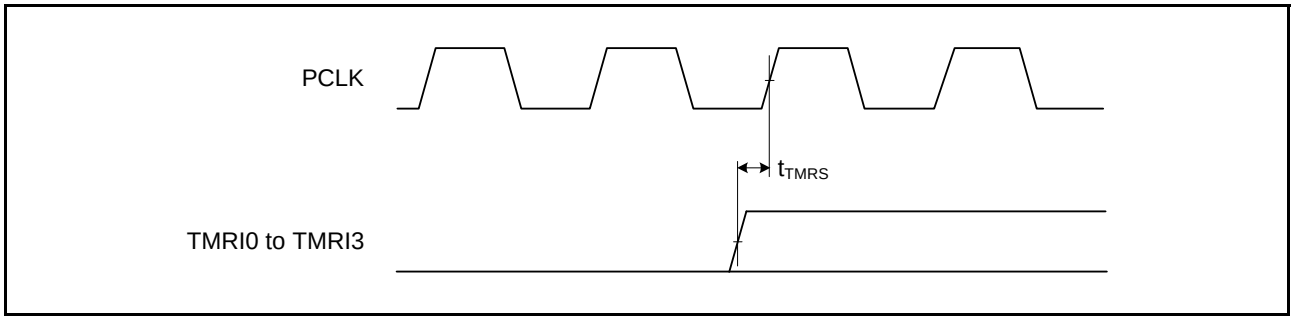


Figure 5.31 8-Bit Timer Reset Input Timing

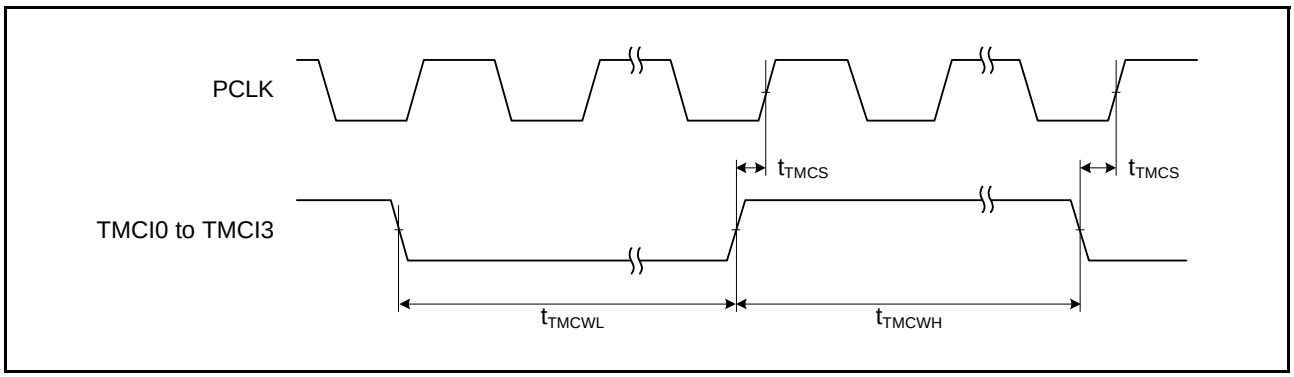


Figure 5.32 8-Bit Timer Clock Input Timing

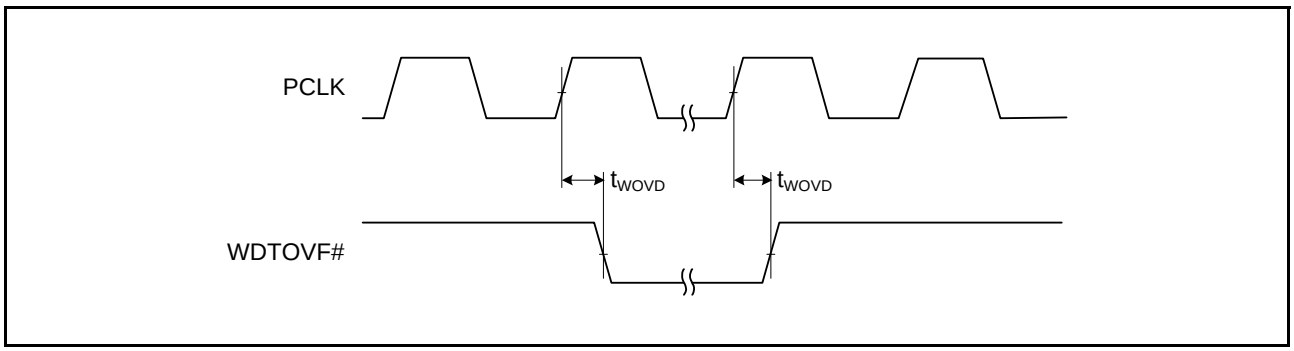


Figure 5.33 WDT Output Timing

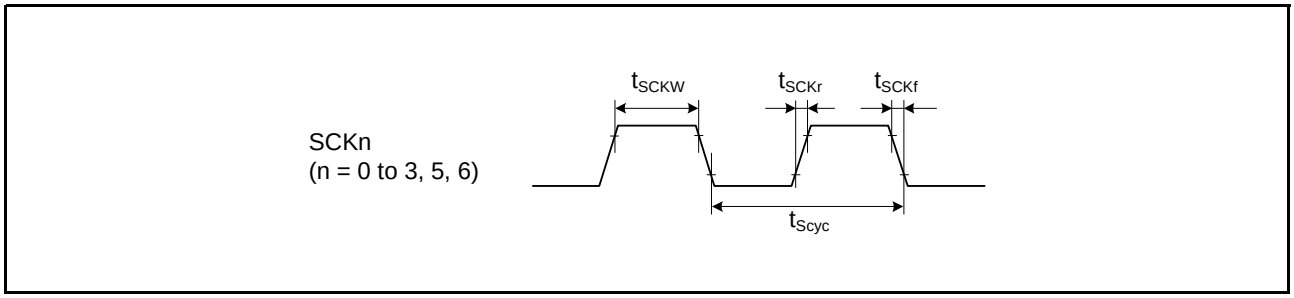


Figure 5.34 SCK Clock Input Timing

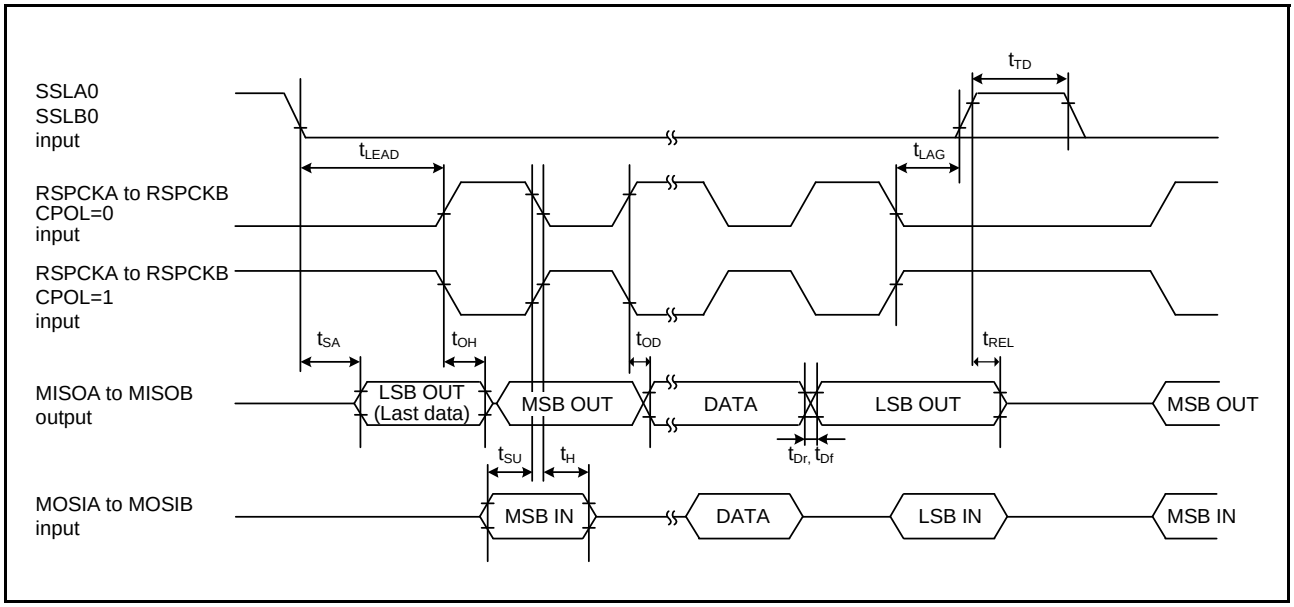


Figure 5.42 RSPI Timing (Slave, CPHA = 1)

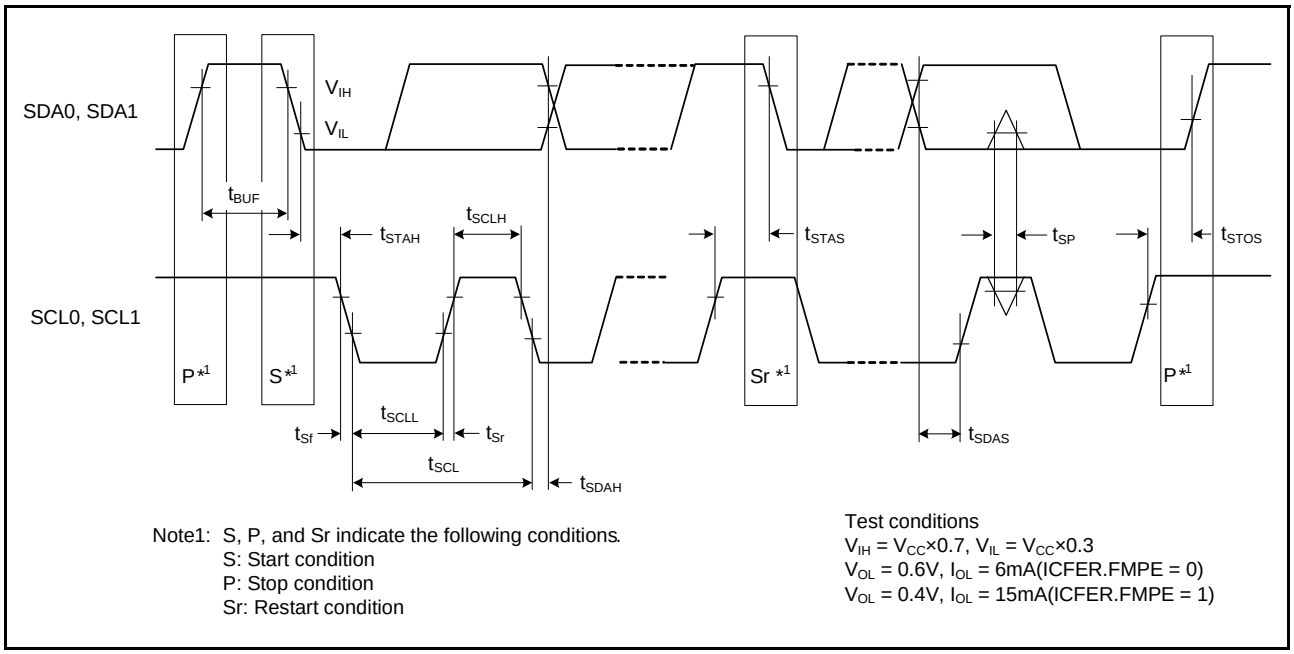


Figure 5.43 I2C Bus Interface Input/Output Timing

5.10 Data Flash (Flash Memory for Data Storage) Characteristics

Table 5.27 Data Flash (Flash Memory for Data Storage) Characteristics

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
Temperature range for the programming/erasure operation: T_a = -40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Programming time	8 bytes	t_{DP8}	—	0.4	2	ms	PCLK = 50-MHz operation
	128 bytes	t_{DP128}	—	1	5	ms	
Erasure time	2 Kbytes	t_{DE2K}	—	70	250	ms	PCLK = 50-MHz operation
Blank check time	8 bytes	t_{DBC8}	—	—	30	µs	PCLK = 50-MHz operation
	2 Kbytes	t_{DBC2K}	—	—	0.7	ms	
Rewrite/erase cycle*1		N_{DPEC}	30000*2	—	—	Times	
Suspend delay time during writing		t_{DSPD}	—	—	120	µs	Figure 5.67 PCLK = 50-MHz operation
First suspend delay time during erasing (in suspend priority mode)		t_{DSESD1}	—	—	120	µs	
Second suspend delay time during erasing (in suspend priority mode)		t_{DSESD2}	—	—	1.7	ms	
Suspend delay time during erasing (in erasure priority mode)		t_{DSEED}	—	—	1.7	ms	
Data hold time*3		t_{DDRP}	10	—	—	Year	

Note 1. Definition of rewrite/erase cycle:
The rewrite/erase cycle is the number of erasing for each block. When the rewrite/erase cycle is n times (n = 30000), erasing can be performed n times for each block. For instance, when 128-byte writing is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the rewrite/erase cycle is counted as one. However, writing to the same address for several times as one erasing is not enabled (over writing is prohibited).

Note 2. This indicates the minimum number that guarantees the characteristics after rewriting. (The guaranteed value is in the range from one to the minimum number.)

Note 3. This indicates the characteristic when rewrite is performed within the specification range including the minimum number.