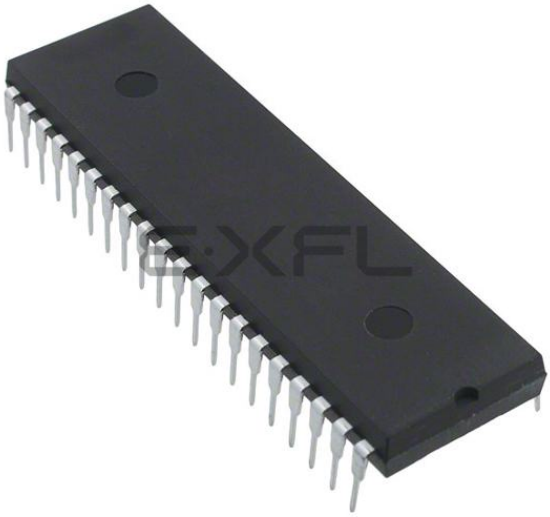

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Product Status	Last Time Buy
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	32
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/n78e517adg

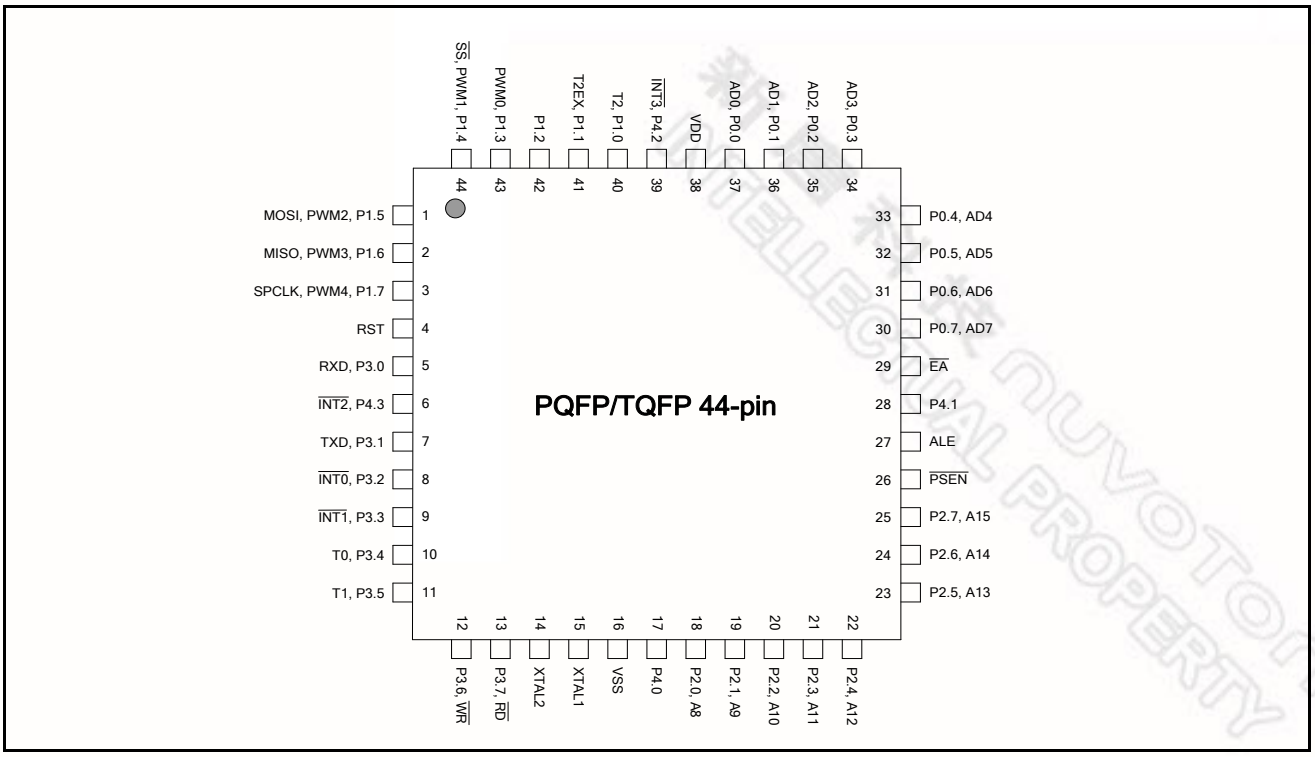


Figure 4–3. Pin Assignment of PQFP/TQFP 44-Pin

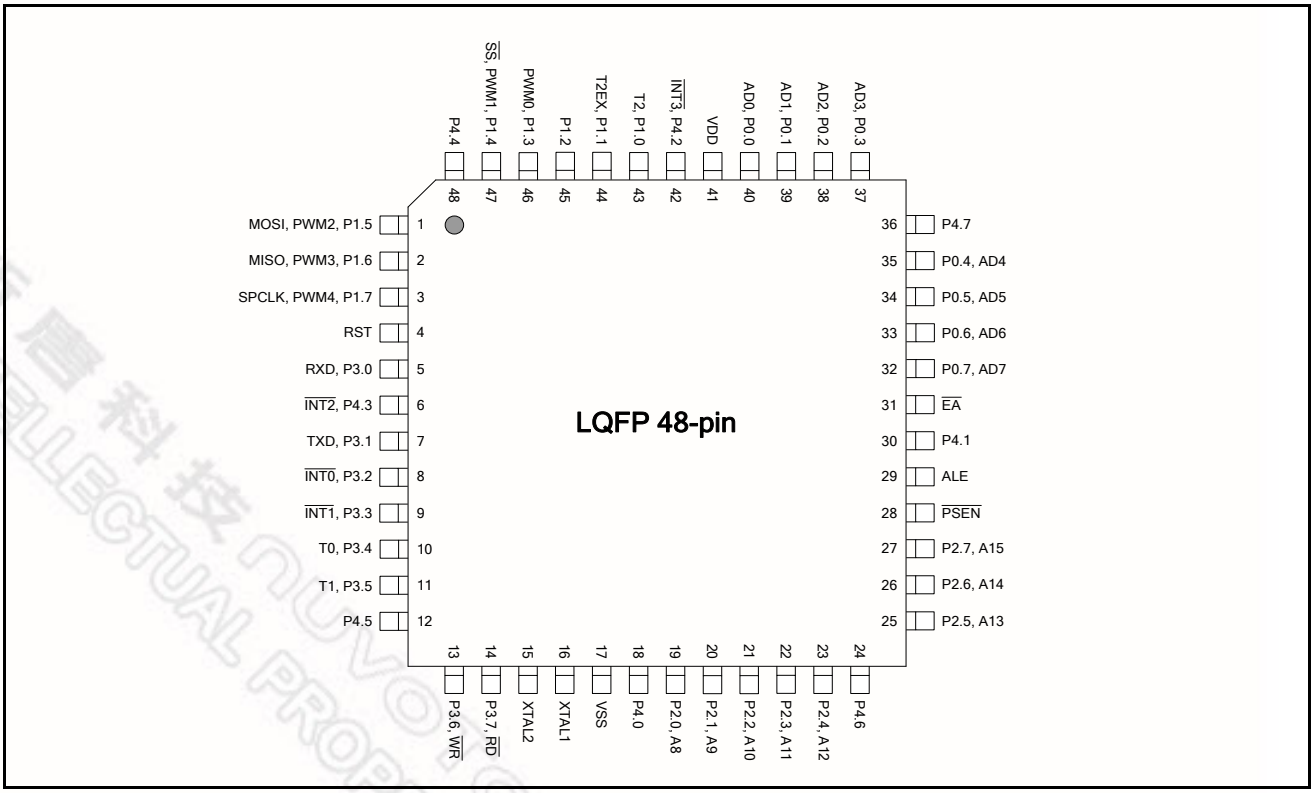


Figure 4–4. Pin Assignment of LQFP 48-Pin

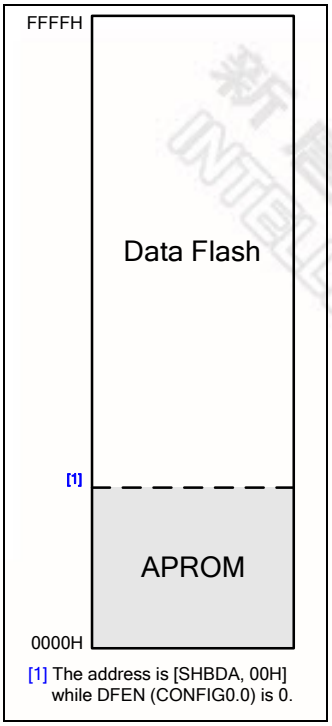


Figure 5–6. N78E517A Data Flash

CONFIG0

7	6	5	4	3	2	1	0
CBS	-	-	-	-	MOVCL	LOCK	DFEN
r/w	-	-	-	-	r/w	r/w	r/w

unprogrammed value: 1111 1111b

Bit	Name	Description
0	DFEN	**Data Flash enable.** 1 = There is no Data Flash space. The APROM size is 64k-byte. 0 = Data Flash exists. The Data Flash and APROM share 64k bytes depending on SHBDA setting.

CONFIG1

7	6	5	4	3	2	1	0
CHBDA[7:0][1]							
r/w							

unprogrammed value: 1111 1111b

Bit	Name	Description
7:0	CHBDA[7:0]	**CONFIG high byte of Data Flash starting address.** This byte is valid only when DFEN (CONFIG0.0) being 0 condition. It is used to determine the starting address of the Data Flash.

[1] Note that there will be no APROM if setting CHBDA 00H. CPU will execute codes in the external Program Memory.

8. AUXILIARY RAM (XRAM)

N78E517A provides additional on-chip 1k-byte RAM called XRAM to enlarge the RAM space. It occupies the address space from 000H through 3FFH. The XRAM is enabled after all resets. The 1024 bytes of XRAM are indirectly accessed by move external instruction MOVX @DPTR or MOVX @Ri along with XRAMAH. (If XRAM is enabled, MOVX @Ri cannot be used to access external RAM anymore.) This block of XRAM shares the same logic address of 000H through 3FFH with the external RAM. A DPTR value given larger than 03FFH will map to the external RAM no matter of the value of bit XRAMEN (CHPCON.4). If the user would like to access contents within 000H to 3FFH address of the off-chip external XRAM, the XRAMEN bit should be cleared as logic 0. (Note that CHPCON is a TA writing protected SFR.) When the XRAM is accessed, the address fetching signal will not emit via P0, P2, $\overline{WR}$, and $\overline{RD}$. Note that the stack pointer cannot locate in any part of XRAM.

CHPCON – Chip Control (TA protected)

7	6	5	4	3	2	1	0
SWRST	ISPF	LDUEN	XRAMEN	-	-	BS	ISPEN
w	r/w	r/w	r/w	-	-	r/w	r/w

Address: 9FH reset value: see Table 6–2. N78E517A SFR Description and Reset Values

Bit	Name	Description
4	XRAMEN	**XRAM enable.** 0 = Disable on-chip XRAM. 1 = Enable on-chip XRAM. (The default value after all resets.)

XRAMAH – XRAM Address High Byte

7	6	5	4	3	2	1	0
-	-	-	-	-	-	XRAMAH.1	XRAMAH.0
-	-	-	-	-	-	r/w	r/w

Address: A1H reset value: 0000 0000b

Bit	Name	Description
7:2	-	**Reserved.**
1:0	XRAMAH[1:0]	**XRAM address high byte.** To set the XRAM high byte address. This setting works along with MOV @Ri instructions. The demo codes are listed below.

XRAM demo code:

```
MOV     XRAMAH,#01H          ;write #5AH to XRAM with address @0123H.
MOV     R0,#23H
MOV     A,#5AH
MOVX    @R0,A

MOV     XRAMAH,#01H          ;read from XRAM with address @0123H.
MOV     R0,#23H
MOVX    A,@R0
```

```
MOV     DPTR,#0123H         ;write #5BH to XRAM with address @0123H.
MOV     A,#5BH
MOVX    @DPTR,A

MOV     DPTR,#0123H         ;read from XRAM with address @0123H.
MOVX    A,@DPTR
```

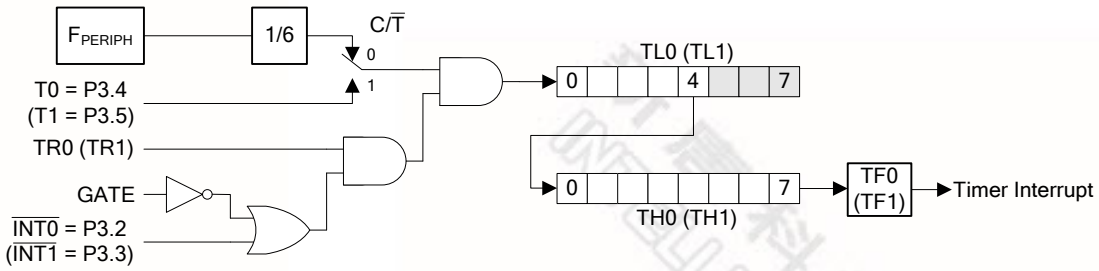


Figure 10–1. Timer/Counters 0 and 1 in Mode 0

10.1.2 Mode 1 (16-bit Timer)

Mode 1 is similar to Mode 0 except that the counting registers are fully used as a 16-bit counter. Roll-over occurs when a count moves FFFFH to 0000H. The Timer overflow flag TFx of the relevant Timer/Counter is set and an interrupt will occurs if enabled.

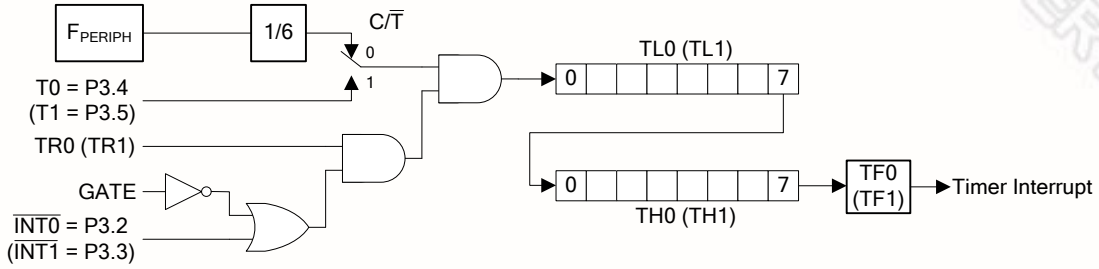


Figure 10–2. Timer/Counters 0 and 1 in Mode 1

10.1.3 Mode 2 (8-bit Auto-reload Timer)

In Mode 2, the Timer/Counter is in auto-reload mode. In this mode, TLx acts as an 8-bit count register whereas THx holds the reload value. When the TLx register overflows from FFH to 00H, the TFx bit in TCON is set, TLx is reloaded with the contents of THx, and the counting process continues from here. The reload operation leaves the contents of the THx register unchanged. This feature is best suitable for UART baud rate generator for it runs without continuous software intervention. Note that only Timer1 can be the baud rate source for UART. Counting is enabled by the TRx bit and proper setting of GATE and $\overline{INTx}$ pins. The functions of GATE and $\overline{INTx}$ pins are just the same as Mode 0 and 1.

Bit	Name	Description
3	EXEN2	**Timer 2 external enable.** This bit enables 1-to-0 transitions on T2EX trigger. 0 = 1-to-0 transitions on T2EX is ignored. 1 = 1-to-0 transitions on T2EX will set EXF2 logic 1. If Timer 2 is configured in capture or auto-reload mode, the 1-to-0 transitions on T2EX will cause capture or reload event.
2	TR2	**Timer 2 run control.** 0 = Timer 2 is halted. Clearing this bit will halt Timer 2 and the current count will be preserved in TH2 and TL2. 1 = Timer 2 is enabled.
1	C/$\overline{T2}$	**Timer 2 Counter/Timer select.** 0 = Timer 2 is incremented by internal peripheral clocks. 1 = Timer 2 is incremented by the falling edge of the external pin T2. If Timer 2 would like to be set in clock-out mode, C/$\overline{T2}$ must be 0.
0	CP/$\overline{RL2}$	**Timer 2 Capture or Reload select.** This bit selects whether Timer 2 functions in capture or auto-reload mode. EXEN2 must be logic 1 for 1-to-0 transitions on T2EX to be recognized and used to trigger captures or reloads. If RCLK or TCLK is set, this bit is ignored and Timer 2 will function in auto-reload mode. 0 = Auto-reload on Timer 2 overflow or 1-to-0 transition on T2EX pin. 1 = Capture on 1-to-0 transition at T2EX pin.

T2MOD – Timer 2 Mode

7	6	5	4	3	2	1	0
-	-	-	-	-	-	T2OE	-
-	-	-	-	-	-	r/w	-

Address: C9H reset value: 0000 0000b

Bit	Name	Description
7:2	-	**Reserved.**
1	T2OE	**Timer 2 clock-out enable.** 0 = Disable Timer 2 clock-out function. T2 pin functions either as a standard port pin or as a counter input for Timer 2. 1 = Enable Timer 2 clock-out function. Timer 2 will drive T2 pin with a clock output if C/$\overline{T2}$ is 0.
0	-	**Reserved.**

RCAP2L – Timer 2 Reload/Capture Low Byte

7	6	5	4	3	2	1	0
RCAP2L[7:0]							
r/w							

Address: CAH reset value: 0000 0000b

Bit	Name	Description
7:0	RCAP2L[7:0]	**Timer 2 reload/capture low byte.** This register captures and stores the low byte of Timer 2 when Timer 2 is configured in capture mode. When Timer 2 is in auto-reload mode, baud rate generator mode, or clock-out mode, it holds the low byte of the reload value.

10.2.4 Clock-out Mode

Timer 2 is equipped with a clock-out feature, which outputs a 50% duty cycle clock on P1.0. It can be invoked as a programmable clock generator. To configure Timer 2 with clock-out mode, software must initiate it by setting bit T2OE (TMOD.1) = 1, $C/\overline{T2}$ = 0 and $CP/\overline{RL2}$ = 0. Setting bit TR2 will start the clock output. This mode is similar to the baud rate generator mode which does not generate an interrupt while Timer 2 overflow. Similar with the baud rate generator mode, T2EX can also be configured as a simple external interrupt.

The clock-out frequency follows the equation $\frac{F_{OSC}}{2 \times 2^{EN6T} \times (65536 - (RCAP2H,RCAP2L))}$.

In this formula, EN6T is bit 6 of CONFIG3. While EN6T = 0, the clock system runs under 6T mode and the clock-out frequency will be double of that in 12T mode. (RCAP2H,RCAP2L) in the formula means $256 \times RCAP2H + RCAP2L$.

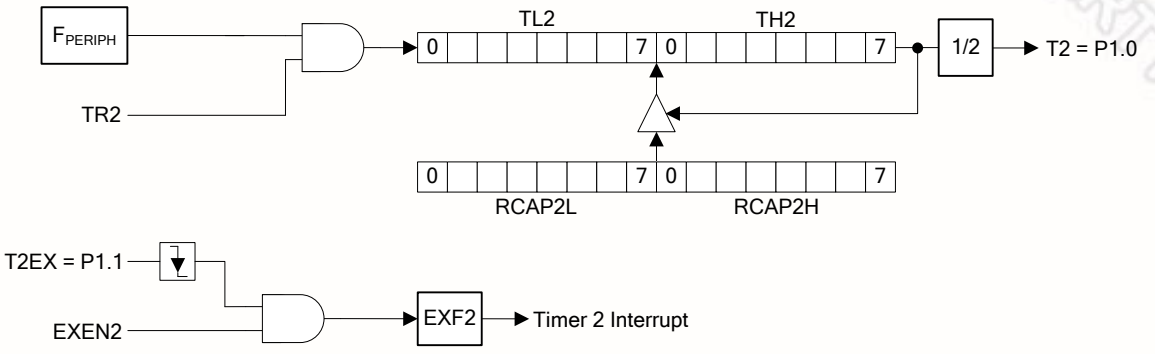


Figure 10–8. Timer/Counter 2 in Clock-out Mode

CONFIG3

7	6	5	4	3	2	1	0
CWDTEN	EN6T	ROG	CKF	INTOSCFS	-	FOSC	-
r/w	r/w	r/w	r/w	r/w	-	r/w	-

unprogrammed value: 1111 1111b

Bit	Name	Description
7	CWDTEN	**CONFIG Watchdog Timer enable.** 1 = Disable Watchdog Timer after all resets. 0 = Enable Watchdog Timer after all resets.

WDCON – Watchdog Timer Control (TA protected)

7	6	5	4	3	2	1	0
WDTEN[1]	WDCLR	-	WIDPD[2]	WDTRF[3]	WPS2[2]	WPS1[2]	WPS0[2]
r/w	w	-	r/w	r/w	r/w	r/w	r/w

Address: AAH reset value: see Table 6–2. N78E517A SFR Description and Reset Values

Bit	Name	Description
7	WDTEN	**Watchdog Timer enable.** 0 = Disable Watchdog Timer. 1 = Enable Watchdog Timer. The WDT counter starts running.
6	WDCLR	**Watchdog Timer clear.** Setting this bit will reset the Watchdog Timer count to 00H. It puts the counter in a known state and prohibit the system from reset. Note that this bit is written-only and has no need to be cleared via software.
5	-	**Reserved.**
4	WIDPD	**Watchdog Timer running in Idle and Power Down mode.** This bit decides whether Watchdog Timer runs in Idle or Power Down mode. 0 = WDT counter is halted while CPU is in Idle or Power Down mode. 1 = WDT keeps running while CPU is in Idle or Power Down mode.
3	WDTRF	**Watchdog Timer reset flag.** When the CPU is reset by Watchdog Timer time-out event, this bit will be set via hardware. This flag is recommended to be cleared via software.
2	WPS2	**Watchdog Timer clock pre-scalar select.** These bits determine the scale of the clock divider for WDT counter. The scale is from 1/1 through 1/256. See Table 11–1.
1	WPS1	
0	WPS0	

[1] WDTEN is initialized by the inversed value of CWDTEN (CONFIG3.7) after all resets.
[2] WIDPD and WPS[2:0] are cleared after power-on reset, and keep unchanged after any other resets.
[3] WDTRF will be cleared after power-on reset, be set after Watchdog Timer reset, and remains unchanged after any other resets.

The Watchdog time-out interval is determined by the formula $\frac{1}{F_{LOSC} \times clock\,divider\,scalar} \times 64$. Where F_{ILRC} is the frequency of internal 10kHz RC. The following table shows an example of the Watchdog time-out interval under different F_{WCK} and pre-scalars.

TH1 reload value	Oscillator Frequency (MHz)				
	11.0592	14.7456	18.432	22.1184	36.864
Baud Rate					
9600	FDh	FCh	FBh	FAh	F6h
4800	FAh	F8h	F6h	F4h	ECh
2400	F4h	F0h	ECh	E8h	D8h
1200	E8h	E0h	D8h	D0h	B0h
300	A0h	80h	60h	40h	

Table 13–4. Timer 2 Generated Commonly Used Baud Rates

RCAP2H, RCAP2L reload value	Oscillator Frequency (MHz)				
	11.0592	14.7456	18.432	22.1184	36.864
Baud Rate					
115200	FFh, FDh	FFh, FCh	FFh, FBh	FFh, FAh	FFh, F6h
57600	FFh, FAh	FFh, F8h	FFh, F6h	FFh, F4h	FFh, ECh
38400	FFh, F7h	FFh, F4h	FFh, F1h	FFh, EEh	FFh, E2h
19200	FFh, EEh	FFh, E8h	FFh, E2h	FFh, DCh	FFh, C4h
9600	FFh, DCh	FFh, D0h	FFh, C4h	FFh, B8h	FFh, 88h
4800	FFh, B8h	FFh, A0h	FFh, 88h	FFh, 70h	FFh, 10h
2400	FFh, 70h	FFh, 40h	FFh, 10h	FEh, E0h	FEh, 20h
1200	FEh, E0h	FEh, 80h	FEh, 20h	FDh, C0h	FCh, 40h
300	FBh, 80h	FAh, 00h	F8h, 80h	F7h, 00h	F1h, 00h

13.6 Multiprocessor Communication

N78E517A multiprocessor communication feature of UART lets a Master device send a multiple frame serial message to a Slave device in a multi-slave configuration. It does this without interrupting other slave devices that may be on the same serial line. This feature can be used only in UART mode 2 or 3 mode. After 9 data bits are received. The 9th bit value is written to RB8 (SCON.2). The user can enable this function by setting SM2 (SCON.5) as a logic 1 so that when the stop bit is received, the serial interrupt will be generated only if RB8 is 1. When the SM2 bit is 1, serial data frames that are received with the 9th bit as 0 do not generate an interrupt. In this case, the 9th bit simply separates the address from the serial data.

When the Master device wants to transmit a block of data to one of several slaves on a serial line, it first sends out an address byte to identify the target slave. Note that in this case, an address byte differs from a data byte: In an address byte, the 9th bit is 1 and in a data byte, it is 0. The address byte interrupts all slaves so that each slave can examine the received byte and see if it is being addressed. The addressed slave then clears its SM2

Bit	Name	Description
3	DISMODF	**Disable Mode Fault error detection.** This bit is used in combination with the SSOE (SPCR.7) bit to determine the feature of $\overline{SS}$ pin as shown in Table 14–1. Slave Select Pin Configurations. DISMODF affects only in Master mode (MSTR = 1). 0 = Mode Fault detection is not disabled. $\overline{SS}$ serves as input pin for Mode Fault detection disregard of SSOE. 1 = Mode Fault detection is disabled. The feature of $\overline{SS}$ follows SSOE bit.
2:0	-	**Reserved.**

SPDR – Serial Peripheral Data Register

7	6	5	4	3	2	1	0
SPDR[7:0]							
r/w							

Address: F5H reset value: 0000 0000b

Bit	Name	Description
7:0	SPDR[7:0]	**Serial peripheral data.** This byte is used of transmitting or receiving data on SPI bus. A write of this byte is a write to the shift register. A read of this byte is actually a read of the read data buffer. In Master mode, a write to this register initiates transmission and reception of a byte simultaneously.

14.4 Operating Modes

14.4.1 Master mode

The SPI can operate in Master mode while MSTR (SPCR.4) is set as 1. Only one Master SPI device can initiate transmissions. A transmission always begins by Master through writing to SPDR. The byte written to SPDR begins shifting out on MOSI pin under the control of SPCLK. Simultaneously, another byte shifts in from the Slave on the MISO pin. After 8-bit data transfer complete, SPIF (SPSR.7) will automatically set via hardware to indicate one byte data transfer complete. At the same time, the data received from the Slave is also transferred in SPDR. The user can clear SPIF and read data out of SPDR.

14.4.2 Slave Mode

When MSTR is 0, the SPI operates in Slave mode. The SPCLK pin becomes input and it will be clocked by another Master SPI device. The $\overline{SS}$ pin also becomes input. The Master device cannot exchange data with the Slave device until the $\overline{SS}$ pin of the Slave device is externally pulled low. Before data transmissions occurs, the $\overline{SS}$ of the Slave device must be pulled and remain low until the transmission is complete. If $\overline{SS}$ goes

CHPCON – Chip Control (TA protected)

7	6	5	4	3	2	1	0
SWRST	ISPF	LDUEN	XRAMEN	-	-	BS	ISPEN
w	r/w	r/w	r/w	-	-	r/w	r/w

Address: 9FH reset value: see Table 6–2. N78E517A SFR Description and Reset Values

Bit	Name	Description
6	ISPF	**ISP fault flag.** The hardware will set this bit when any of the following condition is met: 1. The accessing area is illegal, such as, (a) Erasing or programming APROM itself when APROM code runs. (b) Erasing or programming LDROM when APROM code runs but LDUEN is 0. I Erasing, programming, or reading CONFIG bytes when APROM code runs. (d) Erasing or programming LDROM itself when LDROM code runs. (e) Accessing oversize. 2. The ISP operating runs from internal Program Memory into external one. This bit should be cleared via software.
5	LDUEN	**Updating LDROM enable.** 0 = The LDROM is inhibited to be erased or programmed when APROM code runs. LDROM remains read-only. 1 = The LDROM is allowed to be fully accessed when APROM code runs.
0	ISPEN	**ISP enable.** 0 = Enable ISP function. 1 = Disable ISP function. To enable ISP function will start the internal 22.1184MHz RC oscillator for timing control. To clear ISPEN should always be the last instruction after ISP operation in order to stop internal RC for reducing power consumption.

ISPCN – ISP Control

7	6	5	4	3	2	1	0
ISPA.17	ISPA.16	FOEN	FCEN	FCTRL.3	FCTRL.2	FCTRL.1	FCTRL.0
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Address: AFH reset value: 0000 0000b

Bit	Name	Description
7:6	ISPA[17:16]	**ISP control.** This byte is for ISP controlling command to decide ISP destinations and actions. For details, see Table 18–1. ISP Modes and Command Codes.
5	FOEN	
4	FCEN	
3:0	FCTRL[3:0]	

18.2 ISP Commands

N78E517A provides a wide application to perform ISP to APROM, LDROM or on-chip Data Flash. The ISP action mode and the destination of the flash block are defined by ISP control register ISPCN.

Table 18–1. ISP Modes and Command Codes

ISP Mode	ISPCN				ISPAH, ISPAL ISPA[15:0]	ISPFD[7:0]
	ISPA.17, ISPA.16	FOEN	FCEN	FCTRL[3:0]		
Standby	X, X[1]	1	1	X	X	X
APROM and Data Flash Page Erase	0, 0	1	0	0010	Address in[2]	X
LDROM Page Erase	0, 1	1	0	0010	Address in[2]	X
APROM and Data Flash Program	0, 0	1	0	0001	Address in	Data in
LDROM Program	0, 1	1	0	0001	Address in	Data in
APROM and Data Flash Read	0, 0	0	0	0000	Address in	Data out
LDROM Read	0, 1	0	0	0000	Address in	Data out
All CONFIG bytes Erase	1, 1	1	0	0010	00XXH	X
CONFIG Program	1, 1	1	0	0001	CONFIG0: 0000H CONFIG1: 0001H CONFIG2: 0002H CONFIG3: 0003H	Data in
CONFIG Read	1, 1	0	0	0000	CONFIG0: 0000H CONFIG1: 0001H CONFIG2: 0002H CONFIG3: 0003H	Data out

[1] "x" means "don't care".
[2] Each page is 256-byte size. Therefore, the address for Page Erase should be 0000H, 0100H, 0200H, 0300H, etc., which is incremented by one of high byte address.

18.3 User Guide of ISP

ISP facilitates the updating flash contents in a convenient way; however, the user should follow some restricted laws in order that the ISP operates correctly. Without noticing warnings will possible cause undetermined results even serious damages of devices. Be attention of these notices. Furthermore, this paragraph will also support useful suggestions during ISP procedures.

(1) If no more ISP operation needs, the user must clear ISPEN (CHPCON.0) to zero. It will make the system void to trigger ISP unaware. Furthermore, ISP requires internal 22.1184MHZ RC oscillator running. If the external clock source is chosen, disabling ISP will stop internal 22.1184MHz RC for saving power consumption. Note that a write to ISPEN is TA protected.

Power Down. As mentioned before the user will endure the large current of Brown-out detection circuit. It is not a typical application.

CONFIG3

7	6	5	4	3	2	1	0
CWDTEN	EN6T	ROG	CKF	INTOSCFS	-	FOSC	-
r/w	r/w	r/w	r/w	r/w	-	r/w	-

unprogrammed value: 1111 1111b

Bit	Name	Description
6	EN6T	**Enable 6T mode.** This bit switches MCU between 12T and 6T mode. See Figure 20–1. Clock System Block Diagram for definitions in details. 1 = MCU runs at 12T mode. Each machine-cycle is equal to 12 clocks of system oscillator. The operating mode is the same as a standard 8051 MCU. (F_{CPU} and F_{PERIPH} is a half of F_{OSC}.) 0 = MCU runs at 6T mode. Each machine-cycle is equal to 6 clocks of system oscillator. This mode doubles the whole chip operation compared with the standard 8051. (F_{CPU} and F_{PERIPH} is equal to F_{OSC}.)
5	ROG	**Reducing oscillator gain.** 1 = Use normal gain for crystal oscillating. The crystal frequency can be up to 40MHz. 0 = Use reduced gain for crystal oscillating. The crystal frequency should be lower than 24MHz. In reduced gain mode, it will also help to decrease EMI.
4	CKF	**Clock filter enable.** 1 = Enable clock filter. It increases noise immunity and EMC capacity. 0 = Disable clock filter.
3	INTOSCFS	**Internal RC oscillator frequency select.** 1 = Select 22.1184MHz as the system clock if internal RC oscillator mode is used. It bypasses the divided-by-2 path of internal oscillator to select 22.1184MHz output as the system clock source. 0 = Select 11.0592MHz as the system clock if internal RC oscillator mode is used. The internal RC divided-by-2 path is selected. The internal oscillator is equivalent to 11.0592MHz output used as the system clock.
2	-	**Reserved.**
1	FOSC	**Oscillator selection bit.** This bit selects the source of the system clock. 1 = Crystal, resonator, or external clock input. 0 = Internal RC oscillator.
0	-	**Reserved.**

CHPCON – Chip Control (TA protected)

7	6	5	4	3	2	1	0
SWRST	ISPF	LDUEN	XRAMEN	-	-	BS	ISPEN
w	r/w	r/w	r/w	-	-	r/w	r/w

Address: 9FH reset value: see Table 6–2. N78E517A SFR Description and Reset Values

Bit	Name	Description
0	ISPEN	**ISP enable.** 0 = Enable ISP function. 1 = Disable ISP function. To enable ISP function will start the internal 22.1184MHz RC oscillator for timing control. To clear ISPEN should always be the last instruction after ISP operation in order to stop internal RC for reducing power consumption.

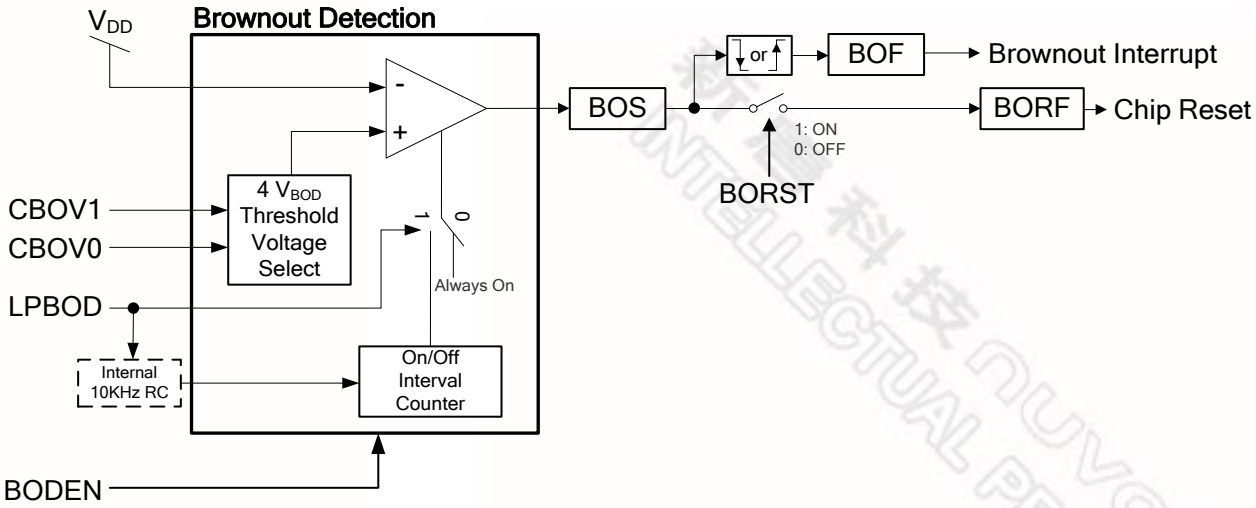
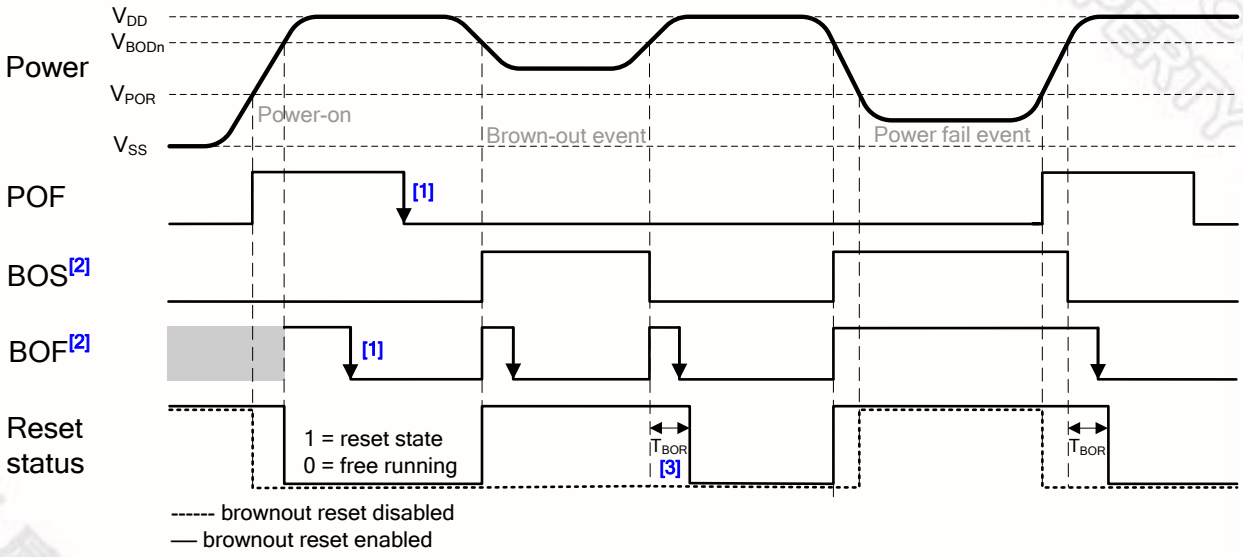


Figure 21–1. Brown-out Detection Block Diagram



[1] POF and BOF are both cleared by software.
[2] Brown-out reset is disabled. While the whole brown-out detection circuit disabled, BOS and BOF will keep 0.
[3] T_{BOR} ~= 8ms

Figure 21–2. Power Monitoring Timing Diagram

Bit	Name	Description
1	-	**Reserved.**
0	BOS	**Brown-out status.** This bit indicates the V_{DD} voltage level comparing with V_{BOD} while Brown-out circuit is enabled. It is helpful to tell a Brown-out event or power resuming event occurrence. This bit is read-only and keeps 0 if Brown-out detection is not enabled. 0 = V_{DD} voltage level is higher than V_{BOD}. 1 = V_{DD} voltage level is lower than V_{BOD}.

[1] BODEN and BORST will be directly loaded from CONFIG2 bit 7 and bit 4 after all resets.

Table 21–1. BOF Reset Value

Reset source	CBODEN (CONFIG2.7)	CBORST (CONFIG2.4)	V_{DD} stable level	BOF
Brown-out reset	1	1	> V_{BOD} always	1
Other resets	1	1	> V_{BOD} always	1
	1	0	> V_{BOD}	1
	1	0	< V_{BOD}	0
	0	X	X	0

Note that if BOF is 1 after chip reset, it is strongly recommended to initialize the user's program by clearing BOF.

PCON – Power Control

7	6	5	4	3	2	1	0
SMOD	-	-	POF	GF1	GF0	PD	IDL
r/w	-	-	r/w	r/w	r/w	r/w	r/w

Address: 87H reset value: see Table 6–2. N78E517A SFR Description and Reset Values

Bit	Name	Description
4	POF	**Power-on reset flag.** This bit will be set as 1 after a power-on reset. It indicates a cold reset, a power-on reset complete. This bit remains its value after any other resets. This flag is recommended to be cleared via software.

25. INSTRUCTION SET

N78E517A executes all the instructions of the standard 8051 family. All instructions are coded within an 8-bit field called an OPCODE. This single byte must be fetched from Program Memory. The OPCODE is decoded by the CPU. It determines what action the microcontroller will take and whether more operation data is needed from memory. If no other data is needed, then only one byte was required. Thus the instruction is called a one byte instruction. In some cases, more data is needed. These will be two or three byte instructions.

Table 25–1 lists all instructions in details. Note of the instruction set and addressing modes are shown below.

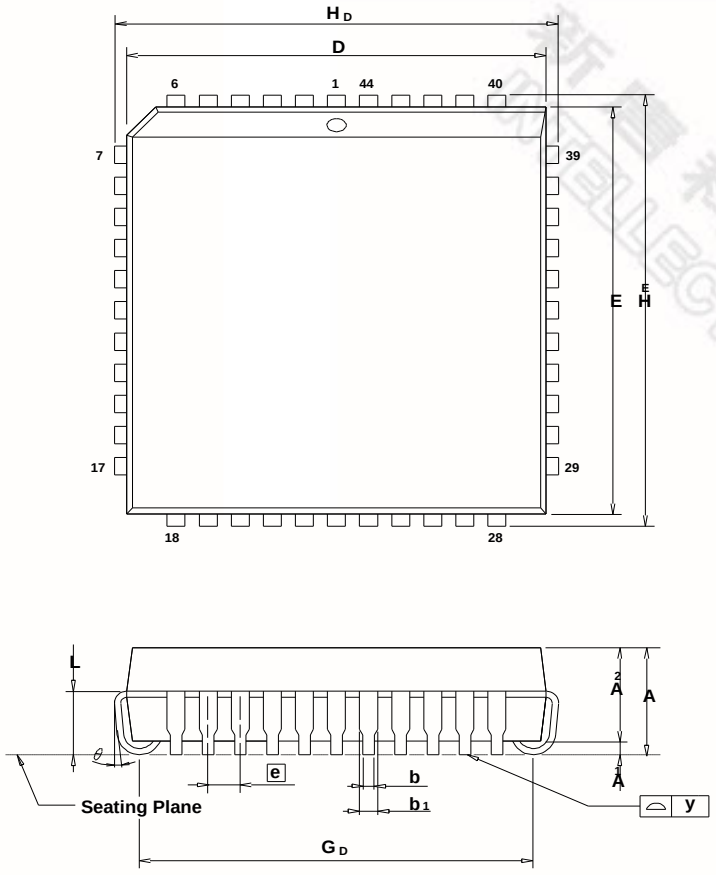
Rn (n = 0-7)	Register R0-R7 of the currently selected Register Bank.
direct	8-bit internal data location's address. It could be an internal data RAM location (0-127) or a SFR (e.g., I/O port, control register, status register, etc. (128-255)).
@Ri (i = 0, 1)	8-bit internal data RAM location (0-255) addressed indirectly through register R0 or R1.
#data	8-bit constant included in the instruction.
#data16	16-bit constant included in the instruction.
addr16	16-bit destination address. Used by LCALL and LJMP. A branch can be anywhere within the 64k-byte Program Memory address space.
addr11	11-bit destination address. Used by ACALL and AJMP. The branch will be within the same 2k-byte page of Program Memory as the first byte of the following instruction.
rel	Signed (2's complement) 8-bit offset byte. Used by SJMP and all conditional branches. Range is -128 to +127 bytes relative to first byte of the following instruction.
bit	Direct addressed bit in internal data RAM or SFR.

Table 25–1. Instruction Set for N78E517A

Instruction	OPCODE	Bytes	Clock Cycles in 12T Mode	Clock Cycles in 6T Mode
NOP	00	1	12	6
ADD A, Rn	28-2F	1	12	6
ADD A, @Ri	26, 27	1	12	6
ADD A, direct	25	2	12	6
ADD A, #data	24	2	12	6
ADDC A, Rn	38-3F	1	12	6
ADDC A, @Ri	36, 37	1	12	6
ADDC A, direct	35	2	12	6
ADDC A, #data	34	2	12	6
SUBB A, Rn	98-9F	1	12	6
SUBB A, @Ri	96, 97	1	12	6
SUBB A, direct	95	2	12	6
SUBB A, #data	94	2	12	6

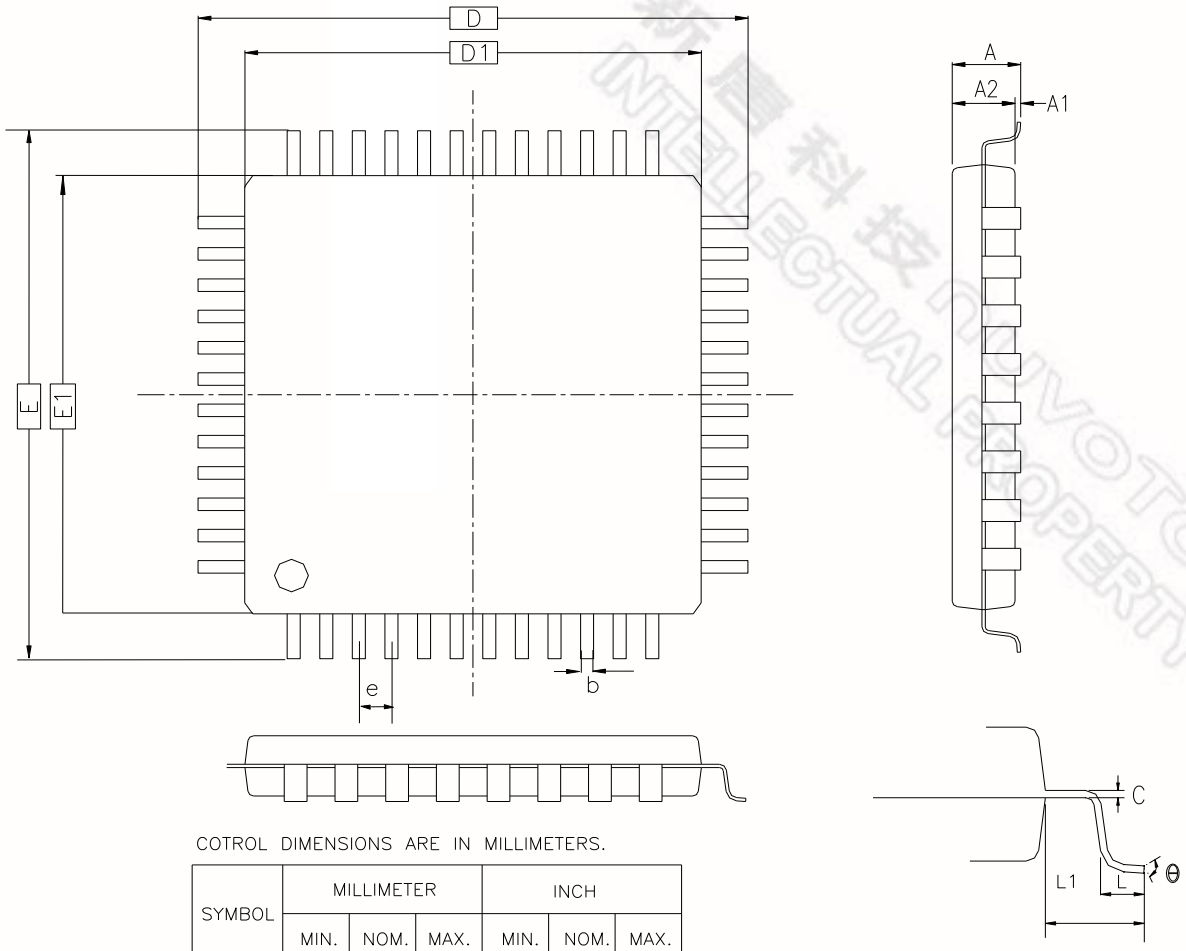
Table 25–1. Instruction Set for N78E517A

Instruction		OPCODE	Bytes	Clock Cycles in 12T Mode	Clock Cycles in 6T Mode
MOV	A, #data	74	2	12	6
MOV	Rn, A	F8-FF	1	12	6
MOV	Rn, direct	A8-AF	2	24	12
MOV	Rn, #data	78-7F	2	12	6
MOV	@Ri, A	F6, F7	1	12	6
MOV	@Ri, direct	A6, A7	2	24	12
MOV	@Ri, #data	76, 77	2	12	6
MOV	direct, A	F5	2	12	6
MOV	direct, Rn	88-8F	2	24	12
MOV	direct, @Ri	86, 87	2	24	12
MOV	direct, direct	85	3	24	12
MOV	direct, #data	75	3	24	12
MOV	DPTR, #data16	90	3	24	12
MOVC	A, @A+DPTR	93	1	24	12
MOVC	A, @A+PC	83	1	24	12
MOVX	A, @Ri	E2, E3	1	24	12
MOVX	A, @DPTR	E0	1	24	12
MOVX	@Ri, A	F2, F3	1	24	12
MOVX	@DPTR, A	F0	1	24	12
PUSH	direct	C0	2	24	12
POP	direct	D0	2	24	12
XCH	A, Rn	C8-CF	1	12	6
XCH	A, @Ri	C6, C7	1	12	6
XCH	A, direct	C5	2	12	6
XCHD	A, @Ri	D6, D7	1	12	6
CLR	C	C3	1	12	6
CLR	bit	C2	2	12	6
SETB	C	D3	1	12	6
SETB	bit	D2	2	12	6
CPL	C	B3	1	12	6
CPL	bit	B2	2	12	6
ANL	C, bit	82	2	24	12
ANL	C, /bit	B0	2	24	12
ORL	C, bit	72	2	24	12
ORL	C, /bit	A0	2	24	12
MOV	C, bit	A2	2	12	6
MOV	bit, C	92	2	24	12
ACALL	addr11	11, 31, 51, 71, 91, B1, D1, F1[1]	2	24	12
LCALL	addr16	12	3	24	12



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.185	—	—	4.70
A_1	0.020	—	—	0.51	—	—
A_2	0.145	0.150	0.155	3.68	3.81	3.94
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.36
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e	0.050 BSC			1.27 BSC		
G_D	0.590	0.610	0.630	14.99	15.49	16.00
G_E	0.590	0.610	0.630	14.99	15.49	16.00
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.29	2.54	2.79
y	—	—	0.004	—	—	0.10

Figure 27–2. PLCC-44 Package Dimention



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A_1	0.05	0.10	0.15	0.002	0.004	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
D1	6.90	7.00	7.10	0.272	0.276	0.260
E1	6.90	7.00	7.10	0.272	0.276	0.260
e	0.35	0.50	0.65	0.014	0.020	0.260
D	8.9	9.00	9.10	0.350	0.354	0.358
E	8.9	9.00	9.10	0.350	0.354	0.358
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	—	1.00	—	—	0.039	—
C	0.09	—	0.20	0.0035	—	0.0079
θ	0°	—	7°	0°	—	7°
b	0.17	0.22	0.27	0.007	0.0087	0.011

Figure 27–5. LQFP-48 Package Dimention