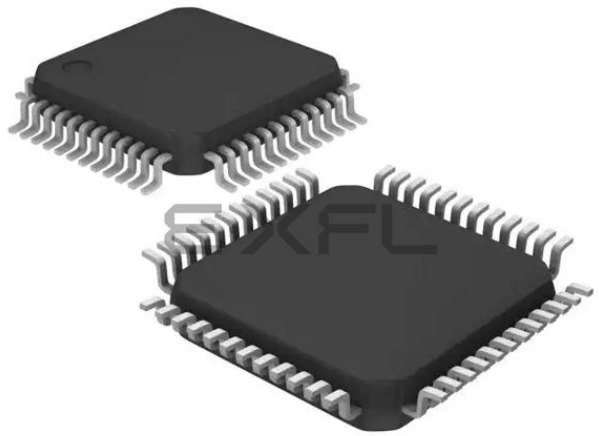

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/n78e517alg

Table 4–1. Pin Description

Pin number				Symbol	Alternate Function		Type[1]	Description
DIP	PLCC	PQFP TQFP	LQFP		1	2		
19	21	15	16	XTAL1			I (ST)	**CRYSTAL1:** This is the input pin to the internal inverting amplifier. The system clock is from external crystal or resonator when FOSC (CONFIG3.1) is logic 1 by default. ***A 0.1µF capacitor is recommended to be added on XTAL1 pin to gain the more precise frequency of the internal RC oscillator frequency if it is selected as the system clock source.***
18	20	14	15	XTAL2			O	**CRYSTAL2:** This is the output pin from the internal inverting amplifier. It emits the inverted signal of XTAL1. While on-chip RC oscillator is used, float XTAL2 pin always.
40	44	38	41	VDD			P	**POWER SUPPLY:** Supply voltage V_{DD} for operation.
20	22	16	17	VSS			P	**GROUND:** Ground potential.
31	35	29	31	$\overline{EA}$			I	**EXTERNAL ACCESS ENABLE:** To force $\overline{EA}$ low will make the CPU execute the external Program Memory. The address and data will be presented on the bus P0 and P2. If the $\overline{EA}$ pin is high, CPU will fetch internal code unless the Program Counter addresses the area out of the internal Program Memory. It will make CPU run external Program Memory continuously. $\overline{EA}$ possesses reset lock. After all reset, the $\overline{EA}$ state will be latched and any state change of this pin after reset will not switch between internal and external Program Memory execution. ***The user should take care of this pin from floating but connecting to V_{DD} directly if internal Program Memory is used.***
30	33	27	29	ALE			O	**ADDRESS LATCH ENABLE:** ALE is used to enable the address latch that separates the address from the data on Port 0. ALE runs at 1/6 of the Fosc[2]. An ALE pulse is omitted always. The user can turn ALE off by setting ALEOFF (AUXR.0) to reduce EMI. Setting ALEOFF will just make ALE activating only during external memory access through a MOVC or MOVX instruction. ALE will stay high in other conditions.
29	32	26	28	$\overline{PSEN}$			O	**PROGRAM STORE ENABLE:** $\overline{PSEN}$ strobes the external Program Memory. When internal Program Memory access is performed, there will be no $\overline{PSEN}$ strobe signal output from this pin.

Table 4–1. Pin Description

Pin number				Symbol	Alternate Function		Type[1]	Description
DIP	PLCC	PQFP TQFP	LQFP		1	2		
9	10	4	4	RST			I (ST)	**RESET:** RST pin is a Schmitt trigger input pin for hardware device reset. A high on this pin for two machine-cycles while the system clock is running will reset the device. RST pin has an internal pull-down resistor allowing power-on reset by simply connecting an external capacitor to V_{DD}.
39	43	37	40	P0.0		AD0	D, I/O	**PORT0:** Port 0 is an 8-bit open-drain port by default. Via setting P0UP (P0OR.0), P0 will switch as weakly pulled up internally. P0 has an alternative function as AD[7:0] while external memory accessing. During the external memory access, P0 will output high will be internal strong pulled-up rather than weak pull-up in order to drive out high byte address for external devices.
38	42	36	39	P0.1		AD1	D, I/O	
37	41	35	38	P0.2		AD2	D, I/O	
36	40	34	37	P0.3		AD3	D, I/O	
35	39	33	35	P0.4		AD4	D, I/O	
34	38	32	34	P0.5		AD5	D, I/O	
33	37	31	33	P0.6		AD6	D, I/O	
32	36	30	32	P0.7		AD7	D, I/O	
1	2	40	43	P1.0	T2		I/O	**PORT1:** Port 1 is an 8-bit quasi bi-directional I/O port. Its multifunction pins are for T2, T2EX, PWM0-PWM4, $\overline{SS}$, MOSI, MISO, and SPCLK.
2	3	41	44	P1.1	T2EX		I/O	
3	4	42	45	P1.2			I/O	
4	5	43	46	P1.3	PWM0		I/O	
5	6	44	47	P1.4	PWM1	$\overline{SS}$	I/O	
6	7	1	1	P1.5	PWM2	MOSI	I/O	
7	8	2	2	P1.6	PWM3	MISO	I/O	
8	9	3	3	P1.7	PWM4	SPCLK	I/O	
21	24	18	19	P2.0		A8	I/O	**PORT2:** Port 2 is an 8-bit quasi bi-directional I/O port. It has an alternative function as A[15:8] while external memory accessing. During the external memory access, P2 will output high will be internal strong pulled-up rather than weak pull-up in order to drive out high byte address for external devices.
22	25	19	20	P2.1		A9	I/O	
23	26	20	21	P2.2		A10	I/O	
24	27	21	22	P2.3		A11	I/O	
25	28	22	23	P2.4		A12	I/O	
26	29	23	25	P2.5		A13	I/O	
27	30	24	26	P2.6		A14	I/O	

The application circuit is shown below. The user is recommended follow the circuit enclosed by gray blocks to achieve the most stable and reliable operation of MCU especially in a noisy power environment for a healthy EMS immunity. If internal RC oscillator is used as the system clock, a 0.1μF capacitor should be added to gain a precise RC frequency.

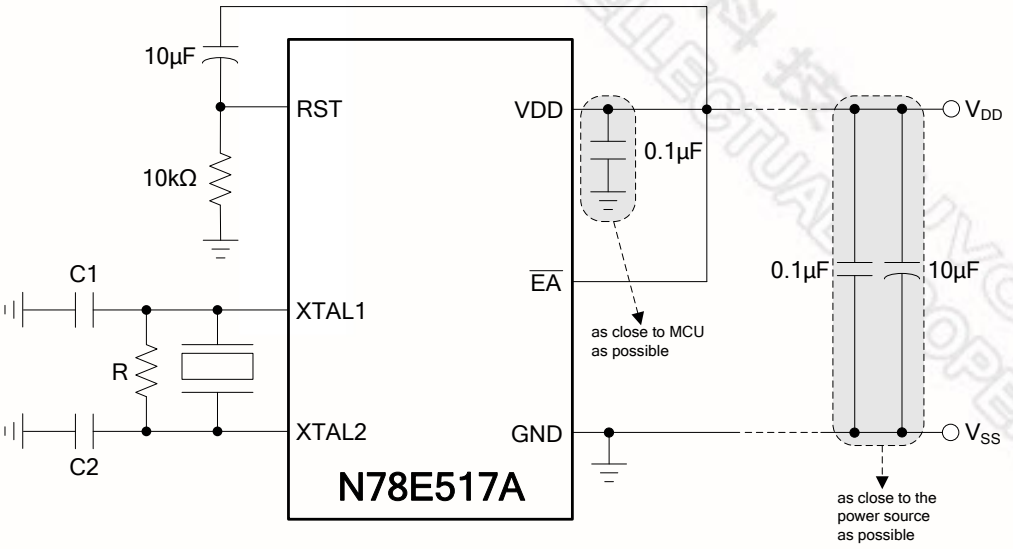


Figure 4–5. Application Circuit for Execution of Internal Program Code with External Crystal

Crystal Frequency	R	C1	C2
4MHz-33MHz	Without	Depend on crystal specifications	
33MHZ-40MHz	5kΩ-10kΩ		

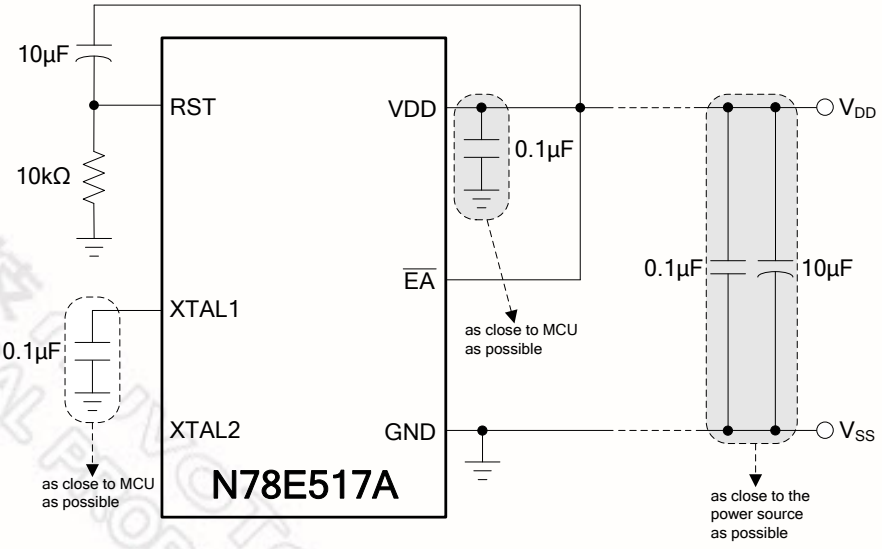


Figure 4–6. Application Circuit for Execution of Internal Program Code with Internal RC Oscillator

5. MEMORY ORGANIZATION

A standard 8051 based MCU divides the memory into two different sections, the Program Memory and the Data Memory. The Program Memory is used to store the instruction codes, whereas the Data Memory is used to store data or variations during the program execution.

Data Memory occupies a separate address space from Program Memory. In N78E517A, there are 256 bytes of internal scratch-pad RAM and up to 64k bytes of memory space for external Data Memory. The MCU generates the 16-bit or 8-bit addresses, read and write strobe signals ($\overline{RD}$ and $\overline{WR}$, respectively) during external Data Memory access. For many applications which need more internal RAM, N78E517A possesses on-chip 1k bytes of RAM (called XRAM) accessed by MOVX instruction.

The whole embedded flash is divided into 4 banks, APROM for storage of user's program code, Data Flash for parameter data storage, LDROM for ISP program and CONFIG bytes. Each bank is accumulated page by page and the page size is 256 bytes. The flash control unit supports Page Erase, Byte Program, and Byte Read modes. The external writer tools though specific I/O pins or the internal ISP (In System Programming) function can both performs these modes.

5.1 Internal Program Memory

Program Memory is the one, which stores the program codes to execute, as shown in Figure 5–1. While $\overline{EA}$ pin is pulled high and after any reset, the CPU begins execution from location 0000H where should be the starting point of the user's application code. To service the interrupts, the interrupt service locations (called interrupt vectors) should be located in the Program Memory. Each interrupt is assigned with a fixed location in the Program Memory. The interrupt causes the CPU to jump to that location with where it commences execution of the interrupt service routine (ISR). External Interrupt 0, for example, is assigned to location 0003H. If External Interrupt 0 is going to be used, its service routine must begin at location 0003H. If the interrupt is not going to be used, its service location is available as general purpose Program Memory.

The interrupt service locations are spaced at an interval of 8 bytes: 0003H for External Interrupt 0, 000BH for Timer 0, 0013H for External Interrupt 1, 001BH for Timer 1, etc. If an interrupt service routine is short enough (as is often the case in control applications), it can reside entirely within that 8-byte interval. However longer service routines should use a JMP instruction to skip over subsequent interrupt locations if other interrupts are in use.

N78E517A provides two internal Program Memory bank APROM and LDROM. Although they both behave the same as the standard 8051 Program Memory, they play different rules according to their ROM size. The APROM on N78E517A can be 64k-byte size maximum. The user's main program code is normally put inside.

5.4 On-chip XRAM

N78E517A provides additional on-chip auxiliary RAM called XRAM to enlarge RAM space. The 1024 bytes of XRAM (000H to 3FFH) are indirectly accessed by move external instruction MOVX. For details, see Section 8. "AUXILIARY RAM (XRAM)" on page 30.

5.5 External Data Memory

Access to external Data Memory can use either a 16-bit address (using 'MOVX @DPTR') or an 8-bit address (using 'MOVX @Ri', i = 0 or 1). For another 1k-byte XRAM exists, remember the bit XRAMEN (CHPCON.4) should be cleared as logic 0 in order to access the range of 000H to 3FFH address of the external Data Memory.

16-bit addresses are often used to access up to 64k bytes of external RAM. Whenever a 16-bit address is used, P0, P2, P3.7 and P3.6 serve as the low byte address/data, the high byte address, $\overline{RD}$ strobe and $\overline{WR}$ strobe signals respectively. Meanwhile the pins listed above cannot be used as general purpose I/O during external Data Memory access.

8-bit addresses are often used in conjunction with one or more other I/O lines to page the RAM. For example, if a 1k-byte external RAM is used, Port 0 serves as a multiplexed address/data bus to the RAM, and 2 pins of Port 2 are used to page the RAM. The CPU generates $\overline{RD}$ and $\overline{WR}$ (alternate functions of P3.7 and P3.6) to strobe the memory. In 8-bit addressing mode, P2 pins other than the two pins for RAM paging are free for general purpose I/O usage. It facilitates P2 application. Of course, the user may use any other I/O lines instead of P2 to page the RAM.

In all cases, the low byte of the address is time-multiplexed with the data byte on Port 0. ALE (Address Latch Enable) should be used to capture the address byte into an external latch. The address byte is valid at the negative transition of ALE. Then, in a write cycle, the data byte to be written appears on Port 0 just before $\overline{WR}$ is activated, and remains there until after $\overline{WR}$ is deactivated. In a read cycle, the incoming byte is accepted at Port 0 just before the read strobe is deactivated. During any access to external memory, the CPU writes 0FFH to the Port 0 latch (P0 in SFRs), thus obliterating whatever information the Port 0 SFR may have been holding.

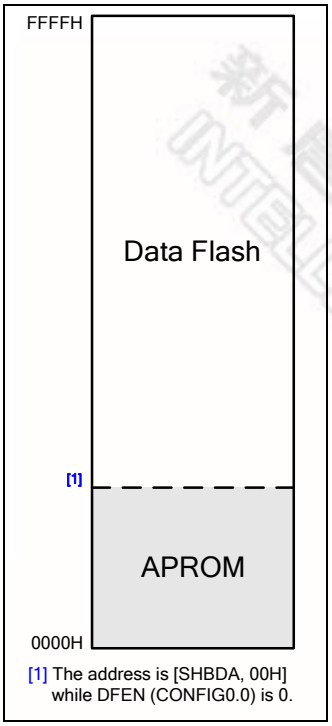


Figure 5–6. N78E517A Data Flash

CONFIG0

7	6	5	4	3	2	1	0
CBS	-	-	-	-	MOVCL	LOCK	DFEN
r/w	-	-	-	-	r/w	r/w	r/w

unprogrammed value: 1111 1111b

Bit	Name	Description
0	DFEN	**Data Flash enable.** 1 = There is no Data Flash space. The APROM size is 64k-byte. 0 = Data Flash exists. The Data Flash and APROM share 64k bytes depending on SHBDA setting.

CONFIG1

7	6	5	4	3	2	1	0
CHBDA[7:0][1]							
r/w							

unprogrammed value: 1111 1111b

Bit	Name	Description
7:0	CHBDA[7:0]	**CONFIG high byte of Data Flash starting address.** This byte is valid only when DFEN (CONFIG0.0) being 0 condition. It is used to determine the starting address of the Data Flash.

[1] Note that there will be no APROM if setting CHBDA 00H. CPU will execute codes in the external Program Memory.

6. SPECIAL FUNCTION REGISTER (SFR)

The N78E517A uses Special Function Registers (SFRs) to control and monitor peripherals and their modes. The SFRs reside in the register locations 80-FFH and are accessed by direct addressing only. Some of the SFRs are bit-addressable. It is very useful in cases where users would like to modify a particular bit directly without changing other bits. Those which are bit-addressable SFRs end their addresses as 0H or 8H. N78E517A contains all the SFRs presenting in the standard 8051. However some additional SFRs are built in. Therefore, some of unused bytes in the original 8051 have been given new functions. The SFRs is listed below.

Table 6–1. N78E517A Special Function Registers Mapping

F8	-	-	-	-	-	-	-	-	**FF**
F0	**B**	-	-	SPCR	SPSR	SPDR	-	-	**F7**
E8	-	-	-	-	-	-	-	-	**EF**
E0	**ACC**	-	-	-	-	-	-	-	**E7**
D8	**P4**	PWMP	PWM0	PWM1	PWMCON0	PWM2	PWM3	-	**DF**
D0	**PSW**	-	-	-	-	-	-	-	**D7**
C8	**T2CON**	T2MOD	RCAP2L	RCAP2H	TL2	TH2	PWMCON1	PWM4	**CF**
C0	**XICON**	-	-	-	-	-	-	TA	**C7**
B8	**IP**	-	IPH	EIPH	EIP	EIE	-	-	**BF**
B0	**P3**	-	-	-	-	-	-	-	**B7**
A8	**IE**	-	WDCON	PDCON	PMC	-	ISPFD	ISPCN	**AF**
A0	**P2**	XRAMAH	-	-	ISPTRG	-	ISPAL	ISPAH	**A7**
98	**SCON**	SBUF	-	-	SHBDA	-	-	CHPCON	**9F**
90	**P1**	-	-	-	-	-	RSR	-	**97**
88	**TCON**	TMOD	TL0	TL1	TH0	TH1	AUXR	-	**8F**
80	**P0**	SP	DPL	DPH	-	-	P0OR	PCON	**87**

In Bold	bit-addressable
-	reserved

Note that the reserved SFR addresses must be kept in their own initial states. Users should never change their values.

10. TIMERS/COUNTERS

N78E517A has three 16-bit programmable timers/counters.

10.1 Timer/Counters 0 and 1

Timer/Counter 0 and 1 on N78E517A are two 16-bit Timer/Counters. Each of them has two 8 bit registers which form the 16 bit counting register. For Timer/Counter 0 they are TH0, the upper 8 bits register, and TL0, the lower 8 bit register. Similarly Timer/Counter 1 has two 8 bit registers, TH1 and TL1. TCON and TMOD can configure modes of Timer/Counter 0 and 1.

The Timer or Counter function is selected by the C/$\overline{T}$ bit in TMOD. Each Timer/Counter has its own selection bit. TMOD.2 selects the function for Timer/Counter 0 and TMOD.6 selects the function for Timer/Counter 1

When configured as a “Timer”, the timer counts clock cycles. The timer clock is 1/6 of the peripheral clock (F_{PERIPH}). In the “Counter” mode, the register increases on the falling edge of the external input pins T0 for Timer 0 and T1 for Timer 1. If the sampled value is high in one machine-cycle and low in the next, a valid 1 to 0 transition on the pin is recognized and the count register increases.

In addition, each Timer/Counter can be set to operate in any one of four possible modes. Bits M0 and M1 in TMOD do the mode selection.

TMOD – Timer 0 and 1 Mode

7	6	5	4	3	2	1	0
GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Address: 89H reset value: 0000 0000b

Bit	Name	Description
7	GATE	**Timer 1 gate control.** 0 = Timer 1 will clock when TR1 = 1 regardless of $\overline{INT1}$ logic level. 1 = Timer 1 will clock only when TR1 = 1 and $\overline{INT1}$ is logic 1.
6	C/$\overline{T}$	**Timer 1 Counter/Timer select.** 0 = Timer 1 is incremented by internal peripheral clocks. 1 = Timer 1 is incremented by the falling edge of the external pin T1.
5	M1	**Timer 1 mode select.**
4	M0	M1 M0 Timer 1 Mode 0 0 Mode 0: 8-bit Timer/Counter with 5-bit pre-scalar (TL1[4:0]) 0 1 Mode 1: 16-bit Timer/Counter 1 0 Mode 2: 8-bit Timer/Counter with auto-reload from TH1 1 1 Mode 3: Timer 1 halted

TH0 – Timer 0 High Byte

7	6	5	4	3	2	1	0
TH0[7:0]							
r/w							

Address: 8CH reset value: 0000 0000b

Bit	Name	Description
7:0	TH0[7:0]	**Timer 0 high byte.** The TH0 register is the high byte of the 16-bit Timer 0.

TL1 – Timer 1 Low Byte

7	6	5	4	3	2	1	0
TL1[7:0]							
r/w							

Address: 8BH reset value: 0000 0000b

Bit	Name	Description
7:0	TL1[7:0]	**Timer 1 low byte.** The TL1 register is the low byte of the 16-bit Timer 1.

TH1 – Timer 1 High Byte

7	6	5	4	3	2	1	0
TH1[7:0]							
r/w							

Address: 8DH reset value: 0000 0000b

Bit	Name	Description
7:0	TH1[7:0]	**Timer 1 high byte.** The TH1 register is the high byte of the 16-bit Timer 1.

10.1.1 Mode 0 (13-bit Timer)

In Mode 0, the Timer/Counter is a 13-bit counter. The 13-bit counter consists of THx and the five lower bits of TLx. The upper three bits of TLx are ignored. The Timer/Counter is enabled when TRx is set and either GATE is 0 or $\overline{INTx}$ is 1. Gate = 1 allows the Timer to calculate the pulse width on external input pin $\overline{INTx}$. When the 13-bit value moves from 1FFFH to 0000H, the Timer overflow flag TFx is set and an interrupt occurs if enabled. Note that the peripheral clock is $F_{OSC}/2$ in 12T mode and is F_{OSC} in 6T mode. See Section 20. “CLOCK SYSTEM” on page 103.

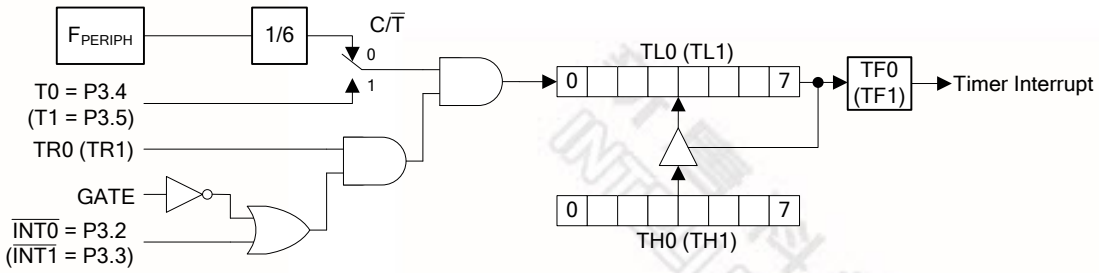


Figure 10–3. Timer/Counter 0 and 1 in Mode 2

10.1.4 Mode 3 (Two Separate 8-bit Timers)

Mode 3 has different operating methods for the two Timer/Counters. For Timer/Counter 1, Mode 3 simply freezes the counter. Timer/Counter 0, however, configures TL0 and TH0 as two separate 8 bit count registers in this mode. TL0 uses the Timer/Counter 0 control bits C/$\overline{T}$, GATE, TR0, $\overline{INT0}$, and TF0. The TL0 also can be used as a 1-to-0 transition counter on pin T0 as determined by C/$\overline{T}$ (TMOD.2). TH0 is forced as a clock cycle counter and takes over the usage of TR1 and TF1 from Timer/Counter 1. Mode 3 is used in case which an extra 8 bit timer is needed. If Timer/Counter 0 is configured in Mode 3, Timer/Counter 1 can be turned on or off by switching it out of or into its own Mode 3. It can still be used in Modes 0, 1 and 2 although its flexibility is restricted. It no longer has control over its overflow flag TF1 and the enable bit TR1. However Timer 1 can still be used as a Timer/Counter and retains the use of GATE and $\overline{INT1}$ pin. It can be used as a baud rate generator for the serial port or other application not requiring an interrupt.

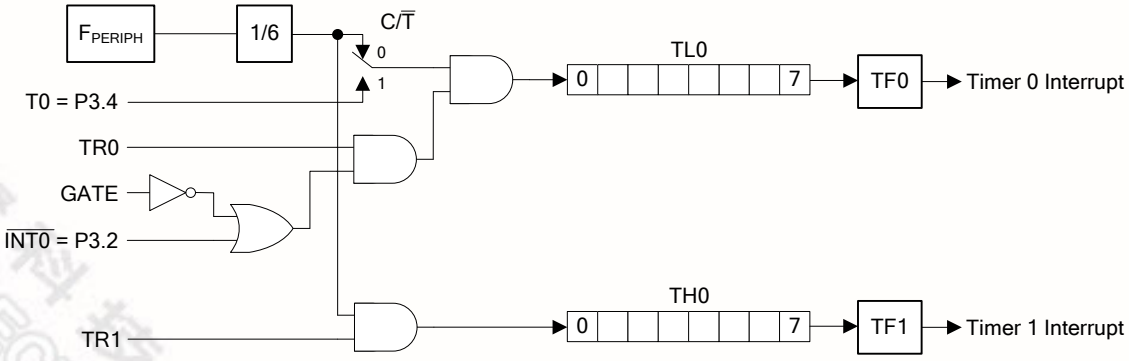


Figure 10–4. Timer/Counter 0 in Mode 3

Transmission is initiated by any writing instructions to SBUF. Transmission takes place on TXD pin. First the start bit comes out, the 8-bit data follows to be shifted out and then ends with a stop bit. After the stop bit appears, TI (SCON.1) will be set to indicate one byte transmission complete. All bits are shifted out depending on the rate determined by the baud rate generator.

Once the baud rate generator is activated and REN (SCON.4) is 1, the reception can begin at any time. Reception is initiated by a detected 1-to-0 transition at RXD. Data will be sampled and shifted in at the selected baud rate. In the midst of the stop bit, certain conditions must be met to load SBUF with the received data:

1. RI (SCON.0) = 0, and

2. Either SM2 (SCON.5) = 0, or the received stop bit = 1 while SM2 = 1.

If these conditions are met, then the SBUF will be loaded with the received data, the RB8 (SCON.2) with stop bit, and RI will be set. If these conditions fail, there will be no data loaded and RI will remain 0. After above receiving progress, the serial control will look forward another 1-0 transition on RXD pin in order to start next data reception.

13.3 Mode 2

Mode 2 supports asynchronous, full duplex serial communication. Different from Mode1, there are 11 bits to be transmitted or received. They are a start bit (logic 0), 8 data bits (LSB first), a programmable 9th bit TB8 or RB8 bit and a stop bit (logic 1). The most common use of 9th bit is to put the parity bit in it. The baud rate is fixed as 1/32 or 1/64 the oscillator frequency depending on SMOD bit. (Condition above is under 12T mode. Under 6T mode, the baud rate will be 1/16 or 1/32 the oscillator frequency.) Figure 13–3 shows a simplified functional diagram of the serial port in Mode 2 and associated timings for transmit and receive.

13.5 Baud Rate

Table 13–2. UART Baud Rate Formulas

UART mode	Baud rate clock source	EN6T (CONFIG3.6) value	
		1 (12T mode)	0 (6T mode)
0	Oscillator	$F_{OSC}/12$	$F_{OSC}/6$
2	Oscillator	$\frac{2^{SMOD}}{64}\times F_{OSC}$	$\frac{2^{SMOD}}{32}\times F_{OSC}$
1 or 3	Timer/Counter 1 overflow[1]	$\frac{2^{SMOD}}{32}\times\frac{F_{OSC}}{12\times(256-TH1)}$	$\frac{2^{SMOD}}{16}\times\frac{F_{OSC}}{12\times(256-TH1)}$
	Timer/Counter 2 overflow[2]	$\frac{F_{OSC}}{32\times(65536-(RCAP2H,RCAP2L))}$ [3]	$\frac{F_{OSC}}{16\times(65536-(RCAP2H,RCAP2L))}$

[1] Timer 1 is configured as a timer in auto-reload mode (Mode 2).
[2] Timer 2 is configured as a timer in baud rate generator mode.
[3] (RCAP2H,RCAP2L) in the formula means $256\times RCAP2H+RCAP2L$.

Note that in using Timer 1 as the baud rate generator, the interrupt should be disabled. In using Timer 2, the interrupt is automatically switched off. The Timer itself can be configured for either “Timer” or “Counter” operation. Timer 1 can be in any of its 3 running modes. In the most typical applications, it is configured for “Timer” operation, in the auto-reload mode (Mode2). If Timer 1 is used as the baud rate generator, the reloaded value is stored in TH1. Therefore the baud rate is determined by TH1 value. If Timer 2 is used, the user should configure it in baud rate generator mode (RCLK or TCLK in T2CON is logic 1) and give 16-bit reloaded value in RCAP2H and RCAP2L.

Table 13–3 lists various commonly used baud rates and how they can be obtained from Timer 1. In this mode, Timer 1 as an auto-reload Timer operates in 12T mode and SMOD (PCON.7) is 0. Table 13–4 is for Timer 2 as the baud rate generator. Timer 2 operates in baud rate generator mode in 12T mode. In 6T mode, the baud rate generated from both Timer 1 and Timer 2 overflows will be doubled.

Table 13–3. Timer 1 Generated Commonly Used Baud Rates

TH1 reload value	Oscillator Frequency (MHz)				
	11.0592	14.7456	18.432	22.1184	36.864
Baud Rate					
57600				FFh	
38400		FFh			
19200		FEh		FDh	FBh

TH1 reload value	Oscillator Frequency (MHz)				
	11.0592	14.7456	18.432	22.1184	36.864
Baud Rate					
9600	FDh	FCh	FBh	FAh	F6h
4800	FAh	F8h	F6h	F4h	ECh
2400	F4h	F0h	ECh	E8h	D8h
1200	E8h	E0h	D8h	D0h	B0h
300	A0h	80h	60h	40h	

Table 13–4. Timer 2 Generated Commonly Used Baud Rates

RCAP2H, RCAP2L reload value	Oscillator Frequency (MHz)				
	11.0592	14.7456	18.432	22.1184	36.864
Baud Rate					
115200	FFh, FDh	FFh, FCh	FFh, FBh	FFh, FAh	FFh, F6h
57600	FFh, FAh	FFh, F8h	FFh, F6h	FFh, F4h	FFh, ECh
38400	FFh, F7h	FFh, F4h	FFh, F1h	FFh, EEh	FFh, E2h
19200	FFh, EEh	FFh, E8h	FFh, E2h	FFh, DCh	FFh, C4h
9600	FFh, DCh	FFh, D0h	FFh, C4h	FFh, B8h	FFh, 88h
4800	FFh, B8h	FFh, A0h	FFh, 88h	FFh, 70h	FFh, 10h
2400	FFh, 70h	FFh, 40h	FFh, 10h	FEh, E0h	FEh, 20h
1200	FEh, E0h	FEh, 80h	FEh, 20h	FDh, C0h	FCh, 40h
300	FBh, 80h	FAh, 00h	F8h, 80h	F7h, 00h	F1h, 00h

13.6 Multiprocessor Communication

N78E517A multiprocessor communication feature of UART lets a Master device send a multiple frame serial message to a Slave device in a multi-slave configuration. It does this without interrupting other slave devices that may be on the same serial line. This feature can be used only in UART mode 2 or 3 mode. After 9 data bits are received. The 9th bit value is written to RB8 (SCON.2). The user can enable this function by setting SM2 (SCON.5) as a logic 1 so that when the stop bit is received, the serial interrupt will be generated only if RB8 is 1. When the SM2 bit is 1, serial data frames that are received with the 9th bit as 0 do not generate an interrupt. In this case, the 9th bit simply separates the address from the serial data.

When the Master device wants to transmit a block of data to one of several slaves on a serial line, it first sends out an address byte to identify the target slave. Note that in this case, an address byte differs from a data byte: In an address byte, the 9th bit is 1 and in a data byte, it is 0. The address byte interrupts all slaves so that each slave can examine the received byte and see if it is being addressed. The addressed slave then clears its SM2

14.7 Mode Fault Detection

The Mode Fault detection is useful in a system where more than one SPI devices might become Masters at the same time. It may induce data contention. When the SPI device is configured as a Master and the $\overline{SS}$ input line is configured for Mode Fault input depending on Table 14–1. Slave Select Pin Configurations, a Mode Fault error occurs once the $\overline{SS}$ is pulled low by others. It indicates that some other SPI device is trying to address this Master as if it is a Slave. Instantly the MSTR and SPIEN control bits in the SPCR are cleared via hardware to disable SPI, Mode Fault flag MODF (SPSR.4) is set and an interrupt is generated if ESPI (EIE .0) and EA are enabled.

14.8 Write Collision Error

The SPI is signal buffered in the transfer direction and double buffered in the receiving direction. New data for transmission cannot be written to the shift register until the previous transaction is complete. Write collision occurs while an attempt was made to write data to the SPDR while a transfer was in progress. SPDR is not double buffered in the transmit direction. Any writing to SPDR cause data to be written directly into the SPI shift register. Once a write collision error is generated, WCOL (SPSR.6) will be set as a 1 via hardware to indicate a write collision. In this case, the current transferring data continues its transmission. However the new data that caused the collision will be lost. Although the SPI logic can detect write collisions in both Master and Slave modes, a write collision is normally a Slave error because a Slave has no indicator when a Master initiates a transfer. During the receive of Slave, a write to SPDR causes a write collision in Slave mode. WCOL flag needs to be cleared via software.

14.9 Overrun Error

For receiving data, the SPI is double buffered in the receiving direction. The received data is transferred into a parallel read data buffer so the shifter is free to accept a second serial byte. However, the received data must be read from SPDR before the next data has been completely shifted in. As long as the first byte is read out of the read data buffer and SPIF is cleared before the next byte is ready to be transferred, no overrun error condition occurs. Otherwise the overrun error occurs. In this condition, the second byte data will not be successfully received into the read data register and the previous data will remains. If overrun occur, SPIOVF (SPSR.5) will be set via hardware. An SPIOVF setting will also require an interrupt if enabled. Figure 14–7. SPI Overrun Waveform shows the relationship between the data receiving and the overrun error.

Bit	Name	Description
5	ET2	**Enable Timer 2 interrupt.** 0 = Disable all Timer 2 interrupts. 1 = Enable interrupt generated by TF2 (T2CON.7) or EXF2 (T2CON.6).
4	ES	**Enable serial port (UART) interrupt.** 0 = Disable all UART interrupts. 1 = Enable interrupt generated by TI (SCON.1) or RI (SCON.0).
3	ET1	**Enable Timer 1 interrupt.** 0 = Disable Timer 1 interrupt 1 = Enable interrupt generated by TF1 (TCON.7).
2	EX1	**Enable external interrupt 1.** 0 = Disable external interrupt 1. 1 = Enable interrupt generated by $\overline{INT1}$ pin (P3.3).
1	ET0	**Enable Timer 0 interrupt.** 0 = Disable Timer 0 interrupt 1 = Enable interrupt generated by TF0 (TCON.5).
0	EX0	**Enable external interrupt 0.** 0 = Disable external interrupt 0. 1 = Enable interrupt generated by $\overline{INT0}$ pin (P3.2).

EIE – Extensive Interrupt Enable

7	6	5	4	3	2	1	0
-	-	-	-	-	EBOD	EPDT	ESPI
-	-	-	-	-	r/w	r/w	r/w

Address: BDH reset value: 0000 0000b

Bit	Name	Description
7:3	-	**Reserved.**
2	EBOD	**Enable Brown-out detection interrupt.** 0 = Disable Brown-out detection interrupt. 1 = Enable interrupt generated by BOF (PMC.3).
1	EPDT	**Enable Power Down waking-up timer interrupt.** 0 = Disable Power Down waking-up timer interrupt 1 = Enable interrupt generated by PDTF (PDCON.5).
0	ESPI	**Enable SPI interrupt.** 0 = Disable SPI interrupt. 1 = Enable interrupt generated by SPIF (SPSR.7), SPIOVF (SPSR.5), or MODF (SPSR.4).

IP – Interrupt Priority (bit-addressable)[1]

7	6	5	4	3	2	1	0
-	-	PT2	PS	PT1	PX1	PT0	PX0
-	-	r/w	r/w	r/w	r/w	r/w	r/w

Address: B8H reset value: 0000 0000b

Bit	Name	Description
7:6	-	**Reserved.**
5	PT2	**Timer 2 interrupt priority low bit.**

21. POWER MONITORING

In order to prevent incorrect execution during power up and power drop, N78E517A provides three power monitor functions, power-on detection, Brown-out detection, and low power detection.

21.1 Power-on Detection

The power-on detection function is designed for detecting power up after power voltage reaches to a level about 2.0V where the system can work. After power-on detected, the POF (PCON.4) will be set 1 to indicate a cold reset, a power-on reset complete. The POF flag can be cleared via software.

21.2 Brown-out Detection

The other power monitoring function, Brown-out detection circuit is for monitoring the V_{DD} level during execution. There are four programmable Brown-out trigger levels available for wide voltage applications. The four nominal levels are 2.2V, 2.7V, 3.8V, and 4.5V selected via setting CBOV[1:0] in CONFIG2. When V_{DD} drops to the selected Brown-out trigger level (V_{BOD}), the Brown-out detection logic will either reset the CPU or request a Brown-out interrupt. The user may determine Brown-out reset or interrupt enable according to different application systems.

The Brown-out detection will request the interrupt while V_{DD} drops below V_{BOD} while BORST (PMC.4) is 0. In this case, BOF (PMC.3) will set as a 1. After the user cleared this flag whereas V_{DD} remains below V_{BOD}, BOF will not set again. BOF just acknowledge the user a power drop occurs. The BOF will set 1 after V_{DD} goes higher than V_{BOD} to indicate a power resuming. The Brown-out circuit provides an useful status indicator BOS (PMC.0), which is helpful to tell a Brown-out event or power resuming event occurrence. If BORST bit is set, this will enable Brown-out reset function. After a Brown-out reset, BORF (RSR.2) will set 1 via hardware. It will not be altered by reset other than power-on. Software can clear this bit. V_{BOD} has a hysteresis of 20-200mV.

The Brown-out detection circuit also provides a low power Brown-out detection mode for power saving. When LPBOD is set 1, the Brown-out detection repeatedly senses the power voltage about every 12.8ms. For the interval counting, the internal 10kHz RC oscillator will turn on in Brown-out low power mode. Note that the hysteresis feature will disappear in low power Brown-out detection mode.

Figure 26–2. Supply Current Under 12T Mode, External Clock (2)

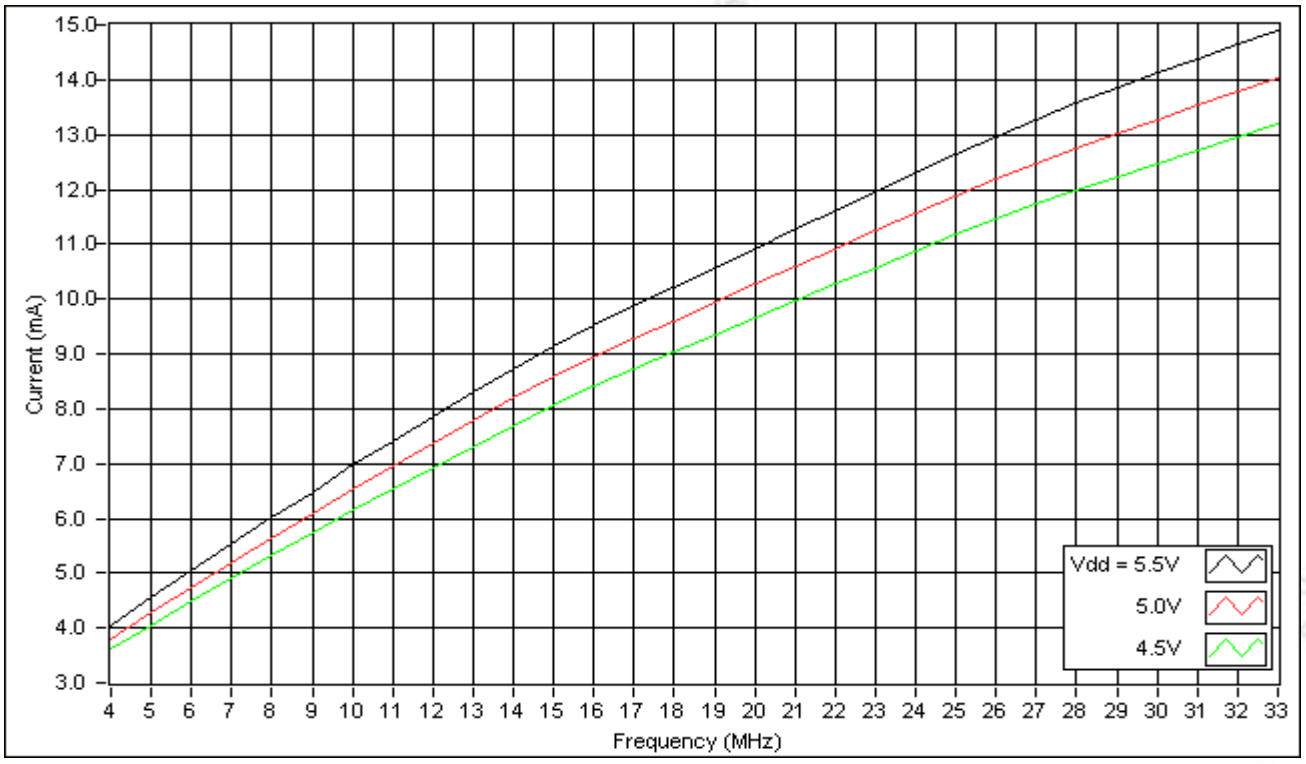


Figure 26–3. Supply Current Under 6T Mode, External Clock (1)

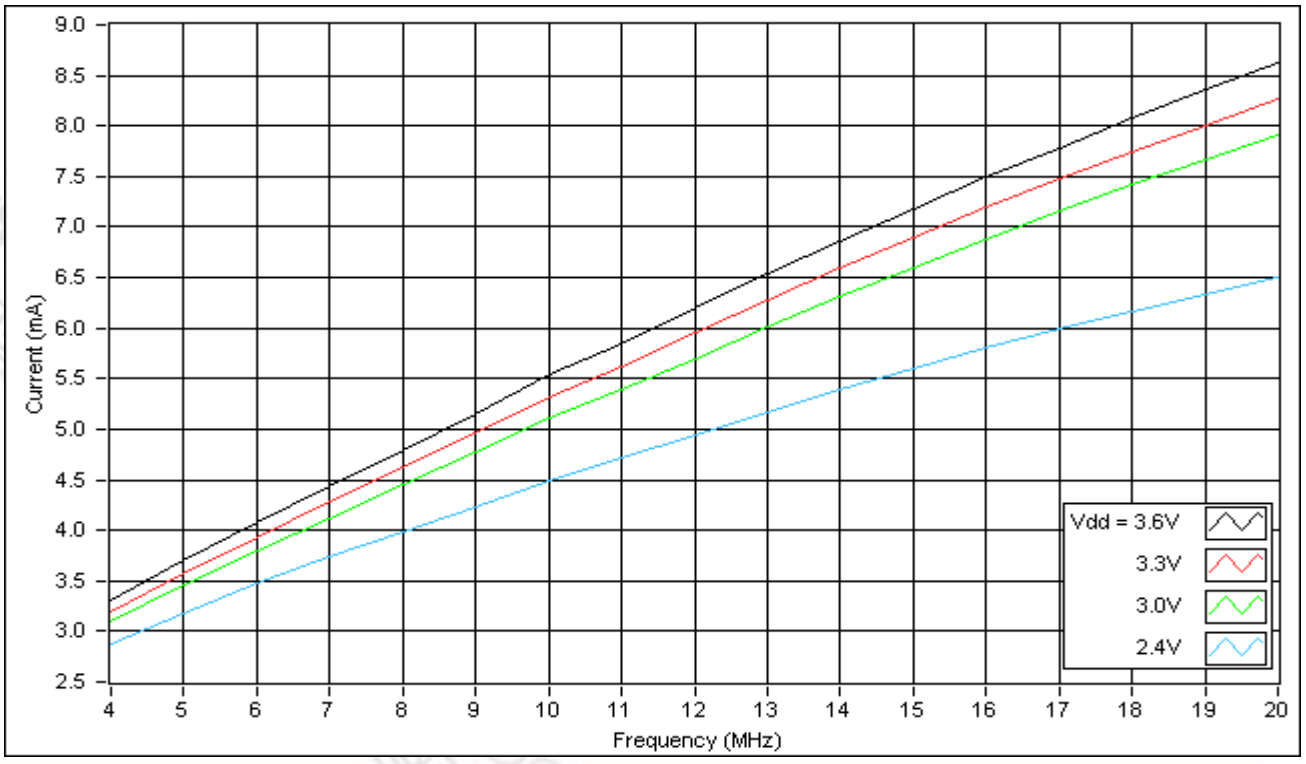


Figure 26–4. Supply Current Under 6T Mode, External Clock (2)

Symbol	Parameter	12T mode		6T mode		Unit
		Min.	Max.	Min.	Max.	
t_{AVWL}	Address valid to $\overline{WR}$ low or $\overline{RD}$ low	4 t_{CLCL} -30		2 t_{CLCL} -30		ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	t_{CLCL} -20		0.5 t_{CLCL} -20		ns
t_{WHQX}	Data hold after $\overline{WR}$	t_{CLCL} -15		0.5 t_{CLCL} -15		ns
t_{RLAZ}	$\overline{RD}$ low to address float		0		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ high to ALE high	t_{CLCL} -15	t_{CLCL} +15	0.5 t_{CLCL} -15	0.5 t_{CLCL} +15	ns

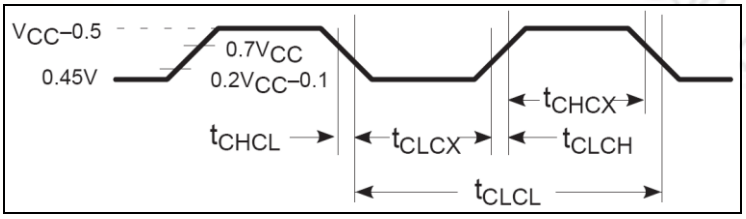


Figure 26–9. External Clock Input Timing

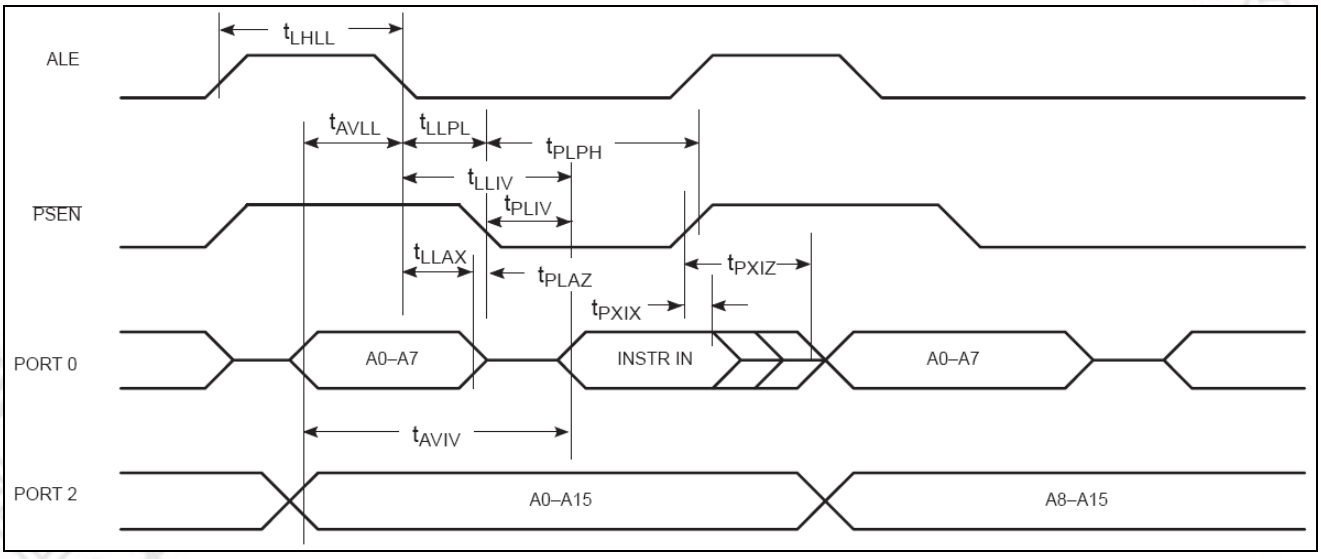
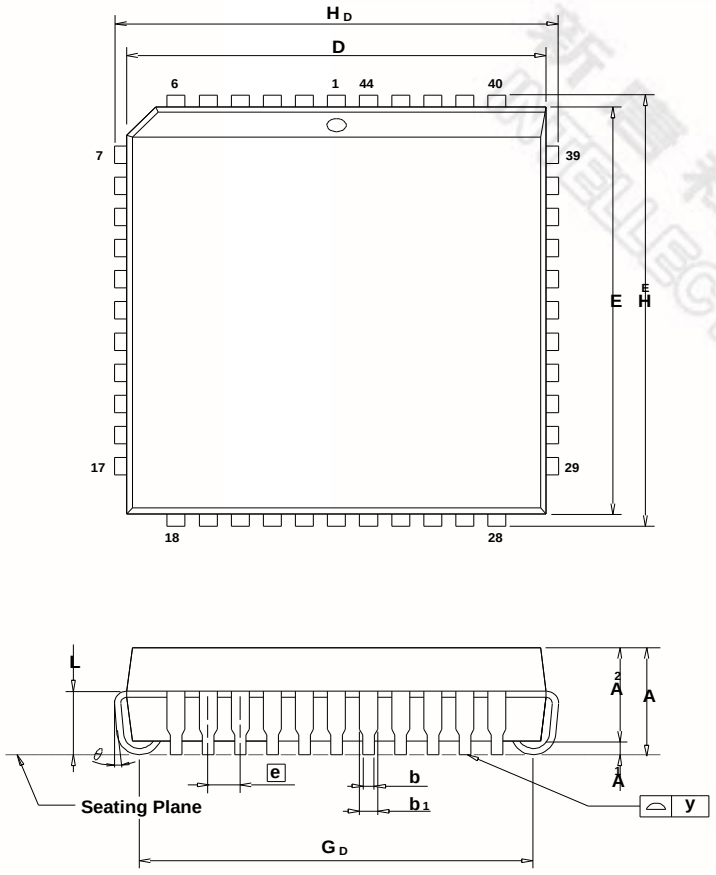
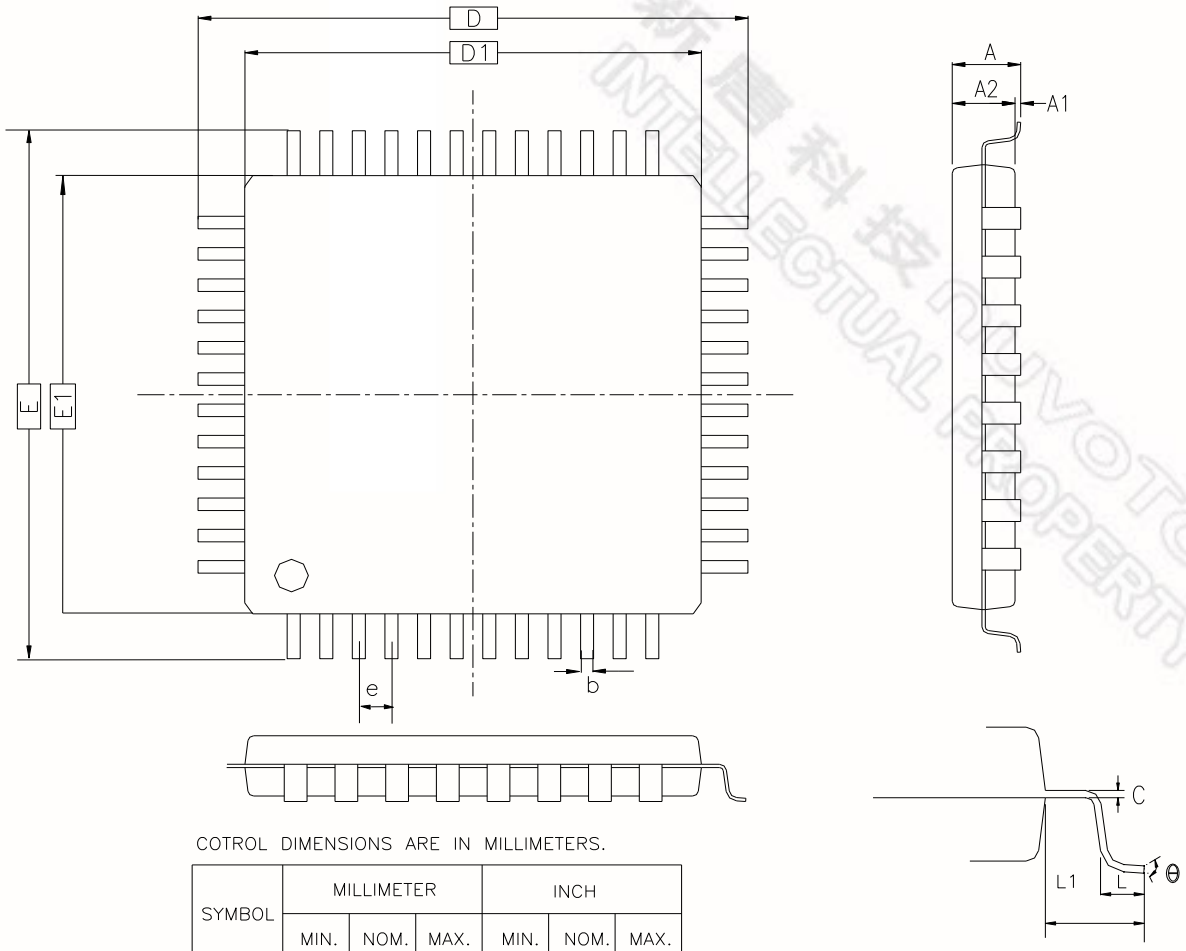


Figure 26–10. External Program Memory Read Cycle



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.185	—	—	4.70
A_1	0.020	—	—	0.51	—	—
A_2	0.145	0.150	0.155	3.68	3.81	3.94
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.36
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e	0.050 BSC			1.27 BSC		
G_D	0.590	0.610	0.630	14.99	15.49	16.00
G_E	0.590	0.610	0.630	14.99	15.49	16.00
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.29	2.54	2.79
y	—	—	0.004	—	—	0.10

Figure 27–2. PLCC-44 Package Dimention



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A_1	0.05	0.10	0.15	0.002	0.004	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
D1	6.90	7.00	7.10	0.272	0.276	0.260
E1	6.90	7.00	7.10	0.272	0.276	0.260
e	0.35	0.50	0.65	0.014	0.020	0.260
D	8.9	9.00	9.10	0.350	0.354	0.358
E	8.9	9.00	9.10	0.350	0.354	0.358
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	—	1.00	—	—	0.039	—
C	0.09	—	0.20	0.0035	—	0.0079
θ	0°	—	7°	0°	—	7°
b	0.17	0.22	0.27	0.007	0.0087	0.011

Figure 27–5. LQFP-48 Package Dimention