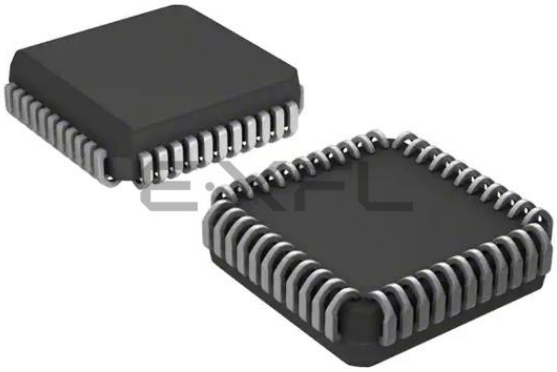

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Details	
Product Status	Last Time Buy
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/n78e517apg

Table 4–1. Pin Description

Pin number				Symbol	Alternate Function		Type[1]	Description
DIP	PLCC	PQFP TQFP	LQFP		1	2		
9	10	4	4	RST			I (ST)	**RESET:** RST pin is a Schmitt trigger input pin for hardware device reset. A high on this pin for two machine-cycles while the system clock is running will reset the device. RST pin has an internal pull-down resistor allowing power-on reset by simply connecting an external capacitor to V_{DD}.
39	43	37	40	P0.0		AD0	D, I/O	**PORT0:** Port 0 is an 8-bit open-drain port by default. Via setting P0UP (P0OR.0), P0 will switch as weakly pulled up internally. P0 has an alternative function as AD[7:0] while external memory accessing. During the external memory access, P0 will output high will be internal strong pulled-up rather than weak pull-up in order to drive out high byte address for external devices.
38	42	36	39	P0.1		AD1	D, I/O	
37	41	35	38	P0.2		AD2	D, I/O	
36	40	34	37	P0.3		AD3	D, I/O	
35	39	33	35	P0.4		AD4	D, I/O	
34	38	32	34	P0.5		AD5	D, I/O	
33	37	31	33	P0.6		AD6	D, I/O	
32	36	30	32	P0.7		AD7	D, I/O	
1	2	40	43	P1.0	T2		I/O	**PORT1:** Port 1 is an 8-bit quasi bi-directional I/O port. Its multifunction pins are for T2, T2EX, PWM0-PWM4, $\overline{SS}$, MOSI, MISO, and SPCLK.
2	3	41	44	P1.1	T2EX		I/O	
3	4	42	45	P1.2			I/O	
4	5	43	46	P1.3	PWM0		I/O	
5	6	44	47	P1.4	PWM1	$\overline{SS}$	I/O	
6	7	1	1	P1.5	PWM2	MOSI	I/O	
7	8	2	2	P1.6	PWM3	MISO	I/O	
8	9	3	3	P1.7	PWM4	SPCLK	I/O	
21	24	18	19	P2.0		A8	I/O	**PORT2:** Port 2 is an 8-bit quasi bi-directional I/O port. It has an alternative function as A[15:8] while external memory accessing. During the external memory access, P2 will output high will be internal strong pulled-up rather than weak pull-up in order to drive out high byte address for external devices.
22	25	19	20	P2.1		A9	I/O	
23	26	20	21	P2.2		A10	I/O	
24	27	21	22	P2.3		A11	I/O	
25	28	22	23	P2.4		A12	I/O	
26	29	23	25	P2.5		A13	I/O	
27	30	24	26	P2.6		A14	I/O	

Table 6–2. N78E517A SFR Description and Reset Values

Symbol	Definition	Address	MSB							LSB[1]	Reset Value[2]
SPDR	SPI data	F5H									0000 0000b
SPSR	SPI status	F4H	SPIF	WCOL	SPIOVF	MODF	DISMODF	-	-	-	0000 0000b
SPCR	SPI control	F3H	SSOE	SPIEN	LSBFE	MSTR	CPOL	CPHA	SPR1	SPR0	0000 0000b
B	B register	F0H	(F7)	(F6)	(F5)	(F4)	(F3)	(F2)	(F1)	(F0)	0000 0000b
ACC	Accumulator	E0H	(E7)	(E6)	(E5)	(E4)	(E3)	(E2)	(E1)	(E0)	0000 0000b
PWM3	PWM3 duty	DEH									0000 0000b
PWM2	PWM2 duty	DDH									0000 0000b
PWMCON0	PWM control 0	DCH	PWM3OE	PWM2OE	PWM3EN	PWM2EN	PWM1OE	PWM0OE	PWM1EN	PWM0EN	0000 0000b
PWM1	PWM1 duty	DBH									0000 0000b
PWM0	PWM0 duty	DAH									0000 0000b
PWMP	PWM period	D9H									0000 0000b
P4	Port 4	D8H	(DF)	(DE)	(DD)	(DC)	(DB) $\overline{\text{INT2}}$	(DA) $\overline{\text{INT3}}$	(D9)	(D8)	1111 1111b
PSW	Program status word	D0H	(D7) CY	(D6) AC	(D5) F0	(D4) RS1	(D3) RS0	(D2) OV	(D1) F1	(D0) P	0000 0000b
PWM4	PWM4 duty	CFH									0000 0000b
PWMCON1	PWM control 1	CEH	-	-	-	-	-	PWM4OE	-	PWM4EN	0000 0000b
TH2	Timer 2 high byte	CDH									0000 0000b
TL2	Timer 2 low byte	CCH									0000 0000b
RCAP2H	Timer 2 reload/capture high byte	CBH									0000 0000b
RCAP2L	Timer 2 reload/capture low byte	CAH									0000 0000b
T2MOD	Timer 2 mode	C9H	-	-	-	-	-	-	T2OE	-	0000 0000b
T2CON	Timer 2 control	C8H	(CF) TF2	(CE) EXF2	(CD) RCLK	(CC) TCLK	(CB) EXEN2	(CA) TR2	(C9) $\overline{\text{C/T2}}$	(C8) $\overline{\text{CP/RL2}}$	0000 0000b
TA	Timed access protection	C7H									0000 0000b
XICON	External interrupt control	C0H	(C7) PX3	(C6) EX3	(C4) IE3	(C4) IT3	(C3) PX2	(C2) EX2	(C1) IE2	(C0) 1IT2	0000 0000b
EIE	Extensive interrupt enable	BDH	-	-	-	-	-	EBOD	EPDT	ESPI	0000 0000b
EIP	Extensive interrupt priority	BCH	-	-	-	-	-	PBOV	PPDT	PSPI	0000 0000b
EIPH	Extensive interrupt priority high	BBH	-	-	-	-	-	PBODH	PPDTH	PSPIH	0000 0000b
IPH	Interrupt priority high	BAH	PX3H	PX2H	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	0000 0000b
IP	Interrupt priority	B8H	(BF) -	(BE) -	(BD) PT2	(BC) PS	(BB) PT1	(BA) PX1	(B9) PT0	(B8) PX0	0000 0000b
P3	Port 3	B0H	(B7) $\overline{\text{RD}}$	(B6) $\overline{\text{WR}}$	(B5) T1	(B4) T0	(B3) $\overline{\text{INT1}}$	(B2) $\overline{\text{INT0}}$	(B1) TXD	(B0) RXD	1111 1111b
ISPCN	ISP flash control	AFH	ISPA17	ISPA16	FOEN	FCEN	FCTRL3	FCTRL2	FCTRL1	FCTRL0	0000 0000b
ISPFD	ISP flash data	AEH									0000 0000b
PMC[3]	Power monitoring control	ACH	BODEN	-	-	BORST	BOF[4]	LPBOD	-	BOS[5]	Power-on[6], XXXX X00Xb Brown-out, XXXX 100Xb Others, XXXX 000Xb
PDCON	Power Down waking-up timer control	ABH	PDTEN	PDTCK	PDTF	-	-	PPS2	PPS1	PPS0	0000 0000b
WDCON[3]	Watchdog Timer control	AAH	WDTEN	WDCLR	-	WIDPD	WDTRF	WPS2	WPS1	WPS0	Power-on[6], X000 0000b Watchdog, X00U 1UUUb Others, X00U UUUUb
IE	Interrupt enable	A8H	(AF) EA	(AE) -	(AD) ET2	(AC) ES	(AB) ET1	(AA) EX1	(A9) ET0	(A8) EX0	0000 0000b
ISPAH	ISP address high byte	A7H									0000 0000b
ISPAL	ISP address low byte	A6H									0000 0000b
ISPTRG[3]	ISP trigger	A4H	-	-	-	-	-	-	-	ISPGO	0000 0000b
XRAMAH	Auxiliary RAM address high byte	A1H	-	-	-	-	-	-	XRAMAH.1	XRAMAH.0	0000 0000b
P2	Port 2	A0H	(A7) A15	(A6) A14	(A5) A13	(A4) A12	(A3) A11	(A2) A10	(A1) A9	(A0) A8	1111 1111b

Table 6–2. N78E517A SFR Description and Reset Values

Symbol	Definition	Address	MSB							LSB[1]	Reset Value[2]
CHPCON[3]	Chip control	9FH	SWRST	ISPF	LDUEN	XRAMEN	-	-	BS	ISPEN	Software[6], 0001 00U0b Others, 0001 00X0b
SHBDA[3]	SFR high byte of Data Flash starting address	9CH									XXXX XXXXb[6]
SBUF	Serial buffer	99H									0000 0000b
SCON	Serial control	98H	(9F) SM0	(9E) SM1	(9D) SM2	(9C) REN	(9B) TB8	(9A) RB8	(99) TI	(98) RI	0000 0000b
RSR	Reset status register	96H	-	-	-	-	-	BORF	-	SWRF	Power-on, 0000 0000b Brown-out, 0000 010Ub Software, 0000 0U01b Others, 0000 0U0Ub
P1	Port 1	90H	(97) PWM4 SPCLK	(96) PWM3 MISO	(95) PWM2 MOSI	(94) PWM1 $\overline{SS}$	(93) PWM0	(92)	(91) T2EX	(90) T2	1111 1111b
AUXR	Auxiliary register	8EH	-	-	-	-	-	-	-	ALEOFF	0000 0000b
TH1	Timer 1 high byte	8DH									0000 0000b
TH0	Timer 0 high byte	8CH									0000 0000b
TL1	Timer 1 low byte	8BH									0000 0000b
TL0	Timer 0 low byte	8AH									0000 0000b
TMOD	Timer 0 and 1 mode	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	0000 0000b
TCON	Timer 0 and 1control	88H	(8F) TF1	(8E) TR1	(8D) TF0	(8C) TR0	(8B) IE1	(8A) IT1	(89) IE0	(88) IT0	0000 0000b
PCON	Power control	87H	SMOD	-	-	POF	GF1	GF0	PD	IDL	Power-on, 0001 0000b Others, 000U 0000b
P0OR	P0 option register	86H	-	-	-	-	-	-	-	P0UP	0000 0000b
DPH	Data pointer high byte	83H									0000 0000b
DPL	Data pointer low byte	82H									0000 0000b
SP	Stack pointer	81H									0000 0111b
P0	Port 0	80H	(87) A7	(86) A6	(85) A5	(84) A4	(83) A3	(82) A2	(81) A1	(80) A0	1111 1111b

[1] ( ) item means the bit address in bit-addressable SFRs.
[2] Reset value symbol description. 0: logic 0, 1: logic 1, U: unchanged, X: see **[4]** - **[6]**.
[3] These SFRs have TA protected writing.
[4] BOF has different power-on reset value according to CBODEN (CONFIG2.7) and CBORST (CONFIG2.4). See Table 21–1. BOF Reset Value.
[5] BOS is a read-only flag decided by V_{DD} level while Brown-out detection is enabled.
[6] These SFRs have bits which are initialized after specified reset by loading certain bits in CONFIG bytes. See Section 24. "CONFIG BYTES" on page 117 for details.

Note that bits marked in "-" must be kept in their own initial states. Users should never change their values.

```
MOV     DPTR,#0123H         ;write #5BH to XRAM with address @0123H.
MOV     A,#5BH
MOVX    @DPTR,A

MOV     DPTR,#0123H         ;read from XRAM with address @0123H.
MOVX    A,@DPTR
```

TH0 – Timer 0 High Byte

7	6	5	4	3	2	1	0
TH0[7:0]							
r/w							

Address: 8CH reset value: 0000 0000b

Bit	Name	Description
7:0	TH0[7:0]	**Timer 0 high byte.** The TH0 register is the high byte of the 16-bit Timer 0.

TL1 – Timer 1 Low Byte

7	6	5	4	3	2	1	0
TL1[7:0]							
r/w							

Address: 8BH reset value: 0000 0000b

Bit	Name	Description
7:0	TL1[7:0]	**Timer 1 low byte.** The TL1 register is the low byte of the 16-bit Timer 1.

TH1 – Timer 1 High Byte

7	6	5	4	3	2	1	0
TH1[7:0]							
r/w							

Address: 8DH reset value: 0000 0000b

Bit	Name	Description
7:0	TH1[7:0]	**Timer 1 high byte.** The TH1 register is the high byte of the 16-bit Timer 1.

10.1.1 Mode 0 (13-bit Timer)

In Mode 0, the Timer/Counter is a 13-bit counter. The 13-bit counter consists of THx and the five lower bits of TLx. The upper three bits of TLx are ignored. The Timer/Counter is enabled when TRx is set and either GATE is 0 or $\overline{INTx}$ is 1. Gate = 1 allows the Timer to calculate the pulse width on external input pin $\overline{INTx}$. When the 13-bit value moves from 1FFFH to 0000H, the Timer overflow flag TFx is set and an interrupt occurs if enabled. Note that the peripheral clock is $F_{OSC}/2$ in 12T mode and is F_{OSC} in 6T mode. See Section 20. “CLOCK SYSTEM” on page 103.

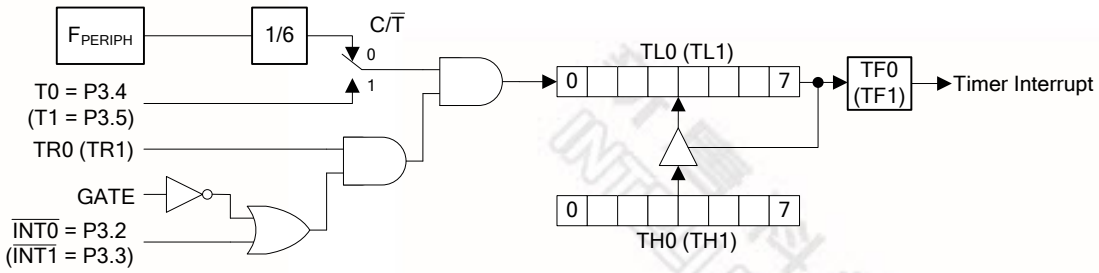


Figure 10–3. Timer/Counter 0 and 1 in Mode 2

10.1.4 Mode 3 (Two Separate 8-bit Timers)

Mode 3 has different operating methods for the two Timer/Counters. For Timer/Counter 1, Mode 3 simply freezes the counter. Timer/Counter 0, however, configures TL0 and TH0 as two separate 8 bit count registers in this mode. TL0 uses the Timer/Counter 0 control bits C/$\overline{T}$, GATE, TR0, $\overline{INT0}$, and TF0. The TL0 also can be used as a 1-to-0 transition counter on pin T0 as determined by C/$\overline{T}$ (TMOD.2). TH0 is forced as a clock cycle counter and takes over the usage of TR1 and TF1 from Timer/Counter 1. Mode 3 is used in case which an extra 8 bit timer is needed. If Timer/Counter 0 is configured in Mode 3, Timer/Counter 1 can be turned on or off by switching it out of or into its own Mode 3. It can still be used in Modes 0, 1 and 2 although its flexibility is restricted. It no longer has control over its overflow flag TF1 and the enable bit TR1. However Timer 1 can still be used as a Timer/Counter and retains the use of GATE and $\overline{INT1}$ pin. It can be used as a baud rate generator for the serial port or other application not requiring an interrupt.

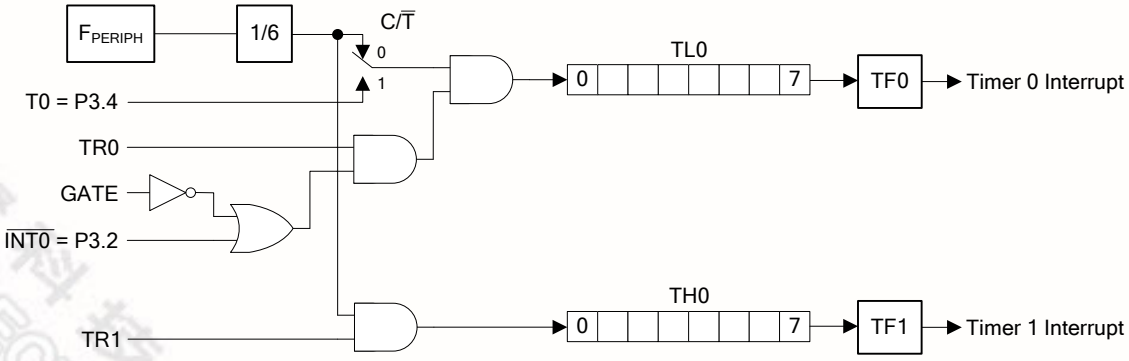


Figure 10–4. Timer/Counter 0 in Mode 3

10.2 Timer/Counter 2

Timer/Counter 2 is a 16-bit up counter, which is configured by the T2MOD and T2CON registers. The count stores in two 8-bit cascade registers TH2 and TL2. Timer/Counter 2 is additionally equipped with a capture or reload capability. It also can be configured as the baud rate generator for UART or a square wave generator. The features listed above could be achieved because of the addition Timer/Counter 2 capture registers RCAP2H and RCAP2L. As with the Timer 0 and Timer 1 counters, there exists considerable flexibility in selecting and controlling the clock and in defining the operating mode. The clock source for Timer/Counter 2 may be selected from either the external T2 pin ($C/\overline{T2}$ (T2CON.1) = 1) or the crystal oscillator ($C/\overline{T2}$ = 0). The clock is then enabled when TR2 (T2CON.2) is a 1, and disabled when TR2 is a 0. The following registers are related to Timer/Counters 2 function.

T2CON – Timer 2 Control (bit-addressable)

7	6	5	4	3	2	1	0
TF2	EXF2	RCLK	TCLK	EXEN2	TR2	$C/\overline{T2}$	$CP/\overline{RL2}$
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Address: C8H reset value: 0000 0000b

Bit	Name	Description
7	TF2	**Timer 2 overflow flag.** This bit is set when Timer 2 overflows. If the Timer 2 interrupt and the global interrupt are enable, setting this bit will make CPU execute Timer 2 interrupt service routine. This bit is not automatically cleared via hardware and must be cleared via software. TF2 will not be set while Timer 2 is configured in the baud rate generator or clock-out mode.
6	EXF2	**Timer 2 external flag.** This bit is set via hardware when a 1-to-0 transition on the T2EX input pin occurs and EXEN2 is logic 1. When the Timer 2 interrupt is enabled, setting this bit causes the CPU to execute the Timer 2 Interrupt service routine. This bit is not automatically cleared via hardware and must be cleared via software.
5	RCLK	**Receive clock flag.** This bit selects which Timer is used for the UART's receive clock in serial Mode 1 or 3. 0 = Timer 1 overflows is used for UART receive baud rate clock. 1 = Timer 2 overflows is used for UART receive baud rate clock.
4	TCLK	**Transmit clock flag.** This bit selects which Timer is used for the UART's transmit clock in serial Mode 1 or 3. 0 = Timer 1 overflows is used for UART transmit baud rate clock. 1 = Timer 2 overflows is used for UART transmit baud rate clock.

12. POWER DOWN WAKING-UP TIMER

12.1 Functional Description of Power Down Waking-up Timer

N78E517A provides another free-running Timer, Power Down waking-up timer which serves as a event timer or a durational system supervisor in a monitoring system which generally operates in Idle or Power Down modes. This timer constructs basically by a set of dividers that divide the peripheral clock. The divider output is selectable and determines the time-out interval. When the time-out interval is fulfilled, it will wake the system up from Idle or Power Down mode and an interrupt event will occur.

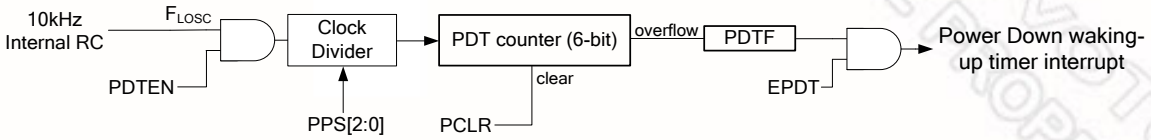


Figure 12–1. Power Down Waking-up Timer Block Diagram

The Power Down waking-up timer should first be reset 00H by using PDCLR(PDCON.6) to ensure that the timer starts from a known state. The PDCLR bit is used to restart the Power Down waking-up timer. This bit is self-cleared thus the user doesn't need to clear it. After writing a 1 to PDCLR, the hardware will automatically clear it. After PDTEN set as 1, the Power Down waking-up timer will start counting clock cycles. The time-out interval is selected by the three bits PPS2, PPS1, and PPS0 (PDCON[2:0]). When the selected time-out occurs, the Power Down waking-up timer will set the interrupt flag PDTF (PDCON.5). The Power Down waking-up timer interrupt enable bit locates at bit 1 in EIE. In general, software should restart the counter to put it into a known state by setting WDCLR.

PDCON – Power Down Waking-up Timer Control

7	6	5	4	3	2	1	0
PDTEN	PDCLR	PDTF	-	-	PPS2	PPS1	PPS0
r/w	w	r/w	-	-	r/w	r/w	r/w

Address: ABH reset value: 0000 0000b

Bit	Name	Description
7	PDTEN	**Power Down waking-up timer enable.** 0 = Disable Power Down waking-up timer. 1 = Enable Power Down waking-up timer. The PDT counter starts running.
6	PDCLR	**Power Down waking-up timer clear.** Setting this bit will reset the Power Down waking-up timer count to 00H. It put the counter in a known state. This bit is written-only and has no need to be cleared via software.
5	PDTF	**Power Down waking-up timer Interrupt Flag.** This bit will be set via hardware when PDT counter overflows. This bit must be cleared via software.

Bit	Name	Description
4:3	-	**Reserved.**
2	PPS2	**Power Down waking-up timer clock pre-scalar select.** These bits determine the scale of the clock divider for PDT counter. The scale is from 1/1 through 1/1024. See Table 12–1.
1	PPS1	
0	PPS0	

The Power Down waking-up time-out interval is determined by the formula $\frac{1}{F_{LOSC} \times clockdividerscalar} \times 64$

where F_{ILRC} is the frequency of internal 10kHz RC. The following table shows an example of the Power Down waking-up time-out interval under different pre-scalars.

Table 12–1. Power Down Waking-up Timer-Out Interval under different pre-scalars

PPS2	PPS1	PPS0	Clock Divider Scale	Typical Power Down Waking-up Time-out Interval (F_{ILRC} = ~10kHz)
0	0	0	1/1	6.40ms
0	0	1	1/4	25.60ms
0	1	0	1/8	51.20ms
0	1	1	1/32	204.80ms
1	0	0	1/64	409.60ms
1	0	1	1/256	1.638s
1	1	0	1/512	3.277s
1	1	1	1/1024	6.554s

12.2 Applications of Power Down Waking-up Timer

The main application of the Power Down waking-up timer is a simple timer. The PDTF flag will be set while the Power Down waking-up timer completes the selected time interval. The software polls the PDTF flag to detect a time-out and the PDCLR allows software to restart the timer. The Power Down waking-up timer can also be used as a very long timer. Every time the time-out occurs, an interrupt will occur if the individual interrupt EPDT (EIE.1) and global interrupt enable EA is set.

In some application of low power consumption, the CPU usually stays in Idle mode when nothing needs to be served to save power consumption. After a while the CPU will be woken up to check if anything needs to be served at an interval of programmed period implemented by Timer 0, 1 or 2. However, the current consumption of Idle mode still keeps at a “mA” level. To further reducing the current consumption to “μA” level, the CPU should stay in Power Down mode when nothing needs to be served, and has the ability of waking up at a pro-

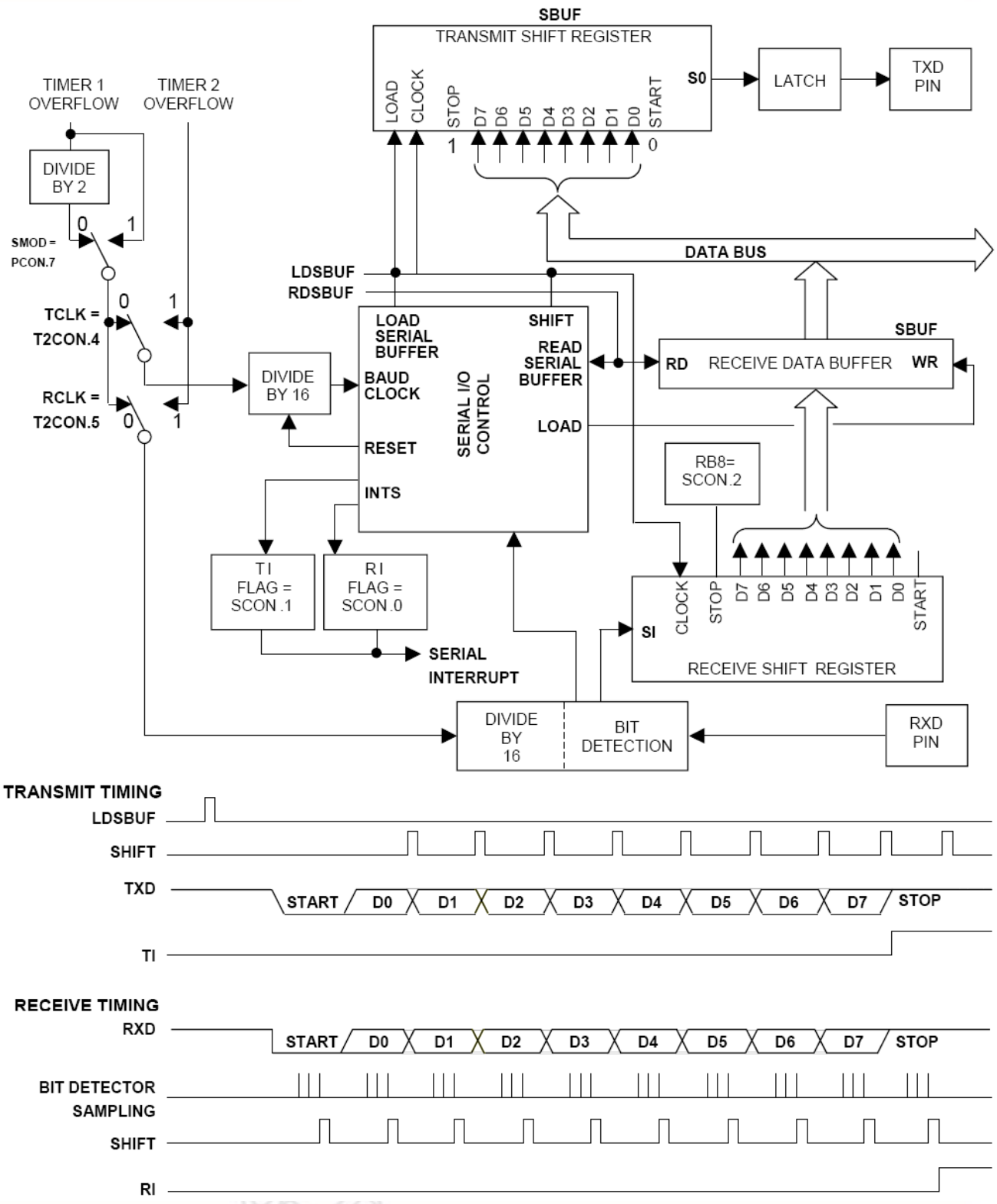


Figure 13–2. Serial Port Mode 1 Function Block and Timing Diagram

Transmission is initiated by any writing instructions to SBUF. Transmission takes place on TXD pin. First the start bit comes out, the 8-bit data follows to be shifted out and then ends with a stop bit. After the stop bit appears, TI (SCON.1) will be set to indicate one byte transmission complete. All bits are shifted out depending on the rate determined by the baud rate generator.

Once the baud rate generator is activated and REN (SCON.4) is 1, the reception can begin at any time. Reception is initiated by a detected 1-to-0 transition at RXD. Data will be sampled and shifted in at the selected baud rate. In the midst of the stop bit, certain conditions must be met to load SBUF with the received data:

1. RI (SCON.0) = 0, and

2. Either SM2 (SCON.5) = 0, or the received stop bit = 1 while SM2 = 1.

If these conditions are met, then the SBUF will be loaded with the received data, the RB8 (SCON.2) with stop bit, and RI will be set. If these conditions fail, there will be no data loaded and RI will remain 0. After above receiving progress, the serial control will look forward another 1-0 transition on RXD pin in order to start next data reception.

13.3 Mode 2

Mode 2 supports asynchronous, full duplex serial communication. Different from Mode1, there are 11 bits to be transmitted or received. They are a start bit (logic 0), 8 data bits (LSB first), a programmable 9th bit TB8 or RB8 bit and a stop bit (logic 1). The most common use of 9th bit is to put the parity bit in it. The baud rate is fixed as 1/32 or 1/64 the oscillator frequency depending on SMOD bit. (Condition above is under 12T mode. Under 6T mode, the baud rate will be 1/16 or 1/32 the oscillator frequency.) Figure 13–3 shows a simplified functional diagram of the serial port in Mode 2 and associated timings for transmit and receive.

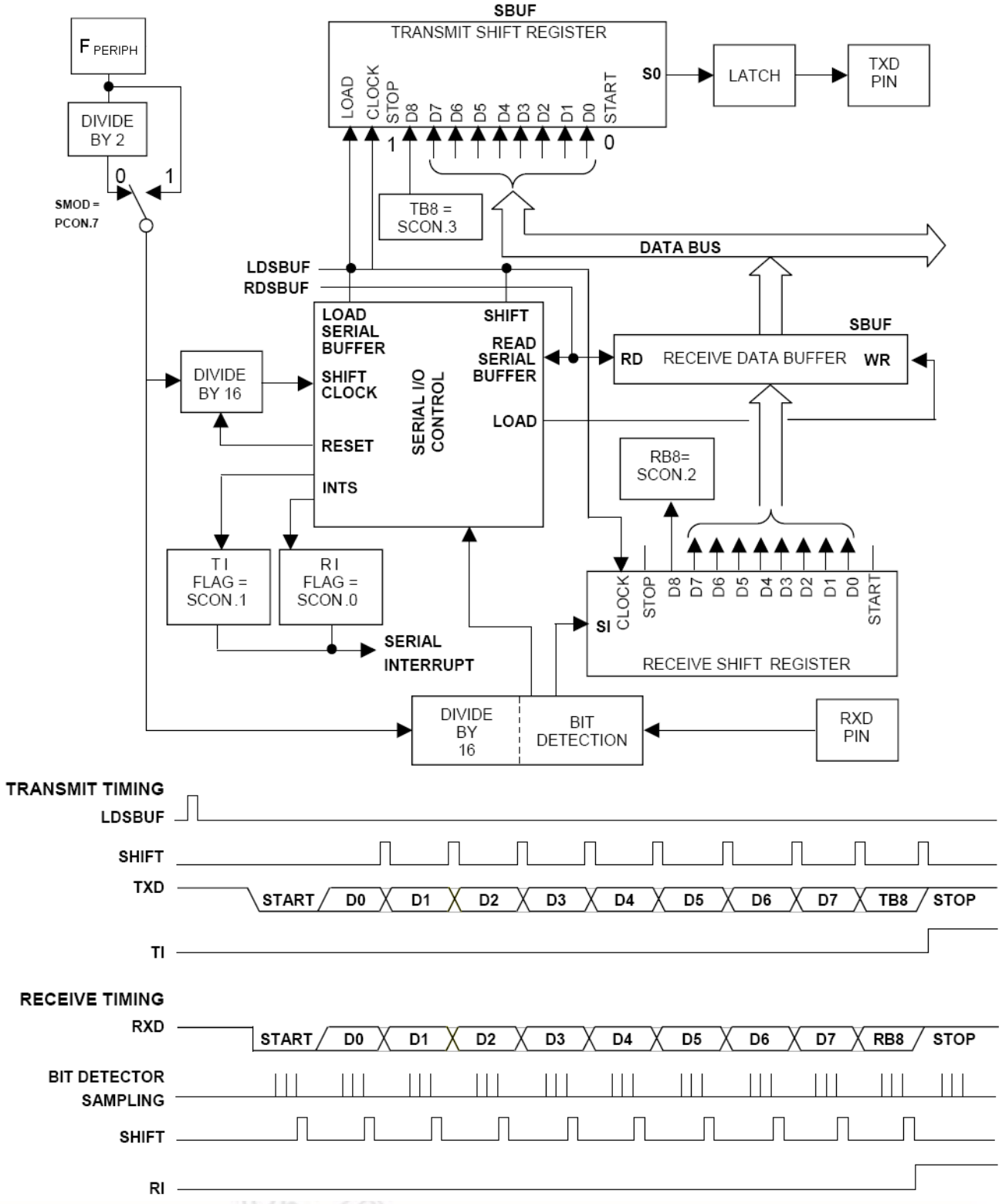


Figure 13–3. Serial Port Mode 2 Function Block and Timing Diagram

13.5 Baud Rate

Table 13–2. UART Baud Rate Formulas

UART mode	Baud rate clock source	EN6T (CONFIG3.6) value	
		1 (12T mode)	0 (6T mode)
0	Oscillator	$F_{OSC}/12$	$F_{OSC}/6$
2	Oscillator	$\frac{2^{SMOD}}{64}\times F_{OSC}$	$\frac{2^{SMOD}}{32}\times F_{OSC}$
1 or 3	Timer/Counter 1 overflow[1]	$\frac{2^{SMOD}}{32}\times\frac{F_{OSC}}{12\times(256-TH1)}$	$\frac{2^{SMOD}}{16}\times\frac{F_{OSC}}{12\times(256-TH1)}$
	Timer/Counter 2 overflow[2]	$\frac{F_{OSC}}{32\times(65536-(RCAP2H,RCAP2L))}$ [3]	$\frac{F_{OSC}}{16\times(65536-(RCAP2H,RCAP2L))}$

[1] Timer 1 is configured as a timer in auto-reload mode (Mode 2).
[2] Timer 2 is configured as a timer in baud rate generator mode.
[3] (RCAP2H,RCAP2L) in the formula means $256\times RCAP2H+RCAP2L$.

Note that in using Timer 1 as the baud rate generator, the interrupt should be disabled. In using Timer 2, the interrupt is automatically switched off. The Timer itself can be configured for either “Timer” or “Counter” operation. Timer 1 can be in any of its 3 running modes. In the most typical applications, it is configured for “Timer” operation, in the auto-reload mode (Mode2). If Timer 1 is used as the baud rate generator, the reloaded value is stored in TH1. Therefore the baud rate is determined by TH1 value. If Timer 2 is used, the user should configure it in baud rate generator mode (RCLK or TCLK in T2CON is logic 1) and give 16-bit reloaded value in RCAP2H and RCAP2L.

Table 13–3 lists various commonly used baud rates and how they can be obtained from Timer 1. In this mode, Timer 1 as an auto-reload Timer operates in 12T mode and SMOD (PCON.7) is 0. Table 13–4 is for Timer 2 as the baud rate generator. Timer 2 operates in baud rate generator mode in 12T mode. In 6T mode, the baud rate generated from both Timer 1 and Timer 2 overflows will be doubled.

Table 13–3. Timer 1 Generated Commonly Used Baud Rates

TH1 reload value	Oscillator Frequency (MHz)				
	11.0592	14.7456	18.432	22.1184	36.864
Baud Rate					
57600				FFh	
38400		FFh			
19200		FEh		FDh	FBh

Bit	Name	Description
5	ET2	**Enable Timer 2 interrupt.** 0 = Disable all Timer 2 interrupts. 1 = Enable interrupt generated by TF2 (T2CON.7) or EXF2 (T2CON.6).
4	ES	**Enable serial port (UART) interrupt.** 0 = Disable all UART interrupts. 1 = Enable interrupt generated by TI (SCON.1) or RI (SCON.0).
3	ET1	**Enable Timer 1 interrupt.** 0 = Disable Timer 1 interrupt 1 = Enable interrupt generated by TF1 (TCON.7).
2	EX1	**Enable external interrupt 1.** 0 = Disable external interrupt 1. 1 = Enable interrupt generated by $\overline{INT1}$ pin (P3.3).
1	ET0	**Enable Timer 0 interrupt.** 0 = Disable Timer 0 interrupt 1 = Enable interrupt generated by TF0 (TCON.5).
0	EX0	**Enable external interrupt 0.** 0 = Disable external interrupt 0. 1 = Enable interrupt generated by $\overline{INT0}$ pin (P3.2).

EIE – Extensive Interrupt Enable

7	6	5	4	3	2	1	0
-	-	-	-	-	EBOD	EPDT	ESPI
-	-	-	-	-	r/w	r/w	r/w

Address: BDH reset value: 0000 0000b

Bit	Name	Description
7:3	-	**Reserved.**
2	EBOD	**Enable Brown-out detection interrupt.** 0 = Disable Brown-out detection interrupt. 1 = Enable interrupt generated by BOF (PMC.3).
1	EPDT	**Enable Power Down waking-up timer interrupt.** 0 = Disable Power Down waking-up timer interrupt 1 = Enable interrupt generated by PDTF (PDCON.5).
0	ESPI	**Enable SPI interrupt.** 0 = Disable SPI interrupt. 1 = Enable interrupt generated by SPIF (SPSR.7), SPIOVF (SPSR.5), or MODF (SPSR.4).

IP – Interrupt Priority (bit-addressable)[1]

7	6	5	4	3	2	1	0
-	-	PT2	PS	PT1	PX1	PT0	PX0
-	-	r/w	r/w	r/w	r/w	r/w	r/w

Address: B8H reset value: 0000 0000b

Bit	Name	Description
7:6	-	**Reserved.**
5	PT2	**Timer 2 interrupt priority low bit.**

hold the pin low till the interrupt is serviced. The IE0 and IE1 will not be cleared by the hardware on entering the service routine. In the level triggered mode, IE0 and IE1 follows the inverse value of $\overline{INT0}$ and $\overline{INT1}$ pins. If interrupt pins continue to be held low even after the service routine is completed, the processor will acknowledge another interrupt request from the same source. N78E517A (on PLCC-44, PQFP-44, TQFP-44, and LQFP-48 packages) possessed other two external interrupts $\overline{INT2}$ and $\overline{INT3}$. Their setting and operation are just the same as interrupt 0 and 1. All configuring bits locate in XICON. The individual interrupt flag corresponding to external interrupt 2 to 3 will also be automatically cleared via hardware once its own interrupt service routine is executed.

The Timer 0 and 1 Interrupts are generated by the TF0 and TF1 flags. These flags are set by the overflow in the Timer 0 and Timer 1 and automatically cleared by the hardware when the timer interrupt is serviced. TF2 or EXF2 flag generates the Timer 2 interrupt. These flags are set by overflow, capture, or reload events in the Timer 2 operation. The hardware will not clear these flags when a Timer 2 interrupt service routine executes. Software has to resolve the cause of the interrupt between TF2 and EXF2 and clear the appropriate flag.

The serial port can generate interrupts on reception or transmission. There are two interrupt sources from the serial port block, which are obtained by the RI and TI bits in the SCON. These bits are not automatically cleared by the hardware. The user has to clear these bits via software.

The Power Down waking-up timer can be used as a simple timer. The Power Down waking-up timer interrupt flag PDTF (PDCON.5) is set once an overflow occurs. If the interrupt is enabled by the enable bit EPDT (EIE.1), then an interrupt will occur.

Brown-out detection, if enabled, can cause Brown-out flag BOF (PMC.3) to be asserted if power voltage drop below Brown-out voltage level. The interrupt will occur if BORST (PMC.4) is 0 and EBOD (EIE.2) is 1.

SPI asserts interrupt flag SPIF (SPSR.7) on completion of data transfer with an external device. If SPI interrupt enable bit ESPI (EIE.0), a serial peripheral interrupt generates. SPIF flag is software clear. MODF (SPSR.4) and SPIOVF (SPSR.5) will also generate SPI interrupt. They share the same vector address with SPIF. When interrupt is generated, the user should tell which flag requires the interrupt.

All the bits that generate interrupts can be set or reset via hardware, and thereby software initiated interrupts can be generated. Each of the individual interrupts can be enabled or disabled by setting or clearing its controlling bit in the IE or EIE. IE also has a global enable bit EA (IE.7) which can be cleared to disable all the interrupts at once. It is set to enable all individually enabled interrupt.

Note that every interrupts, if enabled, is generated by a setting as a logic 1 of its interrupt flag no matter by hardware or software. The user should take care of each interrupt flag in its own interrupt service routine (ISR).

Source	Vector Address	Flag	Enable Bit	Natural Priority	Priority Control Bits	Power Down Waking up
SPI interrupt	0043H	SPIF (SPSR.7) + MODF (SPSR.4) + SPIOVF (SPSR.5)	ESPI (EIE.0)	9	PSPI (EIP.0), PSPIH (EIPH.0)	No
Power Down waking-up timer interrupt	004BH	PDTF (PDCON.5)	EPDT (EIE.1)	10	PPDT (EIP.1), PPDTH (EIPH.1)	Yes
Brown-out interrupt	0053H	BOF (PMC.3)	EBOD (EIE.2)	11	PBOD (EIP.2), PBODH (EIPH.2)	Yes

[1] While the external interrupt pin is set as edge triggered (ITx = 1), its own flag Iex will be automatically cleared if the interrupt service routine (ISR) is executed. While as level triggered (Itx = 0), Iex follows the inverse of respective pin state. It is not controlled via software.

[2] TF0 and TF1 will be automatically cleared if the interrupt service routine (ISR) is executed. But be aware that TF2 will not.

The interrupt flags are sampled every machine-cycle. In the same machine-cycle, the sampled interrupts are polled and their priority is resolved. If certain conditions are met then the hardware will execute an internally generated LCALL instruction which will vector the process to the appropriate interrupt vector address. The conditions for generating the LCALL are,

1. An interrupt of equal or higher priority is not currently being serviced.

2. The current polling cycle is the last machine-cycle of the instruction currently being executed.

3. The current instruction does not involve a write to any enable or priority setting bits and is not a RETI.

If any of these conditions are not met, then the LCALL will not be generated. The polling cycle is repeated every machine-cycle. If an interrupt flag is active in one cycle but not responded to for the above conditions are not met, if the flag is not still active when the blocking condition is removed, the denied interrupt will not be serviced. This means that the interrupt flag, which was once active but not serviced, is not remembered. Every polling cycle is new.

The processor responds to a valid interrupt by executing an LCALL instruction to the appropriate service routine. This action may or may not clear the flag, which caused the interrupt according to different interrupt source. The hardware LCALL behaves exactly like the software LCALL instruction. This instruction saves the Program Counter contents onto the Stack RAM but does not save the Program Status Word (PSW). The PC is reloaded with the vector address of that interrupt which caused the LCALL. Execution continues from the vectored address till an RETI instruction is executed. On execution of the RETI instruction the processor pops the Stack and loads the PC with the contents at the top of the stack. The user must take care that the status of the stack is restored to what it was after the hardware LCALL. If the execution is to return to the interrupted program, the processor does not notice anything if the stack contents are modified and will proceed with execution from the address put back into PC. Note that a simple RET instruction would perform exactly the same process as a RETI instruction, but it would not inform the Interrupt controller that the interrupt service routine is com-

20. CLOCK SYSTEM

N78E517A provides three options of the system clock source. It is configured by FOSC (CONFIG3.1),which switches the system clock from crystal/resonator/external clock from XTAL1 pin or on-chip RC oscillator. N78E517A embeds an on-chip RC oscillator of 22.1184MHz/11.0592MHz selected by CONFIG setting, factory trimmed to ± 1% at room temperature. If the external clock source is from the crystal, the frequency supports from 4MHz to 40MHz.

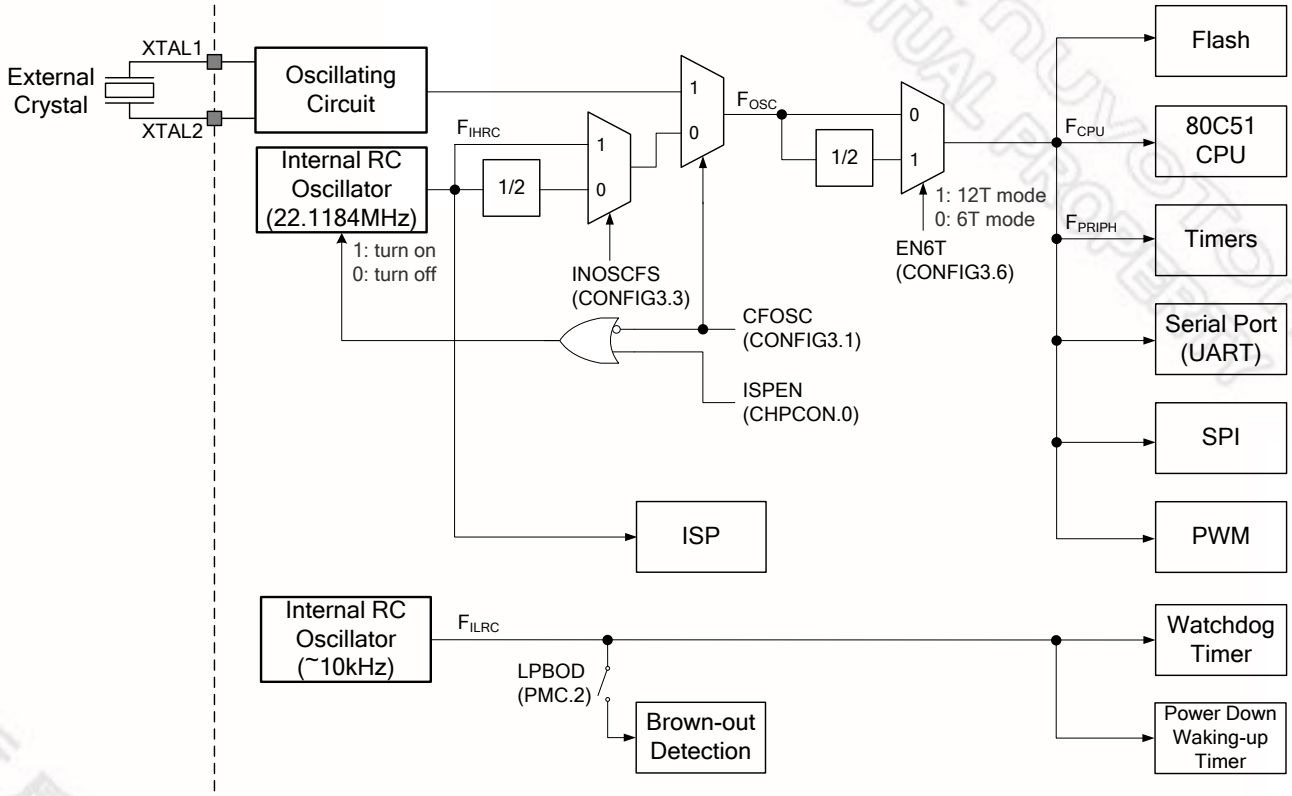


Figure 20–1. Clock System Block Diagram

20.1 12T/6T mode

The clock for the entire circuit and peripherals is normally divided by 2 before being used by the CPU core and peripherals. In 6T mode, this divider is bypassed. This facility provides the same performance when operating with a 24MHz oscillator in 12T mode as with a 12MHz oscillator in 6T mode, for example. The user may choose a divided-by-2 frequency oscillator in 6T mode to reach the same performance as in the original 12T mode. Therefore, it reduces EMI and power consumption if 6T mode is used.

CHPCON – Chip Control (TA protected)

7	6	5	4	3	2	1	0
SWRST	ISPF	LDUEN	XRAMEN	-	-	BS	ISPEN
w	r/w	r/w	r/w	-	-	r/w	r/w

Address: 9FH reset value: see Table 6–2. N78E517A SFR Description and Reset Values

Bit	Name	Description
7	SWRST	**Software reset.** To set this bit as a logic 1 will cause a software reset. It will automatically be cleared via hardware after reset in finished.

The software demo code are listed below.

```
MOV TA,#0Aah              ;TA protection.
MOV TA,#55h               ;
ANL CHPCON,#0FDh          ;BS = 0, reset to APROM.
MOV TA,#0Aah
MOV TA,#55h
ORL CHPCON,#80h           ;Software reset
```

22.6 Boot Select

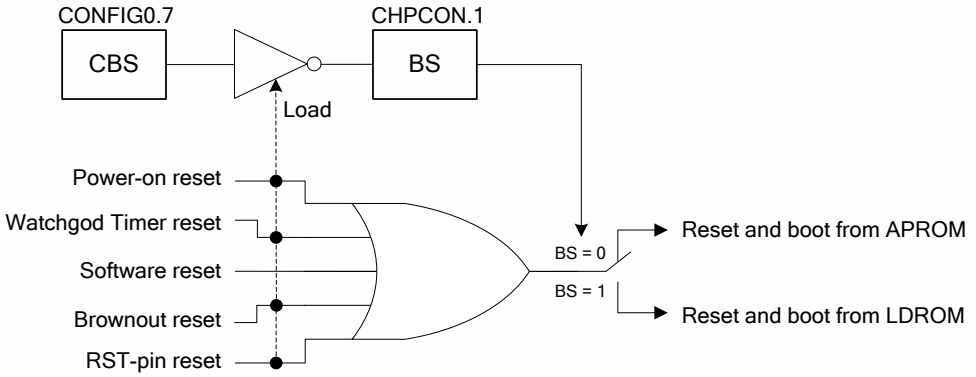


Figure 22–1. Boot Selecting Diagram

N78E517A provides users a flexible boot selection for variant application. The SFR bit BS in CHPCON.1 determines CPU booting from APROM or LDROM after any source of reset. If reset occurs and BS is 0, CPU will reboot from APPROM. Else, the CPU will reboot from LDROM.

Figures below shows supply and Idle mode current under 12T/6T with internal program memory mode.

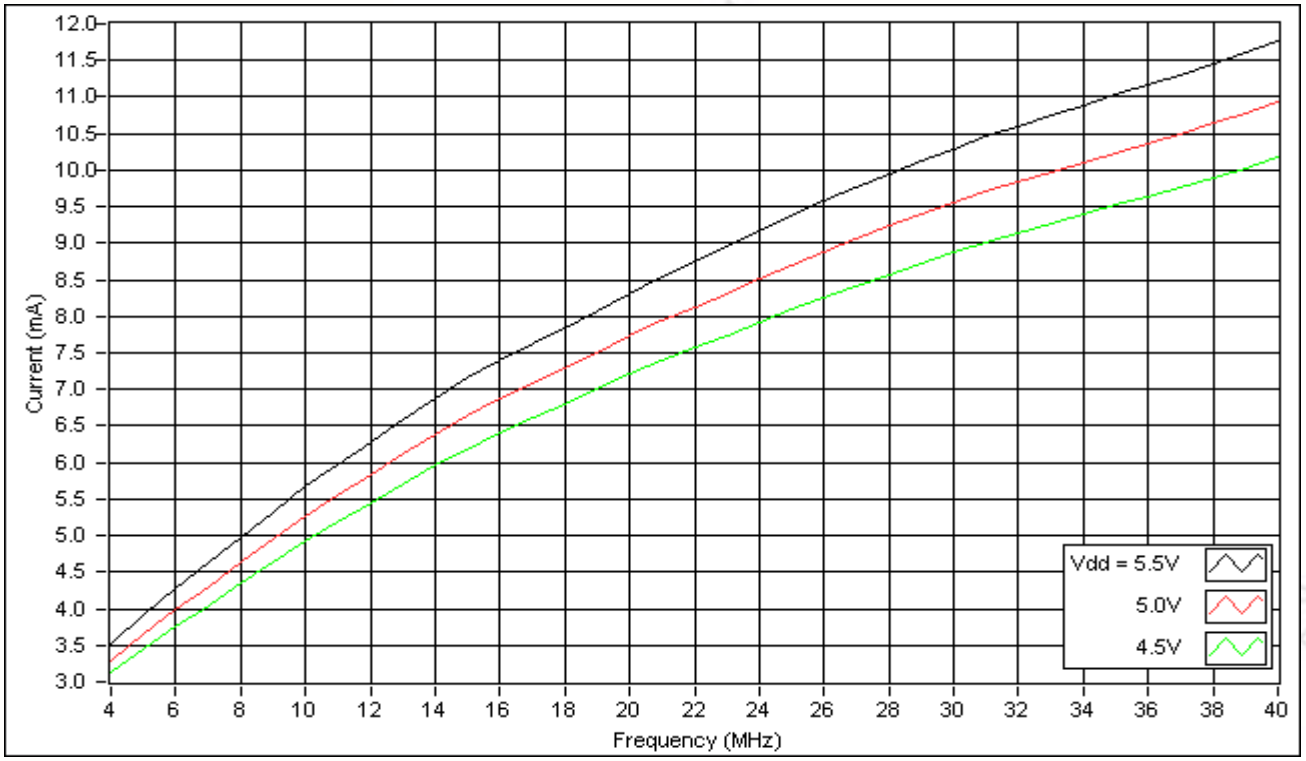
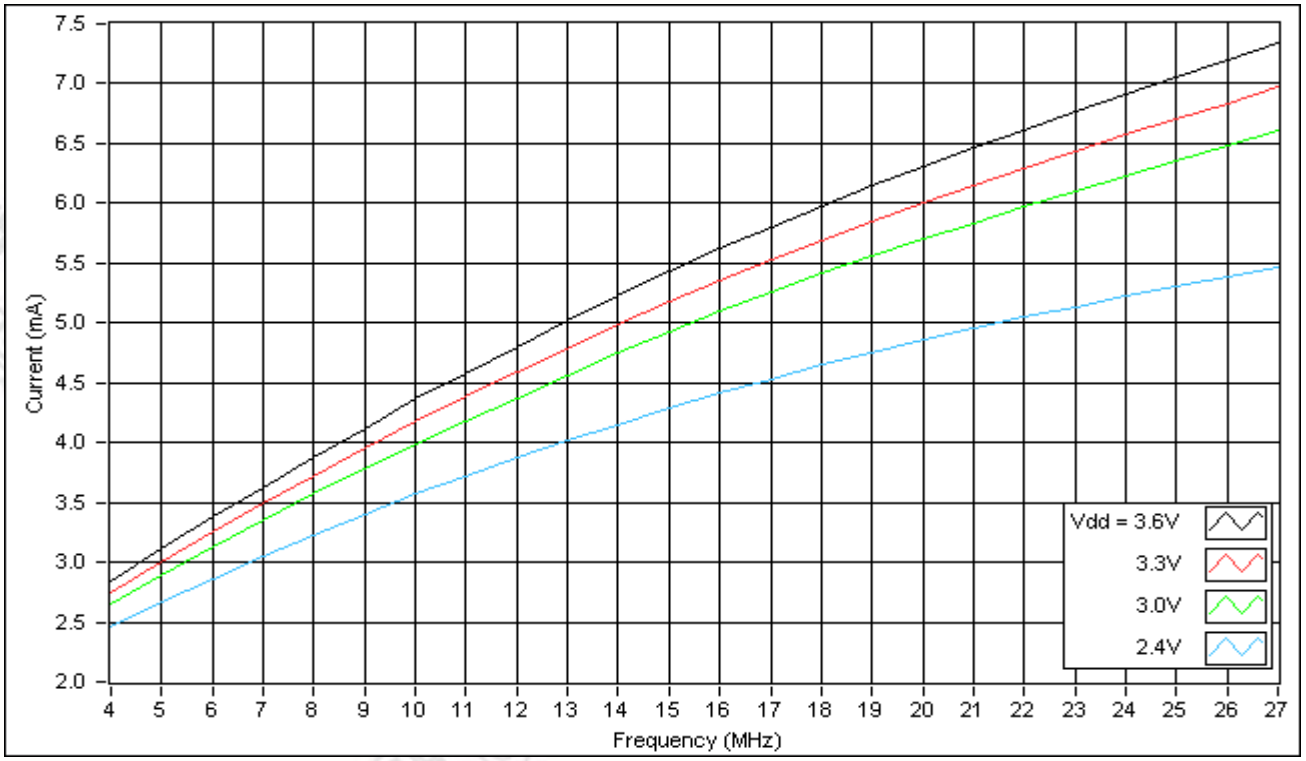


Figure 26–1. Supply Current Under 12T Mode, External Clock (1)



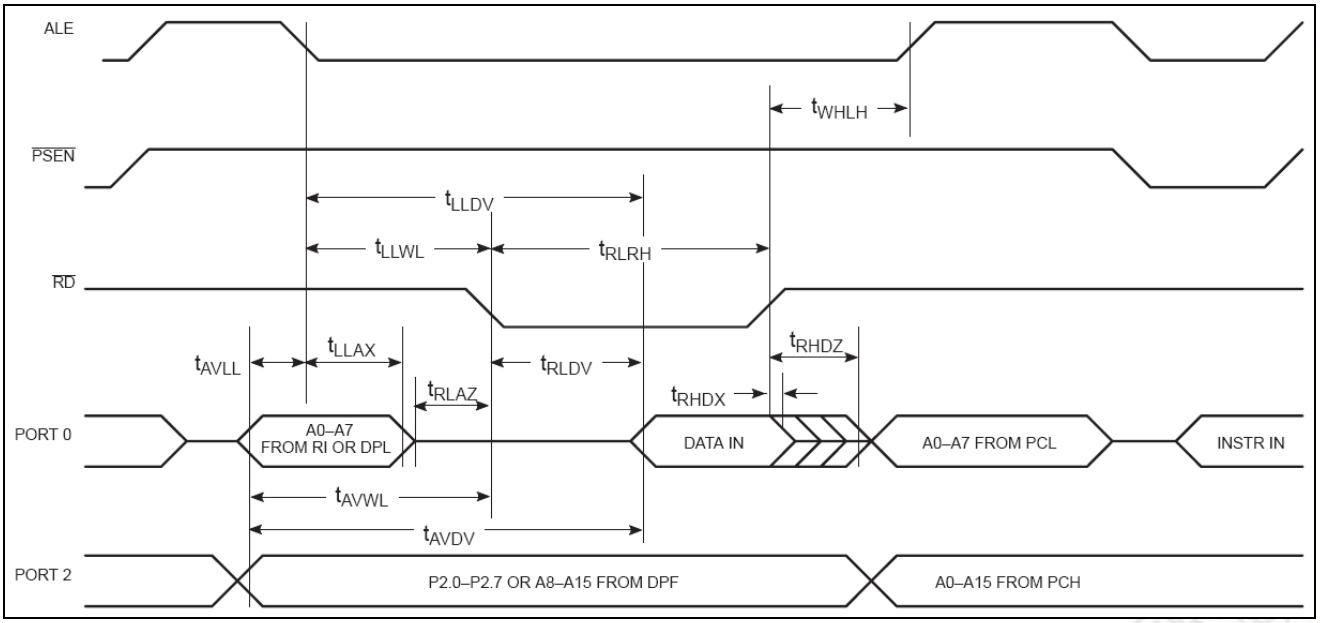


Figure 26–11. External Data Memory Read Cycle

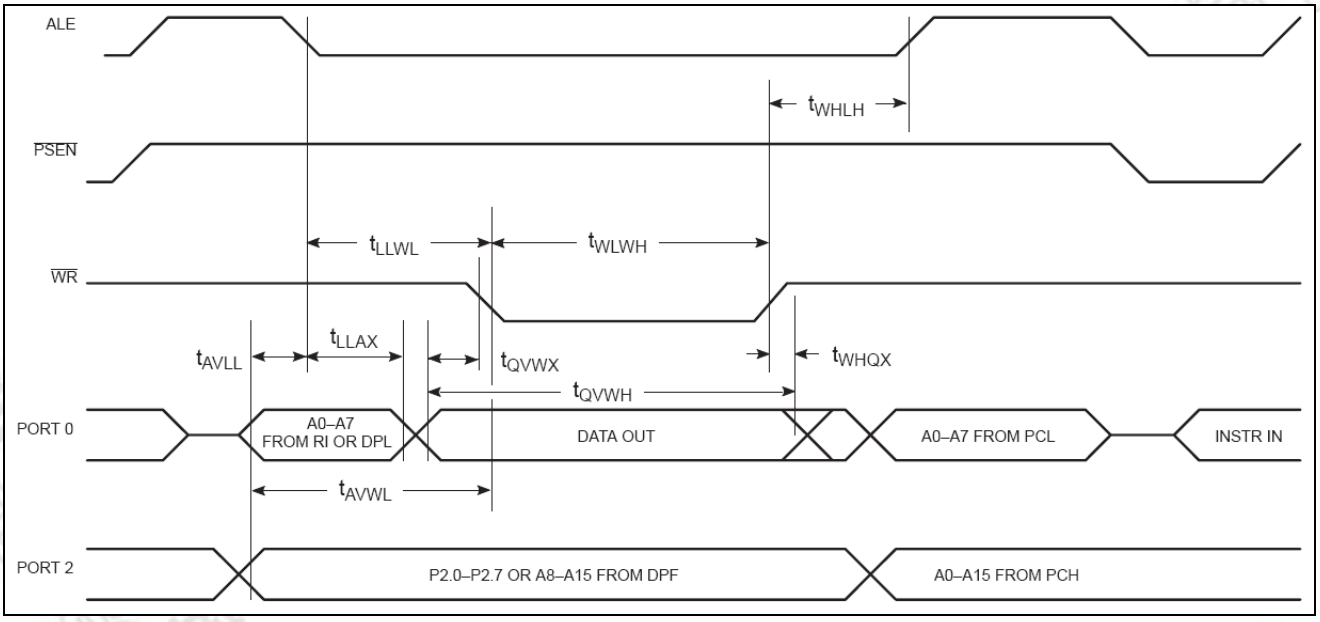


Figure 26–12. External Data Memory Write Cycle