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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, SmartCard, UART/USART, USB
Peripherals	I²S, LVD, POR, PWM, WDT
Number of I/O	65
Program Memory Size	304KB (304K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e1b34e0agf20000

Descriptor System Data Transfer Controller (DSTC) (64 Channels)

- The DSTC can transfer data at high-speed without going via the CPU. The DSTC adopts the Descriptor
- system and, following the specified contents of the Descriptor that has already been constructed on the
- memory, can access directly the memory / peripheral device and performs the data transfer operation.
- It supports the software activation, the hardware activation, and the chain activation functions

A/D Converter (Max: 24 Channels)

- 12-bit A/D Converter
  - Successive approximation type
  - Conversion time: 2.0 µs @ 2.7 V to 3.6 V
  - Priority conversion available (2 levels of priority)
  - Scan conversion mode
  - Built-in FIFO for conversion data storage (for scan conversion: 16 steps, for priority conversion: 4 steps)

Base Timer (Max: 8 Channels)

The operation mode of each channel can be selected from one of the following.

- 16-bit PWM timer
- 16-bit PPG timer
- 16/32-bit reload timer
- 16/32-bit PWC timer

General-Purpose I/O Port

This series can use its pin as a general-purpose I/O port when it is not used for an external bus or a peripheral function. All ports can be set to fast general-purpose I/O ports or slow general-purpose I/O ports. In addition, this series has a port relocate function that can set to which I/O port a peripheral function can be allocated.

- All ports are Fast GPIO which can be accessed by 1cycle
- Capable of controlling the pull-up of each pin
- Capable of reading pin level directly
- Port relocate function
- Up to 102 fast general-purpose I/O ports @120-pin package
- Certain ports are 5 V tolerant.
  See 4. List of Pin Functions and 5. I/O Circuit Type for the corresponding pins.

Dual Timer (32-/16-bit Down Counter)

The Dual Timer consists of two programmable 32-/16-bit down counters. The operation mode of each timer channel can be selected from one of the following.

- Free-running mode
- Periodic mode (= Reload mode)
- One-shot mode

Multi-Function Timer

The Multi-function Timer consists of the following blocks.

- 16-bit free-run timer × 3 channels
- Input capture × 4 channels
- Output compare × 6 channels
- ADC start compare × 6 channel
- Waveform generator × 3 channels
- 16-bit PPG timer × 3 channels

  IGBT mode is contained.

The following function can be used to achieve the motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- ADC start function
- DTIF (motor emergency stop) interrupt function

Real-Time Clock (RTC with Vbat)

The Real-time Clock counts year/month/day/hour/minute/second/day of the week from year 01 to year 99.

- The RTC can generate an interrupt at a specific time (year/month/day/hour/minute/second/day of the week) and can also generate an interrupt in a specific year, in a specific month, on a specific day, at a specific hour or at a specific minute.
- It has a timer interrupt function generating an interrupt upon a specific time or at specific intervals.
- It can keep counting while rewriting the time.
- It can count leap years automatically.

Watch Counter

The Watch Counter wakes up the microcontroller from the low power consumption mode. The clock source can be selected from the main clock, the sub clock, the built-in high-speed CR clock or the built-in low-speed CR clock.

Interval timer: up to 64 s (sub clock: 32.768 kHz)

External Interrupt Controller Unit

- Up to 24 external interrupt input pins
- Non-maskable interrupt (NMI) input pin: 1

Watchdog Timer (2 Channels)

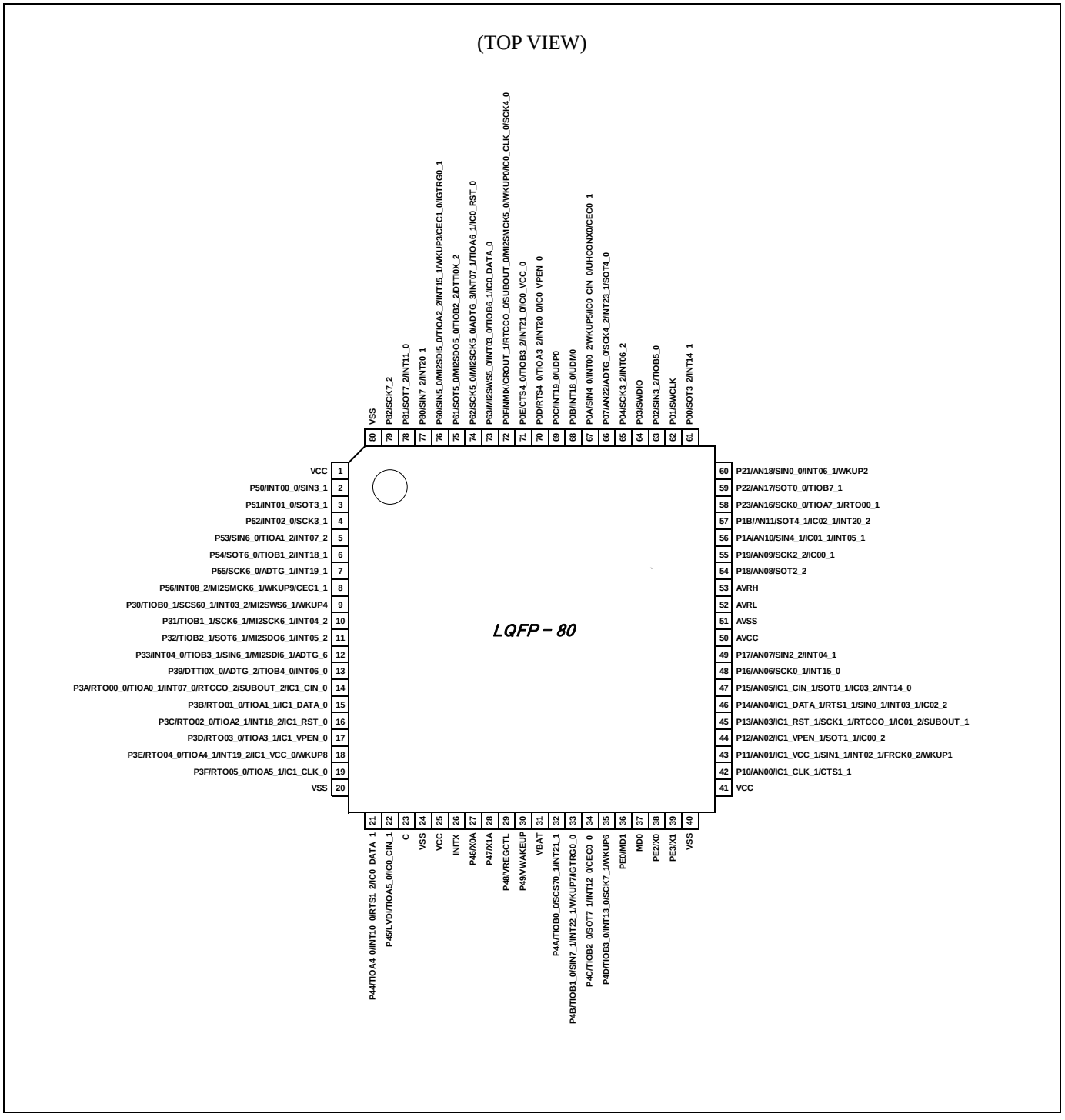
The watchdog timer generates an interrupt or a reset when the counter reaches a time-out value.

This series consists of two different watchdogs, hardware watchdog and software watchdog.

The hardware watchdog timer is clocked by the built-in low-speed CR oscillator. Therefore, the hardware watchdog is

3. Pin Assignment

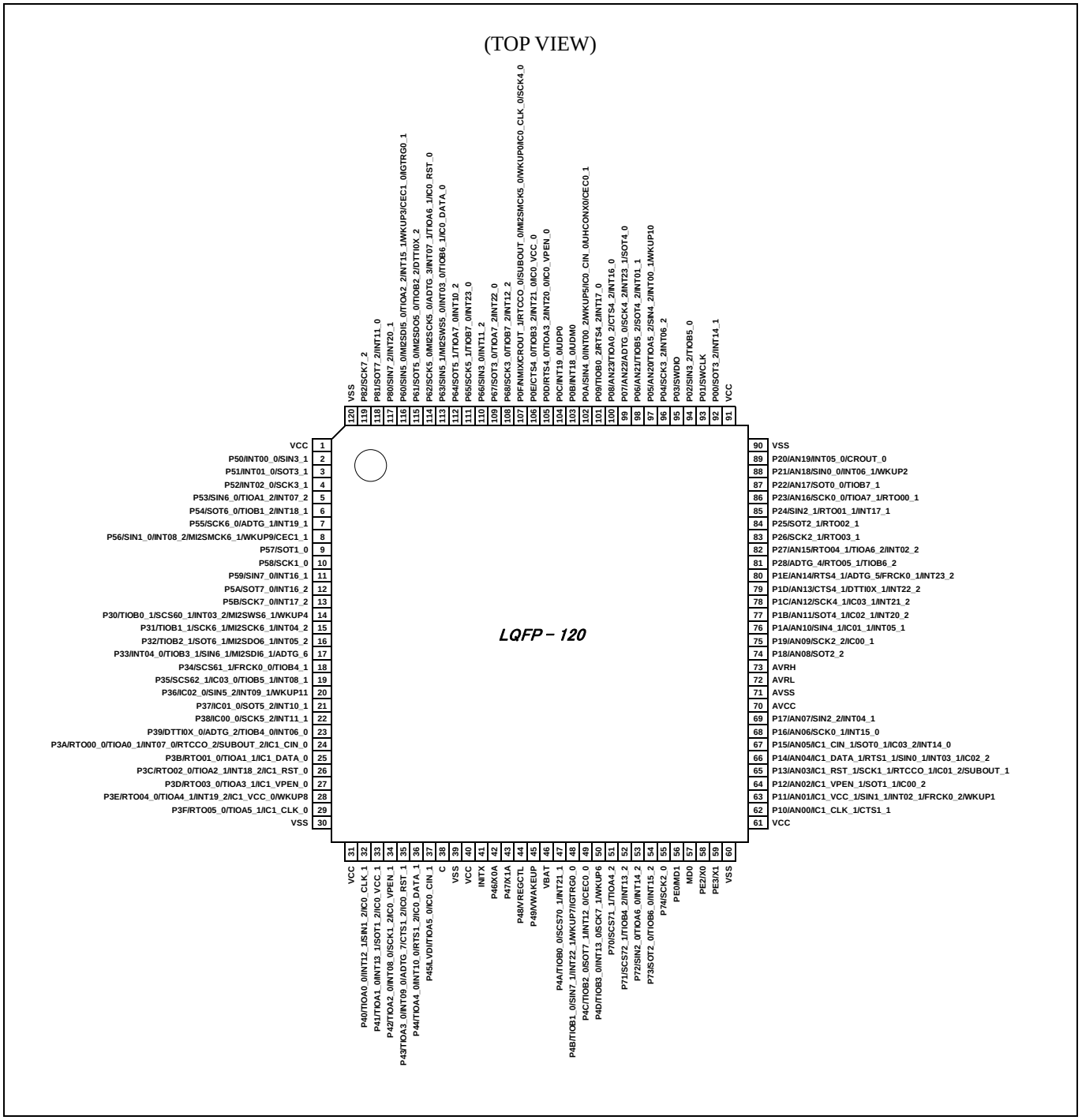
FPT-80P-M21



Note:

- *The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.*

FPT-120P-M21



Note:

- *The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.*

Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
13	-	-	P5B SCK7_0 INT17_2	F	J
14	9	9	P30 TIOB0_1 SCS60_1 MI2SWS6_1 INT03_2 WKUP4	I	N
15	10	10	P31 TIOB1_1 SCK6_1 MI2SCK6_1 INT04_2	I	J
16	11	11	P32 TIOB2_1 SOT6_1 MI2SDO6_1 INT05_2	I	J
17	12	12	P33 TIOB3_1 SIN6_1 MI2SDI6_1 INT04_0 ADTG_6	I	J
18	13	-	P34 SCS61_1 FRCK0_0 TIOB4_1	I	I
19	14	-	P35 SCS62_1 IC03_0 TIOB5_1 INT08_1	I	J
20	15	-	P36 IC02_0 SIN5_2 INT09_1 WKUP11	I	N
21	16	-	P37 IC01_0 SOT5_2 INT10_1	I	J
22	17	-	P38 IC00_0 SCK5_2 INT11_1	F	J

Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
34	29	-	P42 TIOA2_0 SCK1_2 IC0_VPEN_1 INT08_0	F	J
35	30	-	P43 TIOA3_0 CTS1_2 ADTG_7 IC0_RST_1 INT09_0	F	J
36	31	21	P44 TIOA4_0 IC0_DATA_1 INT10_0 RTS1_2	I	J
37	32	22	P45 TIOA5_0 IC0_CIN_1 LVDI	I	I
38	33	23	C	-	-
39	34	24	VSS	-	-
40	35	25	VCC	-	-
41	36	26	INITX	B	C
42	37	27	P46 X0A	D	E
43	38	28	P47 X1A	E	F
44	39	29	P48 VREGCTL	I	I
45	40	30	P49 VWAKEUP	I	I
46	41	31	VBAT	-	-
47	42	32	P4A TIOB0_0 SCS70_1 INT21_1	I	J
48	43	33	P4B TIOB1_0 SIN7_1 INT22_1 WKUP7 IGTRG0_0	I	N
49	44	34	P4C TIOB2_0 SOT7_1 CEC0_0 INT12_0	I	R
50	45	35	P4D TIOB3_0 SCK7_1 INT13_0 WKUP6	I	N

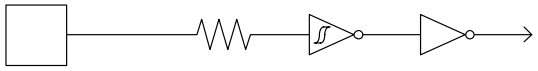
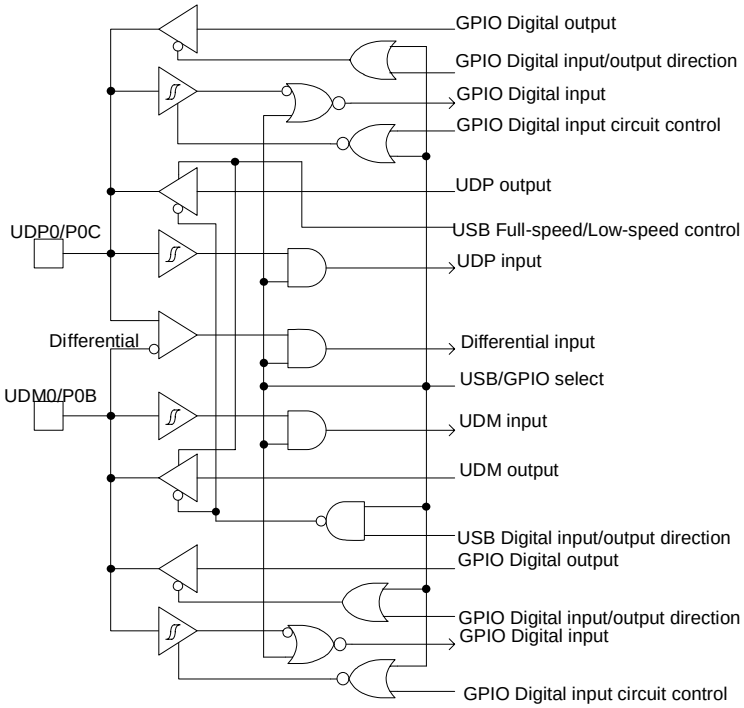
Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
112	-	-	P64	F	J
			SOT5_1		
			TIOA7_0		
			INT10_2		
113	93	73	P63	I	J
			MI2SWS5_0		
			INT03_0		
			TIOB6_1		
			IC0_DATA_0		
	-	-	SIN5_1		
114	94	74	P62	I	J
			SCK5_0		
			MI2SCK5_0		
			ADTG_3		
			INT07_1		
			TIOA6_1		
			IC0_RST_0		
115	95	75	P61	I	I
			SOT5_0		
			MI2SDO5_0		
			TIOB2_2		
			DTTI0X_2		
116	96	76	P60	I	O
			SIN5_0		
			MI2SDI5_0		
			TIOA2_2		
			CEC1_0		
			INT15_1		
			WKUP3		
			IGTRG0_1		
117	97	77	P80	I	J
			SIN7_2		
			INT20_1		
			C0		
118	98	78	P81	I	J
			SOT7_2		
			INT11_0		
			C1		
119	99	79	P82	I	I
			SCK7_2		
120	100	80	VSS	-	-

*: 5 V tolerant I/O

List of Pin Functions

The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
ADC	ADTG_0	A/D converter external trigger input pin	99	84	66
	ADTG_1		7	7	7
	ADTG_2		23	18	13
	ADTG_3		114	94	74
	ADTG_4		81	-	-
	ADTG_5		80	70	-
	ADTG_6		17	12	12
	ADTG_7		35	30	-
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	62	52	42
	AN01		63	53	43
	AN02		64	54	44
	AN03		65	55	45
	AN04		66	56	46
	AN05		67	57	47
	AN06		68	58	48
	AN07		69	59	49
	AN08		74	64	54
	AN09		75	65	55
	AN10		76	66	56
	AN11		77	67	57
	AN12		78	68	-
	AN13		79	69	-
	AN14		80	70	-
	AN15		82	-	-
	AN16		86	71	58
	AN17		87	72	59
	AN18		88	73	60
	AN19		89	74	-
	AN20		97	82	-
	AN21		98	83	-
	AN22		99	84	66
	AN23		100	85	-
Base Timer 0	TIOA0_0	Base timer ch.0 TIOA pin	32	27	-
	TIOA0_1		24	19	14
	TIOA0_2		100	85	-
	TIOB0_0	Base timer ch.0 TIOB pin	47	42	32
	TIOB0_1		14	9	9
	TIOB0_2		101	86	-

Type	Circuit	Remarks
J		・CMOS level hysteresis input
K		It is possible to select the USB I/O / GPIO function. When the USB I/O is selected. ・Full-speed, Low-speed control When the GPIO is selected. ・CMOS level output ・CMOS level hysteresis input ・With standby mode control

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Spansion recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Spansion ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

(1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product.
Store products in locations where temperature changes are slight.

(2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5 ˚C and 30 ˚C.
When you open Dry Package that recommends humidity 40% to 70% relative humidity.

(3) When necessary, Spansion packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.

(4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Spansion recommended conditions for baking.

Condition: 125°C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

(1) Maintain relative humidity in the working environment between 40% and 70%.
Use of an apparatus for ion generation may be needed to remove electricity.

(2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.

(3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.

(4) Ground all fixtures and instruments, or protect with anti-static measures.

(5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

Notes on Power-on

Turn power on/off in the following order or at the same time.

Turning on : VBAT → VCC
VCC → AVCC → AVRH
Turning off : VCC → VBAT
AVRH → AVCC → VCC

Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.
Consider the case of receiving wrong data due to noise; perform error detection such as by applying a checksum of data at the end.
If an error is detected, retransmit the data.

Differences in Features Among the Products with Different Memory Sizes and Between Flash Memory Products and MASK Products

The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash memory products and MASK products are different because chip layout and memory structures are different.

If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

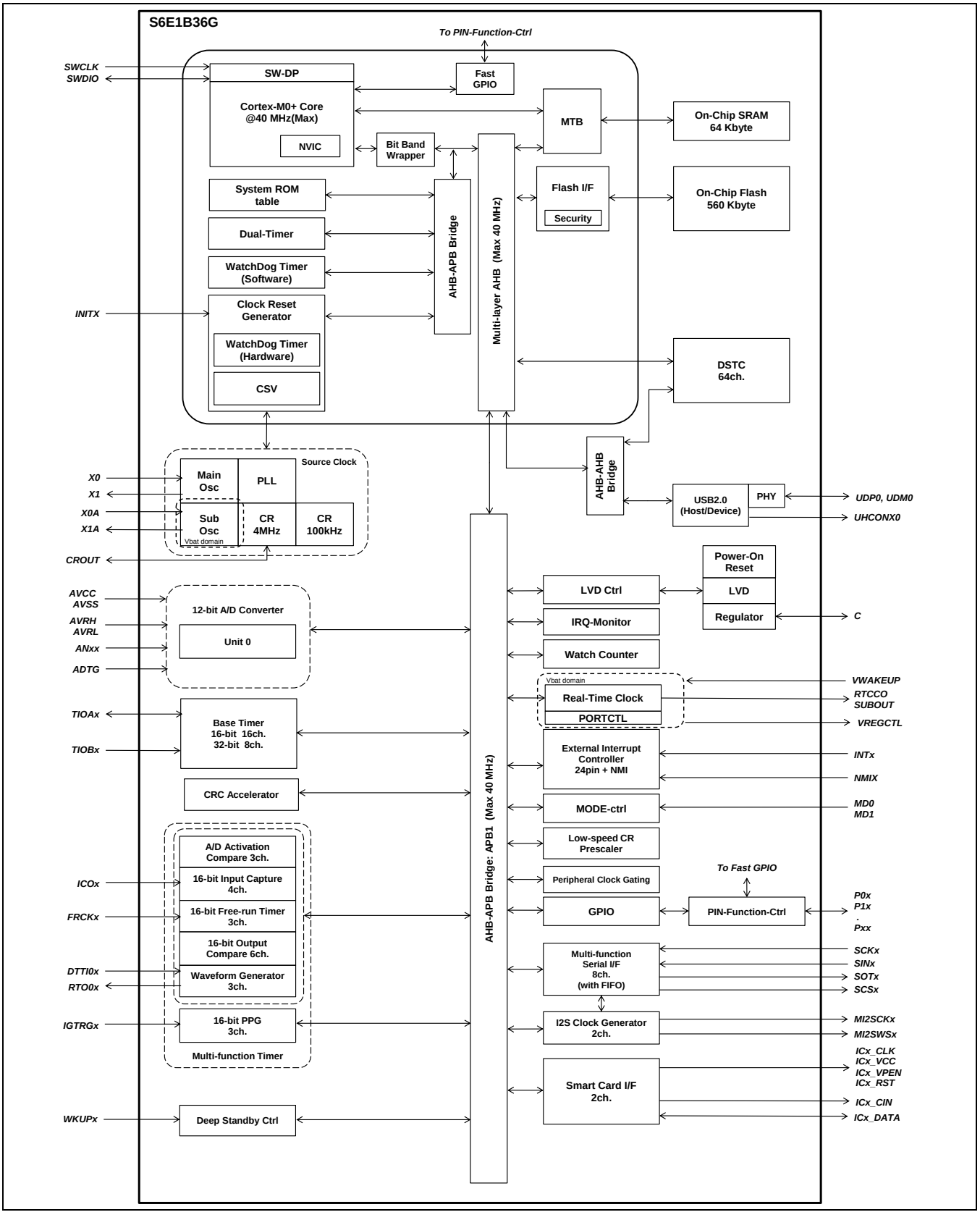
Pull-Up Function of 5 V Tolerant I/O

Please do not input the signal more than VCC voltage at the time of Pull-Up function use of 5 V tolerant I/O.

Handling when Using Debug Pins

When debug pins (SWDIO/SWCLK) are set to GPIO or other peripheral functions, set them as output only; do not set them as input.

8. Block Diagram



11. Electrical Characteristics

11.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1, *2	V_{CC}	V_{SS} - 0.5	V_{SS} + 4.6	V	
Analog power supply voltage*1, *3	AV_{CC}	V_{SS} - 0.5	V_{SS} + 4.6	V	
Analog reference voltage*1, *3	AVRH	V_{SS} - 0.5	V_{SS} + 4.6	V	
Input voltage*1	V_I	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 4.6 V)	V	
		V_{SS} - 0.5	V_{SS} + 6.5	V	5 V tolerant
Analog pin input voltage*1	V_{IA}	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 4.6 V)	V	
Output voltage*1	V_O	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 4.6 V)	V	
L level maximum output current*4	I_{OL}	-	10	mA	
			39	mA	P0B / P0C
L level average output current*5	I_{OLAV}	-	4	mA	
L level total maximum output current	$\sum I_{OL}$	-	100	mA	
L level total average output current*6	$\sum I_{OLAV}$	-	50	mA	
H level maximum output current*4	I_{OH}	-	- 10	mA	
			- 39	mA	P0B / P0C
H level average output current*5	I_{OHAV}	-	- 4	mA	
H level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
H level total average output current*6	$\sum I_{OHAV}$	-	- 50	mA	
Power consumption	P_D	-	250	mW	
Storage temperature	T_{STG}	- 55	+ 150	°C	

*1: These parameters are based on the condition that V_{SS}=AV_{SS}=0 V.

*2: V_{CC} must not drop below V_{SS} - 0.5 V.

*3: Ensure that the voltage does not to exceed V_{CC} + 0.5 V at power-on.

*4: The maximum output current is the peak value for a single pin.

*5: The average output is the average current for a single pin over a period of 100 ms.

*6: The total average output current is the average current for all pins over a period of 100 ms.

*7: When P0C/UDP0 and P0B/UDM0 pins are used as GPIO (P0C, P0B).

*8: When P0C/UDP0 and P0B/UDM0 pins are used as USB (UDP0, UDM0).

<WARNING>

- *Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.*

11.2 Recommended Operating Conditions

(V_{SS}=AV_{SS}=0.0 V)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Power supply voltage	V_{CC}	-	1.65 *3	3.6	V	
			3.0	3.6	V	*1
Sub Oscillation frequency	Fin	-	-	-	kHz	Typical is 32.768 kHz
Analog power supply voltage	AV_{CC}	-	1.65	3.6	V	AV_{CC}=V_{CC}
Analog reference voltage	AVRH	-	2.7	AV_{CC}	V	AV_{CC} ≥ 2.7 V
			AV_{CC}	AV_{CC}	V	AV_{CC} < 2.7 V
	AVRL	-	AV_{SS}	AV_{SS}	V	
Smoothing capacitor	C_S	-	1	10	µF	For regulator*2
Operating temperature	T_A	-	- 40	+ 105	°C	

*1: When P0C/UDP0 and P0B/UDM0 pins are used as USB (UDP0, UDM0).

*2: See "C Pin" in "7. Handling Devices" for the connection of the smoothing capacitor.

*3: In between less than the minimum power supply voltage reset / interrupt detection voltage or more, instruction execution and low voltage detection function by built-in High-speed CR (including Main PLL is used) or built-in Low-speed CR is possible to operate only.

<WARNING>

1. *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.*
2. *Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.*
3. *No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet.*
4. *Users considering application outside the listed conditions are advised to contact their representatives beforehand.*

Parameter	Symbol (Pin Name)	Conditions			Value		Unit	Remarks
					Typ	Max		
Power supply current	I_{CCHD} (VCC)	Deep standby Stop mode	RAM off	T_A=25°C V_{CC}=3.3 V	0.75	TBD	µA	*1
				T_A=25°C V_{CC}=1.65 V	0.7	TBD	µA	*1
				T_A=105°C V_{CC}=3.6 V	-	TBD	µA	*1
			RAM on	T_A=25°C V_{CC}=3.3 V	1.1	TBD	µA	*1
				T_A=25°C V_{CC}=1.65 V	1.0	TBD	µA	*1
				T_A=105°C V_{CC}=3.6 V	-	TBD	µA	*1
	I_{CCRD} (VCC)	Deep standby RTC mode	RAM off	T_A=25°C V_{CC}=3.3 V	1.7	TBD	µA	*1
				T_A=25°C V_{CC}=1.65 V	1.6	TBD	µA	*1
				T_A=105°C V_{CC}=3.6 V	-	TBD	µA	*1
			RAM on	T_A=25°C V_{CC}=3.3 V	1.9	TBD	µA	*1
				T_A=25°C V_{CC}=1.65 V	1.7	TBD	µA	*1
				T_A=105°C V_{CC}=3.6 V	-	TBD	µA	*1

*1: All ports are fixed. LVD off.

Parameter	Symbol (Pin Name)	Conditions		Value		Unit	Remarks
				Typ	Max		
Power supply current	I_{CCVBAT} (VBAT)	RTC operation	T_A=25°C V_{CC}=3.0V 32 kHz Crystal oscillation	0.9	TBD	µA	*1
			T_A=25°C V_{CC}=1.65 V 32 kHz Crystal oscillation	0.8	TBD	µA	*1
			T_A=105°C V_{CC}=3.6V 32 kHz Crystal oscillation	-	TBD	µA	*1
		RTC stop	T_A=25°C V_{CC}=3.0V	0.05	TBD	µA	*1
			T_A=25°C V_{CC}=1.65 V	0.02	TBD	µA	*1
			T_A=105°C V_{CC}=3.6V	-	TBD	µA	*1

*1: All ports are fixed.

11.4 AC Characteristics

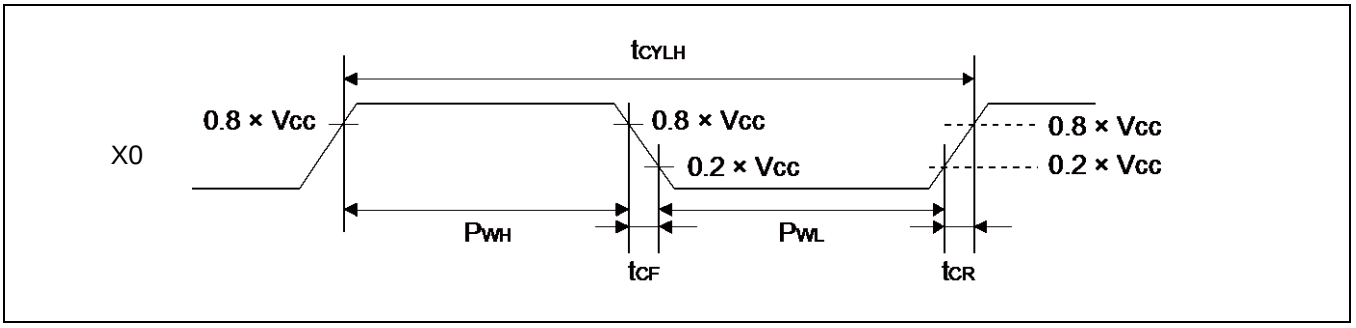
11.4.1 Main Clock Input Characteristics

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

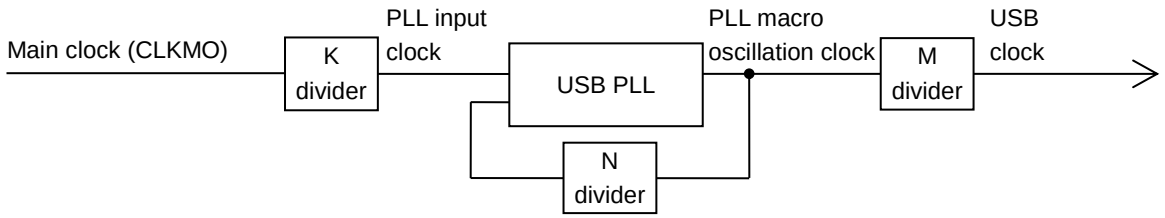
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f_{CH}	X0, X1	V_{CC} ≥ 2.7 V	4	48	MHz	When the crystal oscillator is connected
			V_{CC} < 2.7 V	4	20		
			-	4	48	MHz	When the external clock is used
Input clock cycle	t_{CYLH}		-	20.83	250	ns	When the external clock is used
Input clock pulse width	-		P_{WH}/t_{CYLH}, P_{WL}/t_{CYLH}	45	55	%	When the external clock is used
Input clock rising time and falling time	t_{CF}, t_{CR}		-	-	5	ns	When the external clock is used
Internal operating clock*1 frequency	f_{CM}	-	-	-	40.8	MHz	Master clock
	f_{CC}	-	-	-	40.8	MHz	Base clock (HCLK/FCLK)
	f_{CP0}	-	-	-	40.8	MHz	APB0 bus clock*2
	f_{CP1}	-	-	-	40.8	MHz	APB1 bus clock*2
Internal operating clock*1 cycle time	t_{CYCC}	-	-	24.5	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	24.5	-	ns	APB0 bus clock*2
	t_{CYCP1}	-	-	24.5	-	ns	APB1 bus clock*2

*1: For details of each internal operating clock, refer to "Chapter: Clock" in "FM0+ Family Peripheral Manual".

*2: For details of the APB bus to which a peripheral is connected, see "8. Block Diagram".



USB PLL connection



11.4.6 Reset Input Characteristics

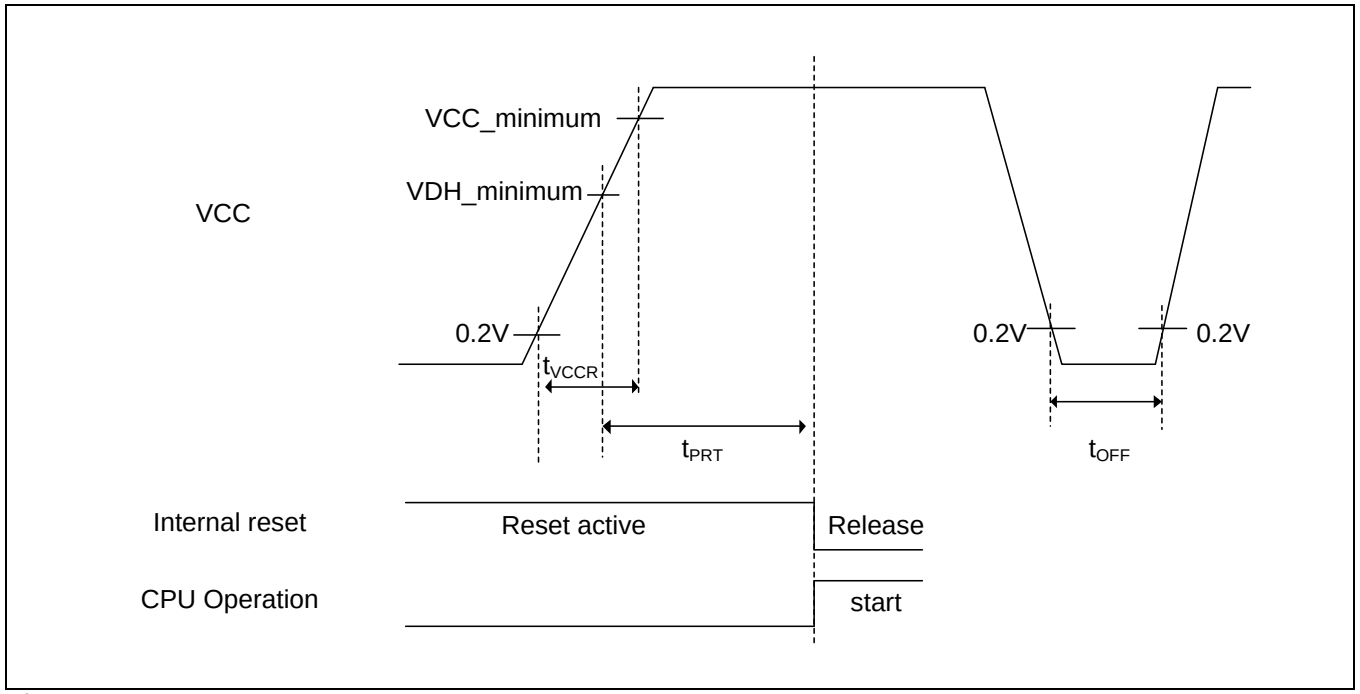
(V_{CC} =AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{INITX}	INITX	-	500	-	ns	

11.4.7 Power-on Reset Timing

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_{VCCR}	VCC	0	-	ms	
Power supply shut down time	t_{OFF}		1	-	ms	
Time until releasing Power-on reset	t_{PRT}		0.43	3.4	ms	



Glossary

- VCC_minimum : Minimum V_{CC} of recommended operating conditions.
- VDH_minimum : Minimum detection voltage of Low-Voltage detection reset.
  See "11.7 Low-Voltage Detection Characteristics".

11.4.10 External Input Timing

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

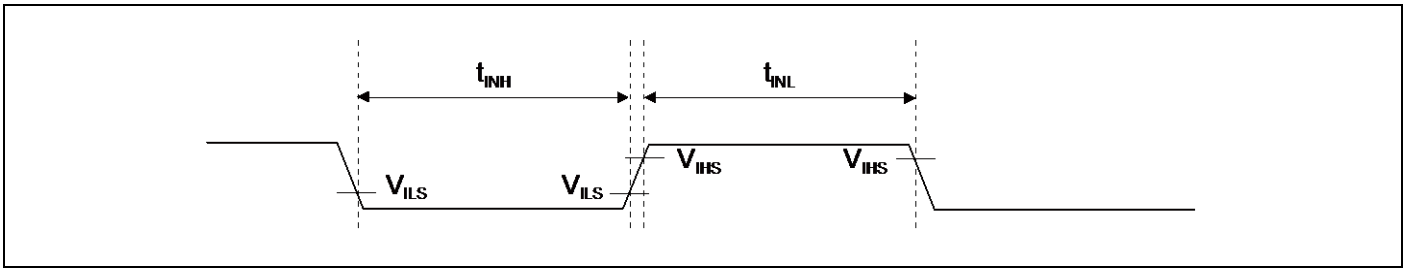
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH}, t_{INL}	ADTGx	-	2 t_{CYCP}*1	-	ns	A/D converter trigger input
		FRCKx					Free-run timer input clock
		ICxx					Input capture
		DTTIxX	-	2 t_{CYCP}*1	-	ns	Wave form generator
		INTxx, NMIX	*2	2 t_{CYCP} +100*1	-	ns	External interrupt, NMI
			*3	500	-	ns	
		WKUPx	*4	500	-	ns	Deep standby wake up

*1: t_{CYCP} represents the APB bus clock cycle time.
For the number of the APB bus to which the Multi-function Timer is connected and that of the APB bus to which the External Interrupt Controller is connected, see "8. Block Diagram".

*2: In Run mode and Sleep mode

*3: In Timer mode and RTC mode and Stop mode

*4: In Deep Standby RTC mode and Deep Standby Stop mode



11.4.11 I²C Timing

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

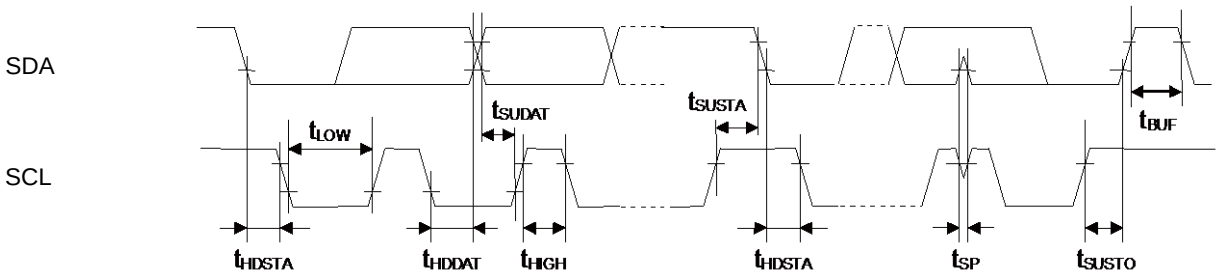
Parameter	Symbol	Conditions	Standard-Mode		Fast-Mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	C_L=30 pF, R=(V_P/I_{OL})*1	0	100	0	400	kHz	
(Repeated) Start condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs	
SCL clock L width	t_{LOW}		4.7	-	1.3	-	µs	
SCL clock H width	t_{HIGH}		4.0	-	0.6	-	µs	
(Repeated) Start setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns	
Stop condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs	
Bus free time between Stop condition and Start condition	t_{BUF}		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	-	2 t_{CYCP}*4	-	2 t_{CYCP}*4	-	ns	

*1: R represents the pull-up resistance of the SCL and SDA lines, and C_L the load capacitance of the SCL and SDA lines. V_P represents the power supply voltage of the pull-up resistance, and I_{OL} the V_{OL} guaranteed current.

*2: The maximum t_{HDDAT} must satisfy at least the condition that the period during which the device is holding the SCL signal at L (t_{LOW}) does not extend.

*3: A Fast-mode I²C bus device can be used in a Standard-mode I²C bus system, provided that the condition of t_{SUDAT} ≥ 250 ns is fulfilled.

*4: t_{CYCP} represents the APB bus clock cycle time.
For the number of the APB bus to which the I²C is connected, see "8. Block Diagram".
To use Standard-mode, set the APB bus clock at 2 MHz or more.
To use Fast-mode, set the APB bus clock at 8 MHz or more.



12. Ordering Information

Part Number	On-Chip Flash Memory	On-Chip SRAM	Package	Packing
S6E1B34E0AGV20000	304	32	Plastic • LQFP (0.50 mm pitch), 80 pins (FPT-80P-M21)	Tray
S6E1B36E0AGV20000	560	64		
S6E1B34F0AGV20000	304	32	Plastic • LQFP (0.50 mm pitch), 100 pins (FPT-100P-M20)	Tray
S6E1B36F0AGV20000	560	64		
S6E1B34G0AGV20000	304	32	Plastic • LQFP (0.50 mm pitch), 120 pins (FPT-120P-M21)	Tray
S6E1B36G0AGV20000	560	64		