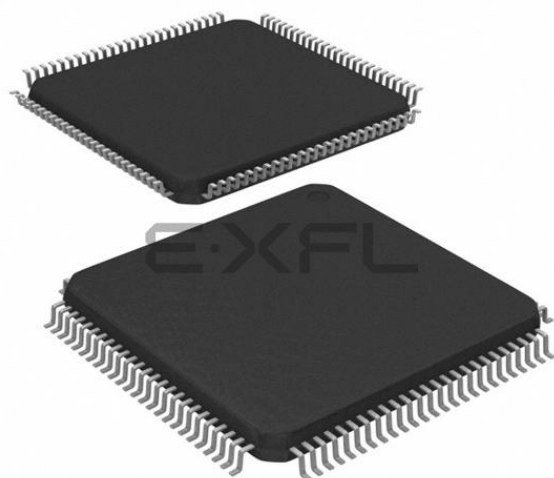




Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

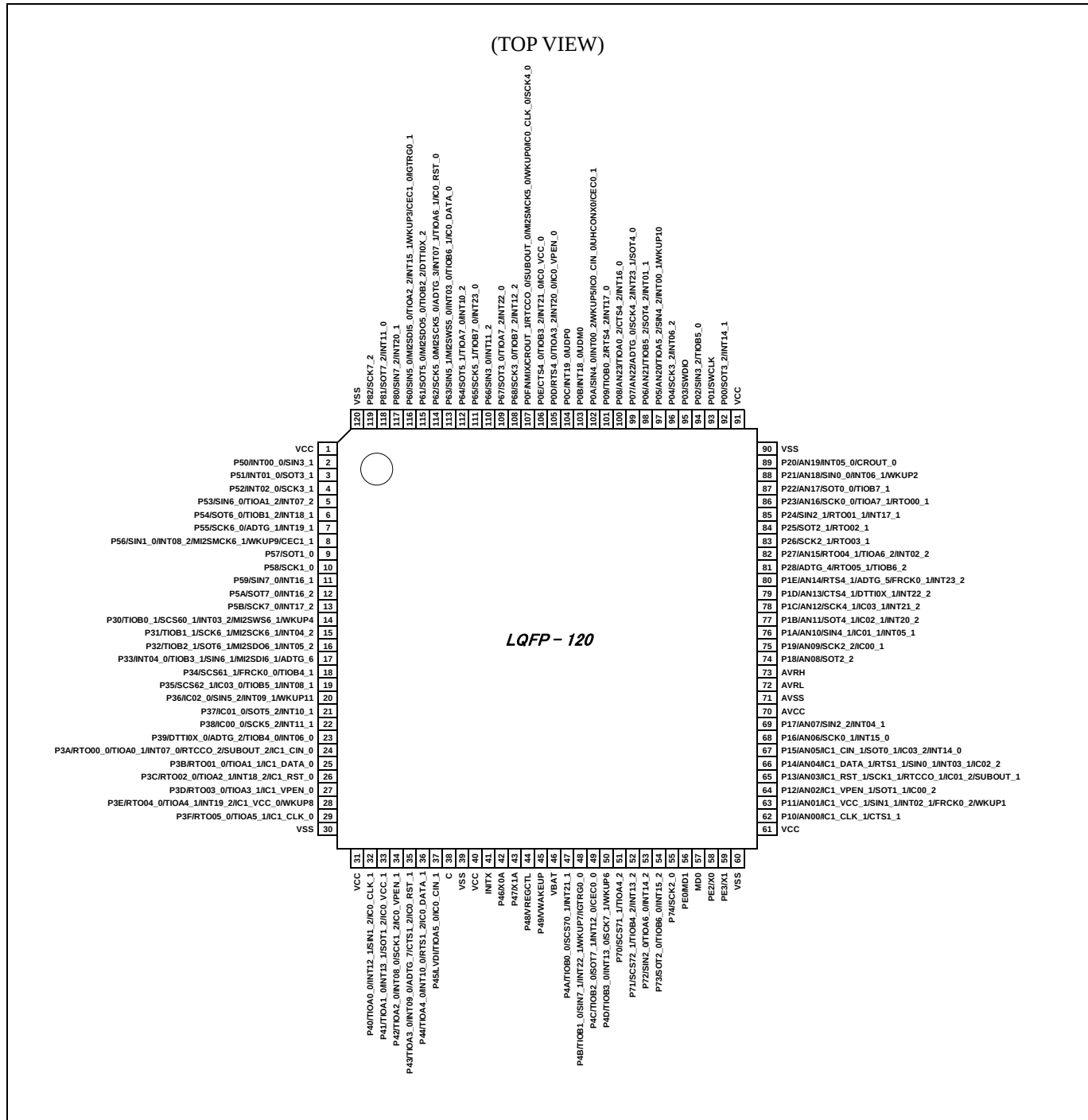
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, SmartCard, UART/USART, USB
Peripherals	I²S, LVD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	304KB (304K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 23x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e1b34f0agv20000



12. Ordering Information	110
13. Package Dimensions	111
Document History.....	114
Sales, Solutions, and Legal Information.....	115



FPT-120P-M21



Note:

- The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.

Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
13	-	-	P5B	F	J
			SCK7_0		
			INT17_2		
14	9	9	P30	I	N
			TIOB0_1		
			SCS60_1		
			MI2SWS6_1		
			INT03_2		
			WKUP4		
15	10	10	P31	I	J
			TIOB1_1		
			SCK6_1		
			MI2SCK6_1		
			INT04_2		
16	11	11	P32	I	J
			TIOB2_1		
			SOT6_1		
			MI2SDO6_1		
			INT05_2		
17	12	12	P33	I	J
			TIOB3_1		
			SIN6_1		
			MI2SDI6_1		
			INT04_0		
			ADTG_6		
18	13	-	P34	I	I
			SCS61_1		
			FRCK0_0		
			TIOB4_1		
19	14	-	P35	I	J
			SCS62_1		
			IC03_0		
			TIOB5_1		
			INT08_1		
20	15	-	P36	I	N
			IC02_0		
			SIN5_2		
			INT09_1		
			WKUP11		
21	16	-	P37	I	J
			IC01_0		
			SOT5_2		
			INT10_1		
22	17	-	P38	F	J
			IC00_0		
			SCK5_2		
			INT11_1		

Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
80	70	-	P1E	H	L
			RTS4_1		
			FRCK0_1		
			ADTG_5		
			INT23_2		
			AN14		
81	-	-	P28	F	I
			RTO05_1		
			TIOB6_2		
			ADTG_4		
82	-	-	P27	G	L
			RTO04_1		
			TIOA6_2		
			INT02_2		
			AN15		
83	-	-	P26	F	I
			SCK2_1		
			RTO03_1		
84	-	-	P25	F	I
			SOT2_1		
			RTO02_1		
85	-	-	P24	F	J
			SIN2_1		
			RTO01_1		
			INT17_1		
86	71	58	P23	H	K
			SCK0_0		
			TIOA7_1		
			RTO00_1		
87	72	59	AN16	H	K
			P22		
			SOT0_0		
			TIOB7_1		
88	73	60	AN17	H	P
			P21		
			SIN0_0		
			INT06_1		
			WKUP2		
			AN18		

List of Pin Functions

The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.

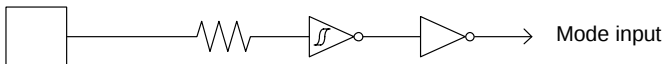
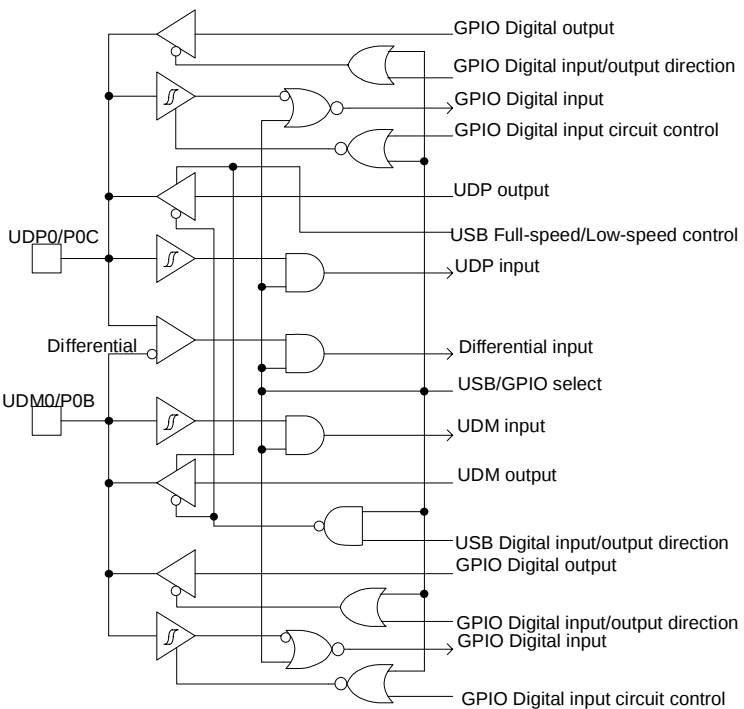
Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
ADC	ADTG_0	A/D converter external trigger input pin	99	84	66
	ADTG_1		7	7	7
	ADTG_2		23	18	13
	ADTG_3		114	94	74
	ADTG_4		81	-	-
	ADTG_5		80	70	-
	ADTG_6		17	12	12
	ADTG_7		35	30	-
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	62	52	42
	AN01		63	53	43
	AN02		64	54	44
	AN03		65	55	45
	AN04		66	56	46
	AN05		67	57	47
	AN06		68	58	48
	AN07		69	59	49
	AN08		74	64	54
	AN09		75	65	55
	AN10		76	66	56
	AN11		77	67	57
	AN12		78	68	-
	AN13		79	69	-
	AN14		80	70	-
	AN15		82	-	-
	AN16		86	71	58
	AN17		87	72	59
	AN18		88	73	60
	AN19		89	74	-
	AN20		97	82	-
	AN21		98	83	-
	AN22		99	84	66
	AN23		100	85	-
Base Timer 0	TIOA0_0	Base timer ch.0 TIOA pin	32	27	-
	TIOA0_1		24	19	14
	TIOA0_2		100	85	-
	TIOB0_0	Base timer ch.0 TIOB pin	47	42	32
	TIOB0_1		14	9	9
	TIOB0_2		101	86	-

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
External Interrupt	INT15_0	External interrupt request 15 input pin	68	58	48
	INT15_1		116	96	76
	INT15_2		54	-	-
	INT16_0	External interrupt request 16 input pin	100	85	-
	INT16_1		11	-	-
	INT16_2		12	-	-
	INT17_0	External interrupt request 17 input pin	101	86	-
	INT17_1		85	-	-
	INT17_2		13	-	-
	INT18_0	External interrupt request 18 input pin	103	88	68
	INT18_1		6	6	6
	INT18_2		26	21	16
	INT19_0	External interrupt request 19 input pin	104	89	69
	INT19_1		7	7	7
	INT19_2		28	23	18
	INT20_0	External interrupt request 20 input pin	105	90	70
	INT20_1		117	97	77
	INT20_2		77	67	57
	INT21_0	External interrupt request 21 input pin	106	91	71
	INT21_1		47	42	32
	INT21_2		78	68	-
	INT22_0	External interrupt request 22 input pin	109	-	-
	INT22_1		48	43	33
	INT22_2		79	69	-
	INT23_0	External interrupt request 23 input pin	111	-	-
	INT23_1		99	84	66
	INT23_2		80	70	-
GPIO	NMIX	Non-Maskable Interrupt input pin	107	92	72
	P00	General-purpose I/O port 0	92	77	61
	P01		93	78	62
	P02		94	79	63
	P03		95	80	64
	P04		96	81	65
	P05		97	82	-
	P06		98	83	-
	P07		99	84	66
	P08		100	85	-
	P09		101	86	-
	P0A		102	87	67
	P0B		103	88	68
	P0C		104	89	69
	P0D		105	90	70
	P0E		106	91	71
	P0F		107	92	72

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
GPIO	P40	General-purpose I/O port 4	32	27	-
	P41		33	28	-
	P42		34	29	-
	P43		35	30	-
	P44		36	31	21
	P45		37	32	22
	P46		42	37	27
	P47		43	38	28
	P48		44	39	29
	P49		45	40	30
	P4A		47	42	32
	P4B		48	43	33
	P4C		49	44	34
	P4D		50	45	35
	P50	General-purpose I/O port 5	2	2	2
	P51		3	3	3
	P52		4	4	4
	P53		5	5	5
	P54		6	6	6
	P55		7	7	7
	P56		8	8	8
	P57		9	-	-
	P58		10	-	-
	P59		11	-	-
	P5A		12	-	-
	P5B		13	-	-
	P60	General-purpose I/O port 6	116	96	76
	P61		115	95	75
	P62		114	94	74
	P63		113	93	73
	P64		112	-	-
	P65		111	-	-
	P66		110	-	-
	P67		109	-	-
	P68		108	-	-
	P70	General-purpose I/O port 7	51	-	-
	P71		52	-	-
	P72		53	-	-
	P73		54	-	-
	P74		55	-	-
	P80	General-purpose I/O port 8	117	97	77
	P81		118	98	78
	P82		119	99	79
	PE0*	General-purpose I/O port E	56	46	36
	PE2		58	48	38
	PE3		59	49	39

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
Multi-function Serial 3	SIN3_0	Multi-function serial interface ch.3 input pin	110	-	-
	SIN3_1		2	2	2
	SIN3_2		94	79	63
	SOT3_0 (SDA3_0)	Multi-function serial interface ch.3 output pin.	109	-	-
	SOT3_1 (SDA3_1)	This pin operates as SOT3 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA3 when used as an I ² C pin (operation mode 4).	3	3	3
	SOT3_2 (SDA3_2)		92	77	61
	SCK3_0 (SCL3_0)	Multi-function serial interface ch.3 clock I/O pin.	108	-	-
	SCK3_1 (SCL3_1)	This pin operates as SCK3 when used as a CSIO (operation mode 2) and as SCL3 when used as an I ² C pin (operation mode 4).	4	4	4
	SCK3_2 (SCL3_2)		96	81	65
Multi-function Serial 4	SIN4_0	Multi-function serial interface ch.4 input pin	102	87	67
	SIN4_1		76	66	56
	SIN4_2		97	82	-
	SOT4_0 (SDA4_0)	Multi-function serial interface ch.4 output pin.	99	84	66
	SOT4_1 (SDA4_1)	This pin operates as SOT4 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA4 when used as an I ² C pin (operation mode 4).	77	67	57
	SOT4_2 (SDA4_2)		98	83	-
	SCK4_0 (SCL4_0)	Multi-function serial interface ch.4 clock I/O pin.	107	92	72
	SCK4_1 (SCL4_1)	This pin operates as SCK4 when used as a CSIO (operation mode 2) and as SCL4 when used as an I ² C pin (operation mode 4).	78	68	-
	SCK4_2 (SCL4_2)		99	84	66
	CTS4_0	Multi-function serial interface ch4 CTS input pin	106	91	71
	CTS4_1		79	69	-
	CTS4_2		100	85	-
	RTS4_0	Multi-function serial interface ch4 RTS input pin	105	90	70
	RTS4_1		80	70	-
	RTS4_2		101	86	-

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
Real-time Clock	RTCCO_0	0.5-seconds pulse output pin of Real-time clock	107	92	72
	RTCCO_1		65	55	45
	RTCCO_2		24	19	14
	SUBOUT_0	Sub clock output pin	107	92	72
	SUBOUT_1		65	55	45
	SUBOUT_2		24	19	14
HDMI-CEC/ Remote Control Reception	CEC0_0	HDMI-CEC/Remote Control Reception ch.0 input/output pin	49	44	34
	CEC0_1		102	87	67
	CEC1_0	HDMI-CEC/Remote Control Reception ch.1 input/output pin	116	96	76
	CEC1_1		8	8	8
Low-Power Consumption Mode	WKUP0	Deep standby mode return signal input pin	107	92	72
	WKUP1		63	53	43
	WKUP2		88	73	60
	WKUP3		116	96	76
	WKUP4		14	9	9
	WKUP5		102	87	67
	WKUP6		50	45	35
	WKUP7		48	43	33
	WKUP8		28	23	18
	WKUP9		8	8	8
	WKUP10		97	82	-
	WKUP11		20	15	-
VBAT	LVDI	Input pin to monitor the external voltage.	37	32	22
	VWAKEUP	The return signal input pin from a hibernation state	45	40	30
	VREGCTL	On-board regulator control pin	44	39	29
Reset	INITX	External Reset Input pin. A reset is valid when INITX="L".	41	36	26
Mode	MD0	Mode 0 pin. During normal operation, input MD0="L". During serial programming to Flash memory, input MD0="H".	57	47	37
	MD1	Mode 1 pin. During normal operation, input is not needed. During serial programming to Flash memory, MD1 = "L" must be input.	56	46	36
Power	VCC	Power supply pin	1	1	1
			31	26	-
			40	35	25
			61	51	41
			91	76	-
VBAT Power	VBAT	VBAT power supply pin Backup power supply (battery etc.) and system power supply	46	41	31

Type	Circuit	Remarks
J		• CMOS level hysteresis input
K		It is possible to select the USB I/O / GPIO function. When the USB I/O is selected. • Full-speed, Low-speed control When the GPIO is selected. • CMOS level output • CMOS level hysteresis input • With standby mode control

6.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

(1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

(2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

(3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

(4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

(5) Smoke, Flame

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Spansion products in other special environmental conditions should consult with sales representatives.

Please check the latest handling precautions at the following URL.

<http://www.spansion.com/fj/documents/fj/datasheet/e-ds/DS00-00004.pdf>

Pin Status Type	Function Group	State Upon Power-on Reset or Low-Voltage Detection	State at INITX Input	State Upon Device Internal Reset	State in Run Mode or Sleep Mode	State in Timer Mode, RTC Mode, or Stop Mode		State in Deep Standby RTC Mode or Deep Standby Stop Mode State		State when Return from Deep Standby Mode State					
		Power Supply Unstable	Power Supply Stable	Power Supply Stable	Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable					
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1					
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-					
N	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled					
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected / Internal input fixed at 0					
	External interrupt enabled selected							GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0						
	Resource other than above selected														
	GPIO selected														
O	CEC enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state					
O	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected / Internal input fixed at 0					
	External interrupt enabled selected							GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0						
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled											
	GPIO selected														

Parameter	Symbol (Pin Name)	Conditions		Value		Unit	Remarks
				Typ	Max		
Power supply current	I _{CCVBAT} (VBAT)	RTC operation	T _A =25°C V _{CC} =3.0V 32 kHz Crystal oscillation	0.9	TBD	μA	*1
			T _A =25°C V _{CC} =1.65 V 32 kHz Crystal oscillation	0.8	TBD	μA	*1
			T _A =105°C V _{CC} =3.6V 32 kHz Crystal oscillation	-	TBD	μA	*1
		RTC stop	T _A =25°C V _{CC} =3.0V	0.05	TBD	μA	*1
			T _A =25°C V _{CC} =1.65 V	0.02	TBD	μA	*1
			T _A =105°C V _{CC} =3.6V	-	TBD	μA	*1

*1: All ports are fixed.

LVD Current

 (V_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Typ	Max		
Low-Voltage detection circuit (LVD) power supply current	I _{CC} LVD	VCC	At operation	0.13	TBD	μA	For occurrence of reset
				0.13	TBD	μA	For occurrence of interrupt

Flash Memory Current

 (V_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Typ	Max		
Flash memory write/erase current	I _{CC} FLASH	VCC	At Write/Erase	9.5	TBD	mA	

A/D converter Current

 (V_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Typ	Max		
Power supply current	I _{CC} AD	AVCC	At operation	0.7	TBD	mA	
			At stop	0.13	TBD	μA	
Reference power supply current (AVRH)	I _{CC} AVRH	AVRH	At operation	1.1	TBD	mA	AVRH=3.6 V
			At stop	0.1	TBD	μA	

11.4.4 Operating Conditions of Main PLL

(In the Case of Using the Main Clock as the Input Clock of the PLL)

($V_{CC}=AV_{CC}=1.65\text{ V}$ to 3.6 V , $V_{SS}=AV_{SS}=0\text{ V}$, $T_A=-40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time* ¹ (LOCK UP time)	t_{LOCK}	100	-	-	μs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiple rate	-	5	-	37	multiple	
PLL macro oscillation clock frequency	f_{PLLO}	75	-	150	MHz	
Main PLL clock frequency* ²	f_{CLKPLL}	-	-	40.8	MHz	
USB clock frequency* ³	f_{CLKSPLL}	-	-	48	MHz	

*1: The wait time is the time it takes for PLL oscillation to stabilize.

*2: For details of the main PLL clock (CLKPLL), refer to "Chapter: Clock" in "FM0+ Family Peripheral Manual".

*3: For more information about USB clock, see "Chapter: USB Clock Generation" in "FM0+ Family Peripheral Manual Communication Macro Part".

11.4.5 Operating Conditions of Main PLL

(In the Case of Using the Built-in High-Speed CR Clock as the Input Clock of the Main PLL)

($V_{CC}=AV_{CC}=1.65\text{ V}$ to 3.6 V , $V_{SS}=AV_{SS}=0\text{ V}$, $T_A=-40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$)

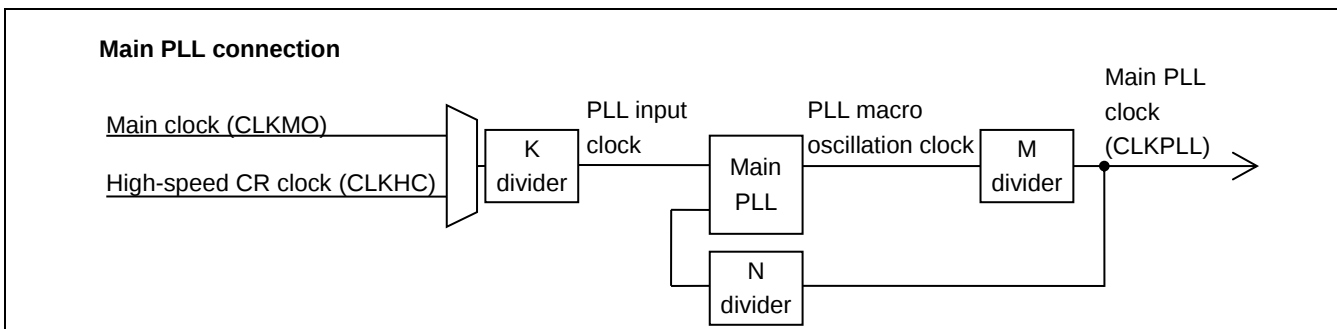
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time* ¹ (LOCK UP time)	t_{LOCK}	100	-	-	μs	
PLL input clock frequency	f_{PLLI}	3.8	4	4.2	MHz	
PLL multiple rate	-	19	-	35	multiple	
PLL macro oscillation clock frequency	f_{PLLO}	72	-	150	MHz	
Main PLL clock frequency* ²	f_{CLKPLL}	-	-	40.8	MHz	

*1: The wait time is the time it takes for PLL oscillation to stabilize.

*2: For details of the main PLL clock (CLKPLL), refer to "Chapter: Clock" in "FM0+ Family Peripheral Manual".

Note:

- For the main PLL source clock, input the high-speed CR clock (CLKHC) whose frequency has been trimmed. When setting PLL multiple rate, please take the accuracy of the built-in High-speed CR clock into account and prevent the master clock from exceeding the maximum frequency.



CSIO (SPI=0, SCINV=1)
 $(V_{CC}=AV_{CC}=1.65\text{ V to }3.6\text{ V}, V_{SS}=AV_{SS}=0\text{ V}, T_A=-40^{\circ}\text{C to }+105^{\circ}\text{C})$

Parameter	Symbol	Pin Name	Conditions	$V_{CC} < 2.7\text{ V}$		$V_{CC} \geq 2.7\text{ V}$		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4\ t_{CYCP}$	-	$4\ t_{CYCP}$	-	ns
SCK $\uparrow \rightarrow$ SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN $\rightarrow$ SCK $\downarrow$ setup time	t_{IVSLI}	SCKx, SINx		60	-	50	-	ns
SCK $\downarrow \rightarrow$ SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	$2\ t_{CYCP} - 10$	-	$2\ t_{CYCP} - 10$	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		$t_{CYCP} + 10$	-	$t_{CYCP} + 10$	-	ns
SCK $\uparrow \rightarrow$ SOT delay time	t_{SHOVE}	SCKx, SOTx		-	65	-	52	ns
SIN $\rightarrow$ SCK $\downarrow$ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK $\downarrow \rightarrow$ SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

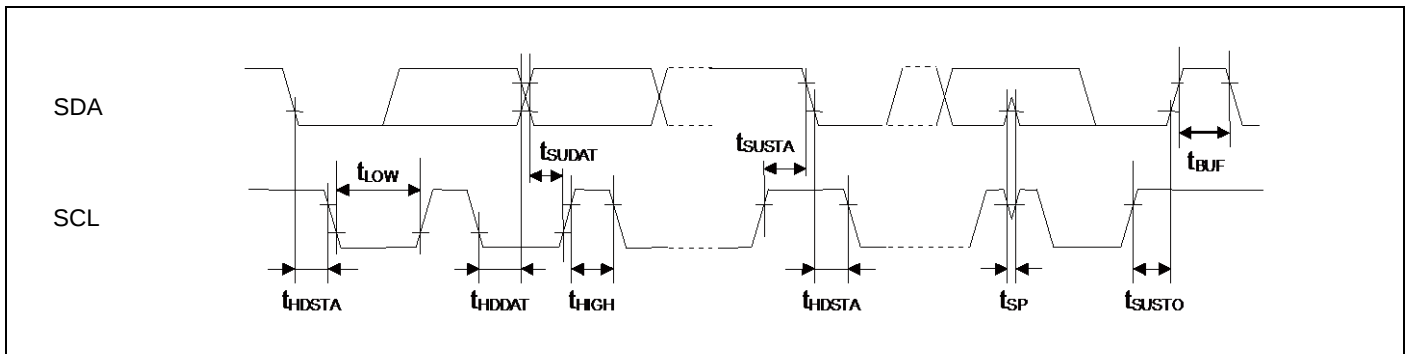
- The above AC characteristics are for clock synchronous mode.
- t_{CYCP} represents the APB bus clock cycle time.
For the number of the APB bus to which Multi-function Serial has been connected, see "8. Block Diagram".
- The characteristics are only applicable when the relocate port numbers are the same.
For instance, they are not applicable for the combination of SCKx_0 and SOTx_1.
- External load capacitance $C_L=30\text{ pF}$

11.4.11 I²C Timing

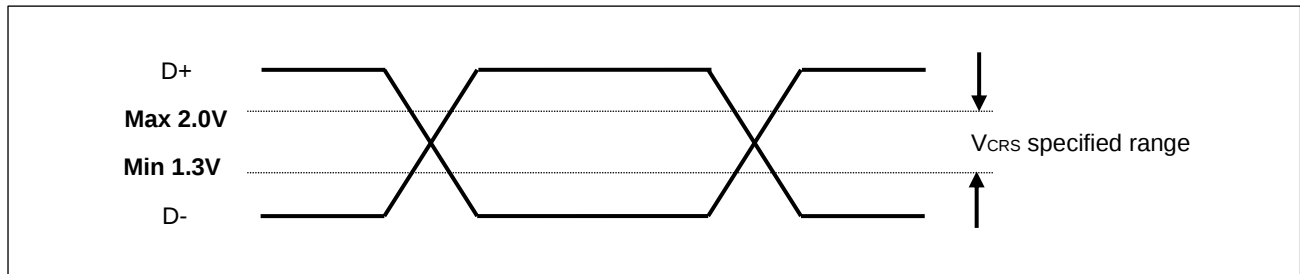
(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Conditions	Standard-Mode		Fast-Mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	f _{SCL}		0	100	0	400	kHz	
(Repeated) Start condition hold time SDA ↓ → SCL ↓	t _{HDSTA}	C _L =30 pF, R=(V _P /I _{OL})* ¹	4.0	-	0.6	-	μs	
SCL clock L width	t _{LOW}		4.7	-	1.3	-	μs	
SCL clock H width	t _{HIGH}		4.0	-	0.6	-	μs	
(Repeated) Start setup time SCL ↑ → SDA ↓	t _{SUSTA}		4.7	-	0.6	-	μs	
Data hold time SCL ↓ → SDA ↓ ↑	t _{HDDAT}		0	3.45* ²	0	0.9* ³	μs	
Data setup time SDA ↓ ↑ → SCL ↑	t _{SUDAT}		250	-	100	-	ns	
Stop condition setup time SCL ↑ → SDA ↑	t _{SUSTO}		4.0	-	0.6	-	μs	
Bus free time between Stop condition and Start condition	t _{BUF}		4.7	-	1.3	-	μs	
Noise filter	t _{SP}	-	2 t _{CYCP} * ⁴	-	2 t _{CYCP} * ⁴	-	ns	

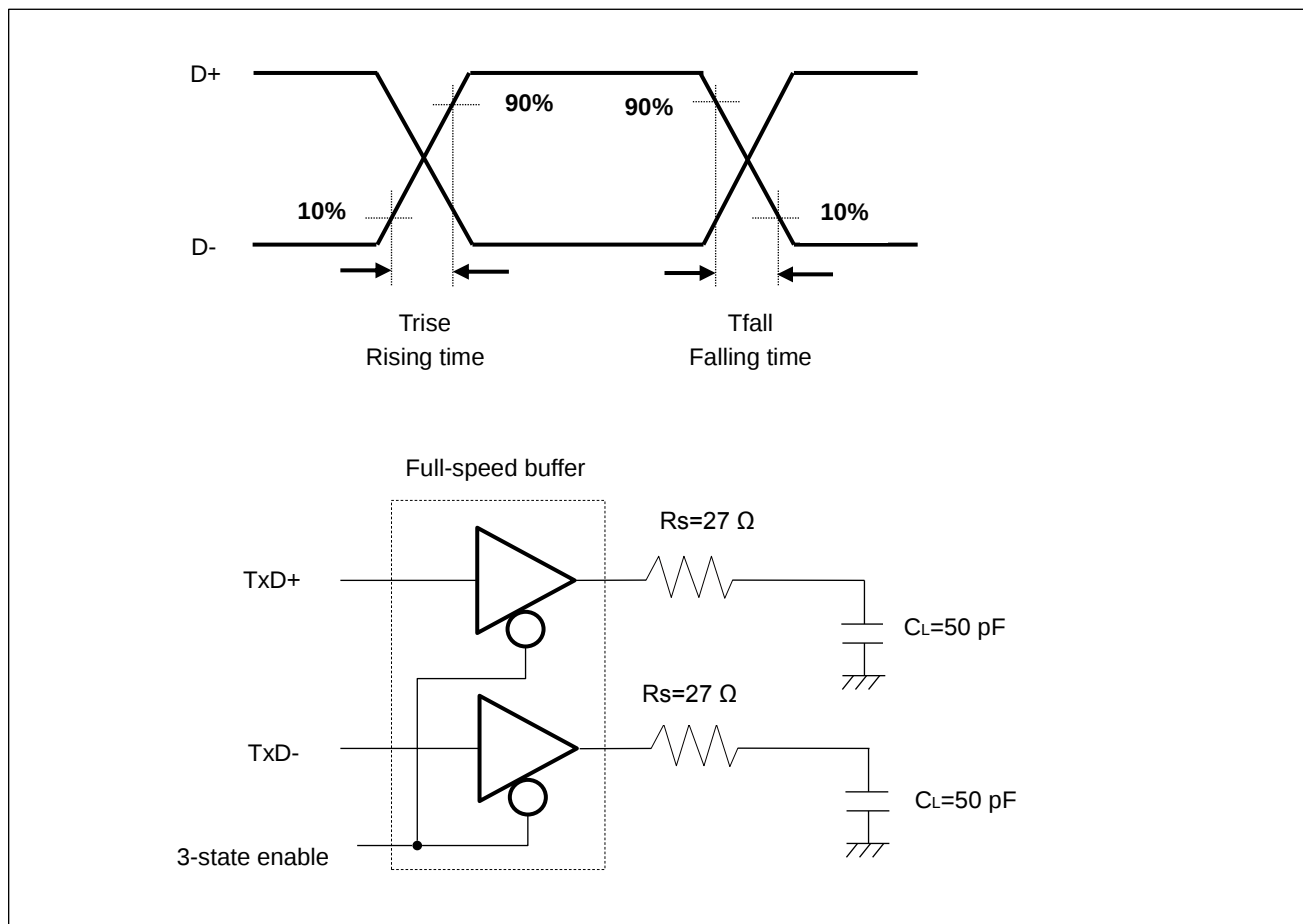
- *1: R represents the pull-up resistance of the SCL and SDA lines, and C_L the load capacitance of the SCL and SDA lines. V_P represents the power supply voltage of the pull-up resistance, and I_{OL} the V_{OL} guaranteed current.
- *2: The maximum t_{HDDAT} must satisfy at least the condition that the period during which the device is holding the SCL signal at L (t_{LOW}) does not extend.
- *3: A Fast-mode I²C bus device can be used in a Standard-mode I²C bus system, provided that the condition of t_{SUDAT} ≥ 250 ns is fulfilled.
- *4: t_{CYCP} represents the APB bus clock cycle time.
 For the number of the APB bus to which the I²C is connected, see "8. Block Diagram".
 To use Standard-mode, set the APB bus clock at 2 MHz or more.
 To use Fast-mode, set the APB bus clock at 8 MHz or more.



- *3 : The output drive capability of the driver is below 0.3 V at Low-state (V_{OL}) (to 3.6 V and 1.5 k Ω load), and 2.8 V or above (to the VSS and 1.5 k Ω load) at high-state (V_{OH})
- *4 : The cross voltage of the external differential output signal (D+ / D-) of USB I/O buffer is within 1.3 V to 2.0 V.



- *5 : The indicate rising time (T_{rise}) and falling time (T_{fall}) of the full-speed differential data signal. They are defined by the time between 10% and 90% of the output signal voltage. For full-speed buffer, T_r/T_f ratio is regulated as within $\pm 10\%$ to minimize RFI emission.



- *6 : USB Full-speed connection is performed via twist pair cable shield with $90 \Omega \pm 15\%$ characteristic impedance (Differential Mode). USB standard defines that output impedance of USB driver must be in range from 28Ω to 44Ω . So, discrete series resistor (R_s) addition is defined in order to satisfy the above definition and keep balance. When using this USB I/O, use it with 25Ω to 33Ω (recommendation value : 27Ω) series resistor R_s .

11.9.2 Return Factor: Reset

The return time from Low-Power consumption mode is indicated as follows. It is from releasing reset to starting the program operation.

Return Count Time

($V_{CC}=1.65\text{ V to }3.6\text{ V}$, $T_A=-40^{\circ}\text{C to }+105^{\circ}\text{C}$)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t_{RCNT}	10 ^{*1} 40 ^{*2}	70	μs	*1 : HCR ON.(HCR/MOSC/PLL mode) *2 : HCR OFF.(LCR/SOS mode)
High-speed CR Timer mode, Main Timer mode, PLL Timer mode		20	30	μs	
Low-speed CR Timer mode		61	114	μs	
Sub Timer mode		61	114	μs	
RTC/Stop mode		38	85	μs	
Deep RTC mode, Deep Stop mode		46	95	μs	

*: The maximum value depends on the accuracy of built-in CR.

Operation Example of Return from Low-Power Consumption Mode (by INITX)

