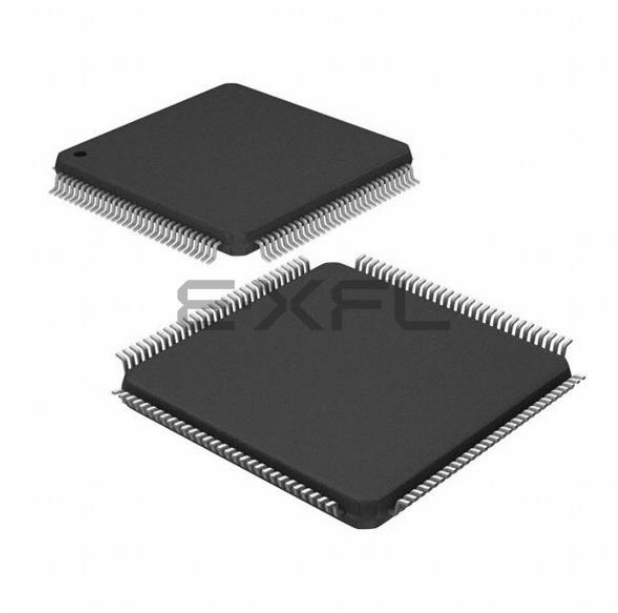

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

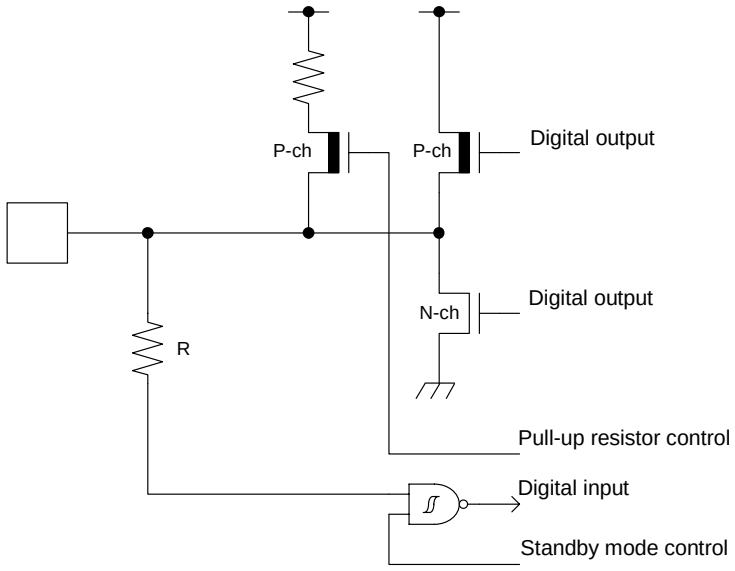
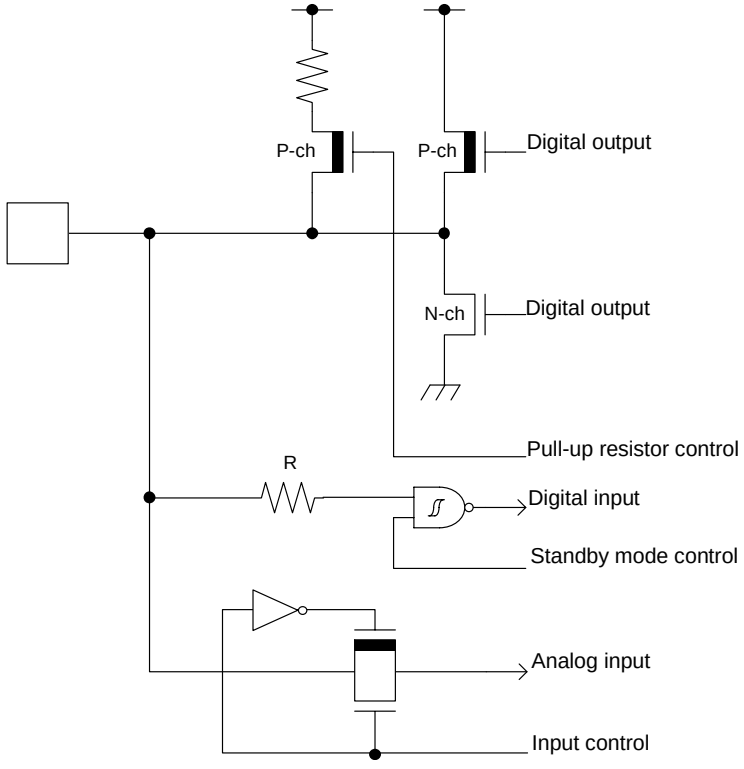
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, SmartCard, UART/USART, USB
Peripherals	I²S, LVD, POR, PWM, WDT
Number of I/O	102
Program Memory Size	304KB (304K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e1b34g0agv20000

Table of Contents

Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
34	29	-	P42 TIOA2_0 SCK1_2 IC0_VPEN_1 INT08_0	F	J
35	30	-	P43 TIOA3_0 CTS1_2 ADTG_7 IC0_RST_1 INT09_0	F	J
36	31	21	P44 TIOA4_0 IC0_DATA_1 INT10_0 RTS1_2	I	J
37	32	22	P45 TIOA5_0 IC0_CIN_1 LVDI	I	I
38	33	23	C	-	-
39	34	24	VSS	-	-
40	35	25	VCC	-	-
41	36	26	INITX	B	C
42	37	27	P46 X0A	D	E
43	38	28	P47 X1A	E	F
44	39	29	P48 VREGCTL	I	I
45	40	30	P49 VWAKEUP	I	I
46	41	31	VBAT	-	-
47	42	32	P4A TIOB0_0 SCS70_1 INT21_1	I	J
48	43	33	P4B TIOB1_0 SIN7_1 INT22_1 WKUP7 IGTRG0_0	I	N
49	44	34	P4C TIOB2_0 SOT7_1 CEC0_0 INT12_0	I	R
50	45	35	P4D TIOB3_0 SCK7_1 INT13_0 WKUP6	I	N

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
External Interrupt	INT00_0	External interrupt request 00 input pin	2	2	2
	INT00_1		97	82	-
	INT00_2		102	87	67
	INT01_0	External interrupt request 01 input pin	3	3	3
	INT01_1		98	83	-
	INT02_0	External interrupt request 02 input pin	4	4	4
	INT02_1		63	53	43
	INT02_2		82	-	-
	INT03_0	External interrupt request 03 input pin	113	93	73
	INT03_1		66	56	46
	INT03_2		14	9	9
	INT04_0	External interrupt request 04 input pin	17	12	12
	INT04_1		69	59	49
	INT04_2		15	10	10
	INT05_0	External interrupt request 05 input pin	89	74	-
	INT05_1		76	66	56
	INT05_2		16	11	11
	INT06_0	External interrupt request 06 input pin	23	18	13
	INT06_1		88	73	60
	INT06_2		96	81	65
	INT07_0	External interrupt request 07 input pin	24	19	14
	INT07_1		114	94	74
	INT07_2		5	5	5
	INT08_0	External interrupt request 08 input pin	34	29	-
	INT08_1		19	14	-
	INT08_2		8	8	8
	INT09_0	External interrupt request 09 input pin	35	30	-
	INT09_1		20	15	-
	INT10_0	External interrupt request 10 input pin	36	31	21
	INT10_1		21	16	-
	INT10_2		112	-	-
	INT11_0	External interrupt request 11 input pin	118	98	78
	INT11_1		22	17	-
	INT11_2		110	-	-
	INT12_0	External interrupt request 12 input pin	49	44	34
	INT12_1		32	27	-
	INT12_2		108	-	-
	INT13_0	External interrupt request 13 input pin	50	45	35
	INT13_1		33	28	-
	INT13_2		52	-	-
	INT14_0	External interrupt request 14 input pin	67	57	47
	INT14_1		92	77	61
	INT14_2		53	-	-

Type	Circuit	Remarks
F		・CMOS level output ・CMOS level hysteresis input ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33 kΩ ・I_{OH} = -4 mA, I_{OL} = 4 mA ・When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
G		・CMOS level output ・CMOS level hysteresis input ・With input control ・Analog input ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33 kΩ ・I_{OH}= -4 mA, I_{OL}= 4 mA ・When this pin is used as an I^2C pin, the digital output P-ch transistor is always off

Latch-Up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

> CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:
>
> (1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
>
> (2) Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Spansion semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

6.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Spansion's recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

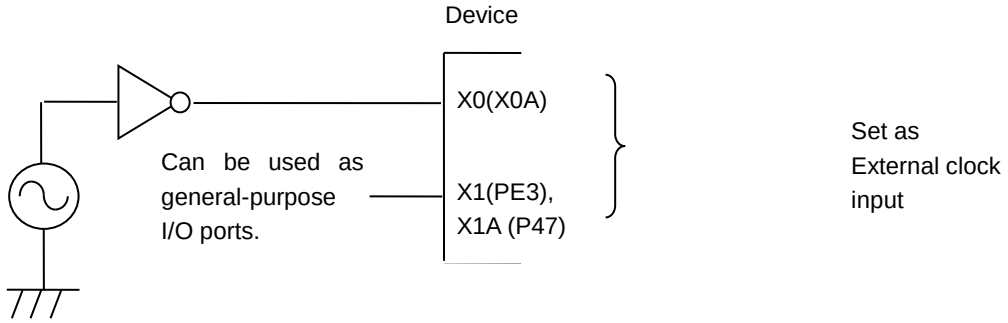
Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Spansion recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

Using an External Clock

When using an external clock as an input of the main clock, set X0/X1 to the external clock input, and input the clock to X0. X1(PE3) can be used as a general-purpose I/O port.
Similarly, when using an external clock as an input of the sub clock, set X0A/X1A to the external clock input, and input the clock to X0A. X1A (P47) can be used as a general-purpose I/O port.

Example of Using an External Clock

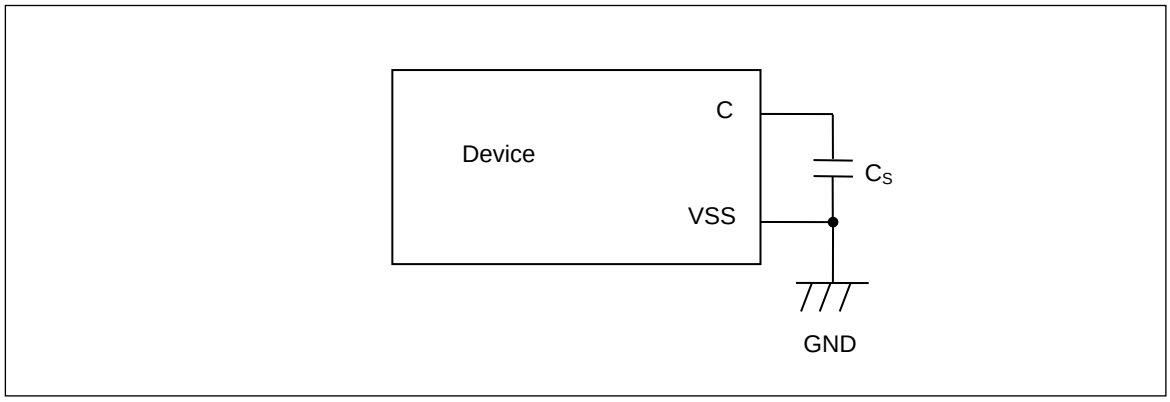


Handling when Using Multi-Function Serial Pin as I²C Pin

If it is using the multi-function serial pin as I²C pins, P-ch transistor of digital output is always disabled. However, I²C pins need to keep the electrical characteristic like other pins and not to connect to the external I²C bus system with power OFF.

C Pin

This series contains the regulator. Be sure to connect a smoothing capacitor (C_S) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor.
However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor.
A smoothing capacitor of about 4.7 µF would be recommended for this series.

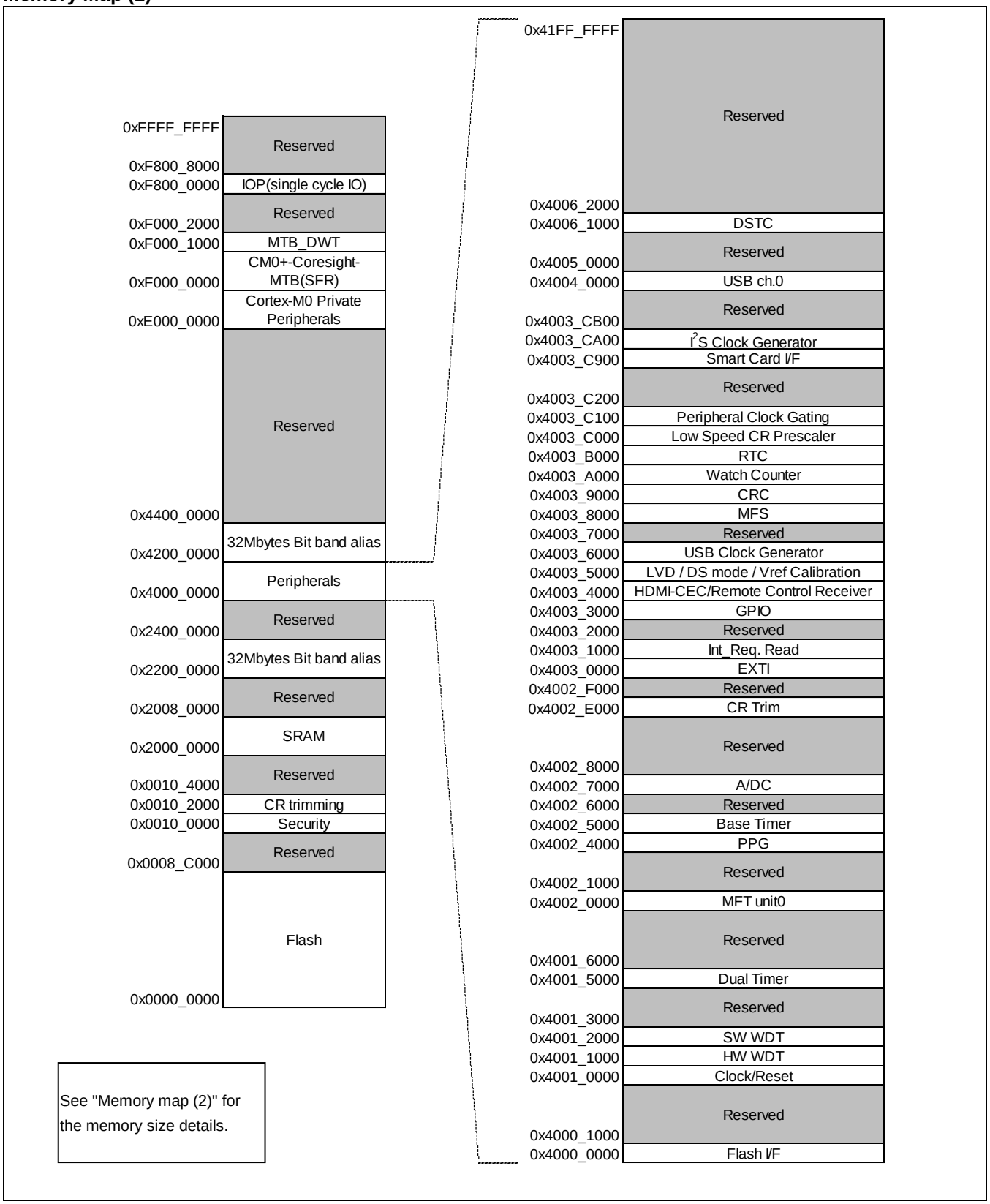


Mode Pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

9. Memory Map

Memory Map (1)



Pin Status Type	Function Group	State Upon Power-on Reset or Low-Voltage Detection	State at INITX Input	State Upon Device Internal Reset	State in Run Mode or Sleep Mode	State in Timer Mode, RTC Mode, or Stop Mode		State in Deep Standby RTC Mode or Deep Standby Stop Mode State		State when Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable	Power Supply Stable	Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
N	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected / Internal input fixed at 0
	External interrupt enabled selected							GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	
	Resource other than above selected						Hi-Z / Internal input fixed at 0			
	GPIO selected									
O	CEC enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected / Internal input fixed at 0
	External interrupt enabled selected							GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected									

11.2 Recommended Operating Conditions

(V_{SS}=AV_{SS}=0.0 V)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Power supply voltage	V_{CC}	-	1.65 *3	3.6	V	
			3.0	3.6	V	*1
Sub Oscillation frequency	Fin	-	-	-	kHz	Typical is 32.768 kHz
Analog power supply voltage	AV_{CC}	-	1.65	3.6	V	AV_{CC}=V_{CC}
Analog reference voltage	AVRH	-	2.7	AV_{CC}	V	AV_{CC} ≥ 2.7 V
			AV_{CC}	AV_{CC}	V	AV_{CC} < 2.7 V
	AVRL	-	AV_{SS}	AV_{SS}	V	
Smoothing capacitor	C_S	-	1	10	µF	For regulator*2
Operating temperature	T_A	-	- 40	+ 105	°C	

*1: When P0C/UDP0 and P0B/UDM0 pins are used as USB (UDP0, UDM0).

*2: See "C Pin" in "7. Handling Devices" for the connection of the smoothing capacitor.

*3: In between less than the minimum power supply voltage reset / interrupt detection voltage or more, instruction execution and low voltage detection function by built-in High-speed CR (including Main PLL is used) or built-in Low-speed CR is possible to operate only.

<WARNING>

1. *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.*
2. *Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.*
3. *No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet.*
4. *Users considering application outside the listed conditions are advised to contact their representatives beforehand.*

Peripheral Current Dissipation

(V_{CC}= 3.3 V, T_A=25°C)

Clock System	Peripheral	Conditions	Frequency (MHz)				Unit	Remarks
			4	8	20	40		
HCLK	GPIO	At all ports operation	0.02	0.04	0.11	0.22	mA	
	DSTC	At 2ch operation	0.07	0.15	0.37	0.74		
PCLK1	Base timer	At 4ch operation	0.02	0.04	0.08	0.16	mA	
	Multi-functional timer/PPG	At 1 unit/4ch operation	0.06	0.11	0.28	0.55		
	ADC	At 1 unit operation	0.02	0.04	010	0.20		
	Multi-function serial	At 1ch operation	0.03	0.06	0.16	0.31		

11.3.2 Pin Characteristics

(V_{CC} =AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

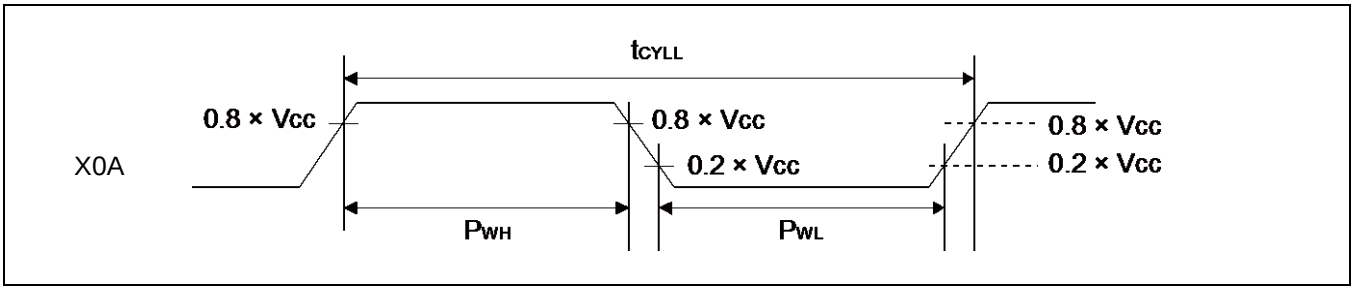
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
H level input voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0, MD1	V_{CC} ≥ 2.7 V	V_{CC} × 0.8	-	V_{CC} +0.3	V	
			V_{CC} < 2.7 V	V_{CC} × 0.7				
		5 V tolerant input pin	V_{CC} ≥ 2.7 V	V_{CC} × 0.8	-	V_{SS} +5.5	V	
			V_{CC} < 2.7 V	V_{CC} × 0.7				
L level input voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0, MD1	V_{CC} ≥ 2.7 V	V_{SS} - 0.3	-	V_{CC} × 0.2	V	
			V_{CC} < 2.7 V			V_{CC} × 0.3		
		5 V tolerant input pin	V_{CC} ≥ 2.7 V	V_{SS} - 0.3	-	V_{CC} × 0.2	V	
			V_{CC} < 2.7 V			V_{CC} × 0.3		
H level output voltage	V_{OH}	4 mA type	V_{CC} ≥ 2.7 V, I_{OH} = - 4 mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 2.7 V, I_{OH} = - 2 mA	V_{CC} - 0.45				
		The pin doubled as USB I/O	-	$USBV_{CC}$ - 0.4	-	$USBV_{CC}$	V	
L level output voltage	V_{OL}	4 mA type	V_{CC} ≥ 2.7 V, I_{OL} 4 mA	V_{SS}	-	0.4	V	
			V_{CC} < 2.7 V, I_{OL}=2 mA					
		The pin doubled as USB I/O	-	V_{SS}	-	0.4	V	
Input leak current	I_{IL}	-	-	- 5	-	+ 5	µA	
Pull-up resistance value	R_{PU}	Pull-up pin	V_{CC} ≥ 2.7 V	21	33	66	kΩ	
			V_{CC} < 2.7 V	-	-	134		
Input capacitance	C_{IN}	Other than VCC, USBVCC, VSS, AVCC, AVSS, AVRH	-	-	5	15	pF	

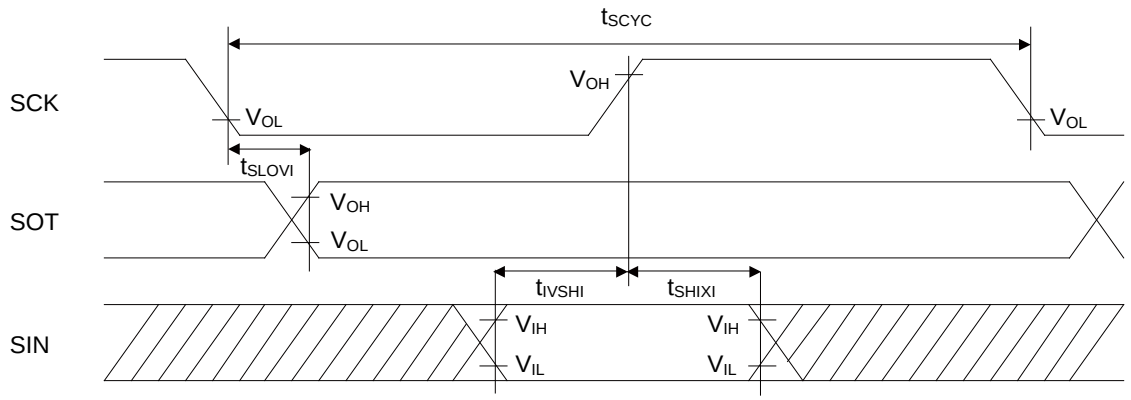
11.4.2 Sub Clock Input Characteristics

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

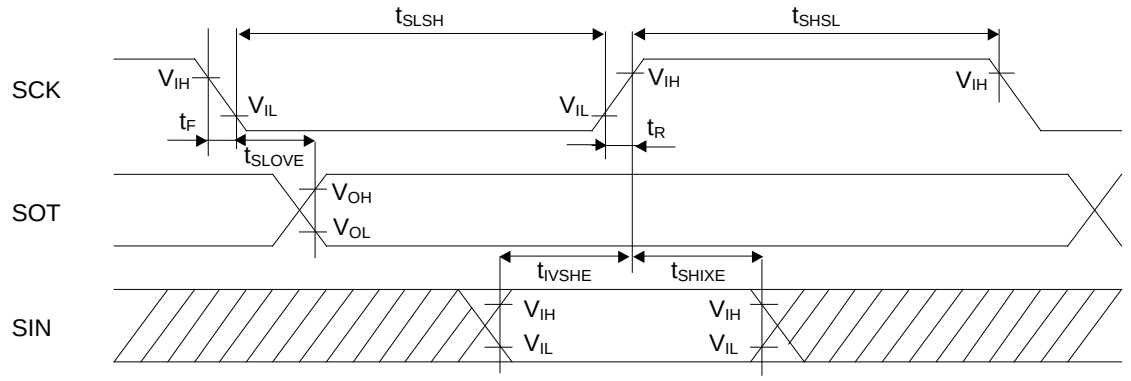
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	f_{CL}	X0A, X1A	-	-	32.768	-	kHz	When the crystal oscillator is connected*
			-	32	-	100	kHz	When the external clock is used
Input clock cycle	t_{CYLL}		-	10	-	31.25	µs	When the external clock is used
Input clock pulse width	-		P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	45	-	55	%	When the external clock is used

*: See "Sub crystal oscillator" in "7. Handling Devices" for the crystal oscillator used.





Master mode



Slave mode

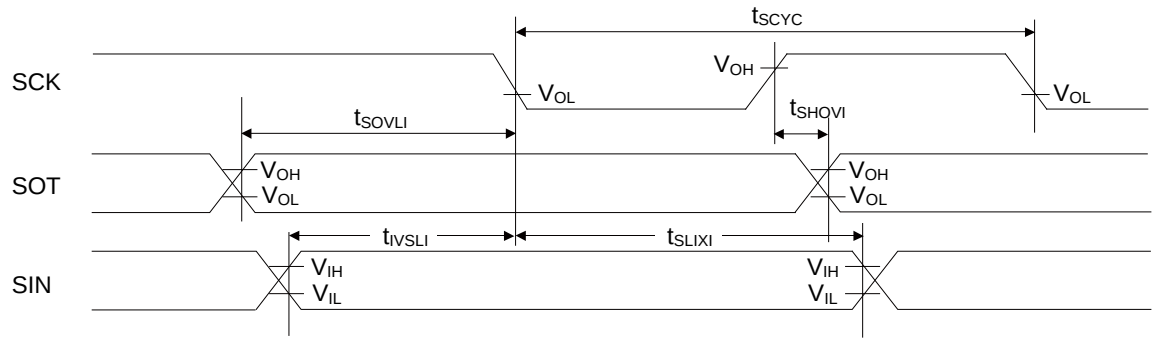
SPI (SPI=1, SCINV=0)

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

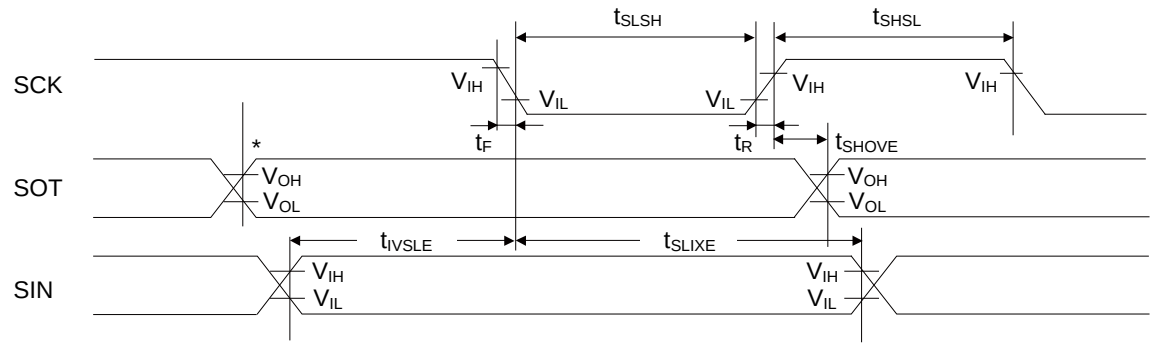
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	4 t_{CYCP}	-	4 t_{CYCP}	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		60	-	50	-	ns
SCK ↓→ SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCKx, SOTx		2 t_{CYCP} - 30	-	2 t_{CYCP} - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	2 t_{CYCP} - 10	-	2 t_{CYCP} - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} +10	-	t_{CYCP} +10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	65	-	52	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK ↓→ SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above AC characteristics are for clock synchronous mode.*
- *t_{CYCP} represents the APB bus clock cycle time.*
  For the number of the APB bus to which Multi-function Serial has been connected, see "8. Block Diagram ".
- *The characteristics are only applicable when the relocate port numbers are the same.*
  For instance, they are not applicable for the combination of SCKx_0 and SOTx_1.
- *External load capacitance C_L=30 pF*



Master mode



Slave mode

*: Changes when writing to TDR register

When Using CSIO/SPI Chip Select (SCINV=0, CSLVL=1)

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓ setup time	t_{CSSI}	Master mode	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50	(*3)+50	(*3)-50	(*3)+50	ns
SCS↓→SCK↓ setup time	t_{CSSE}	Slave mode	$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCK↑→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCS↓→SOT delay time	t_{DSE}		-	55	-	43	ns
SCS↑→SOT delay time	t_{DEE}		0	-	0	-	ns

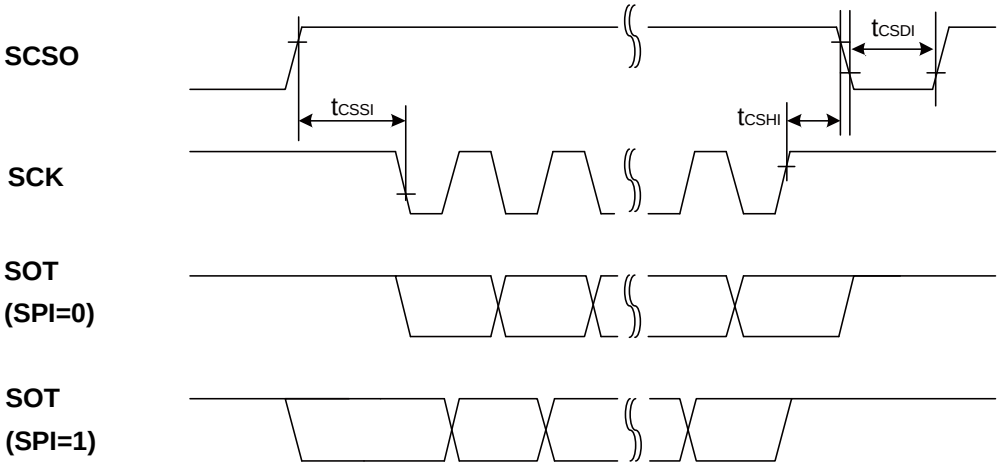
*1: CSSU bit value × serial chip select timing operating clock cycle.

*2: CSHD bit value × serial chip select timing operating clock cycle.

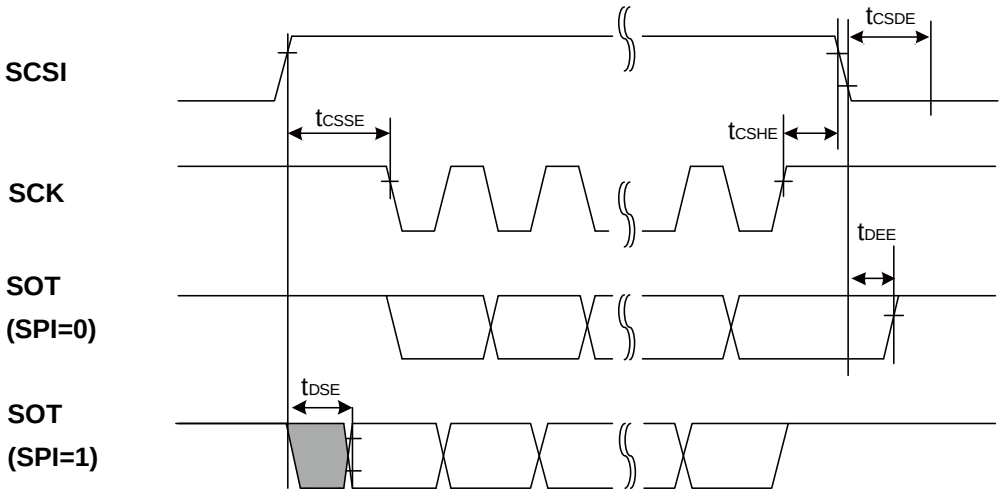
*3: CSDS bit value × serial chip select timing operating clock cycle.
Irrespective of CSDS bit setting, $5t_{CYCP}$ or more are required for the period the time when the serial chip select pin becomes inactive to the time when the serial chip select pin becomes active again.

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  For information about the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram ".
- *For information about CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family Peripheral Manual".*
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SCSIx_1 is not guaranteed.
- *When the external load capacitance C_L=30 pF.*



Master mode



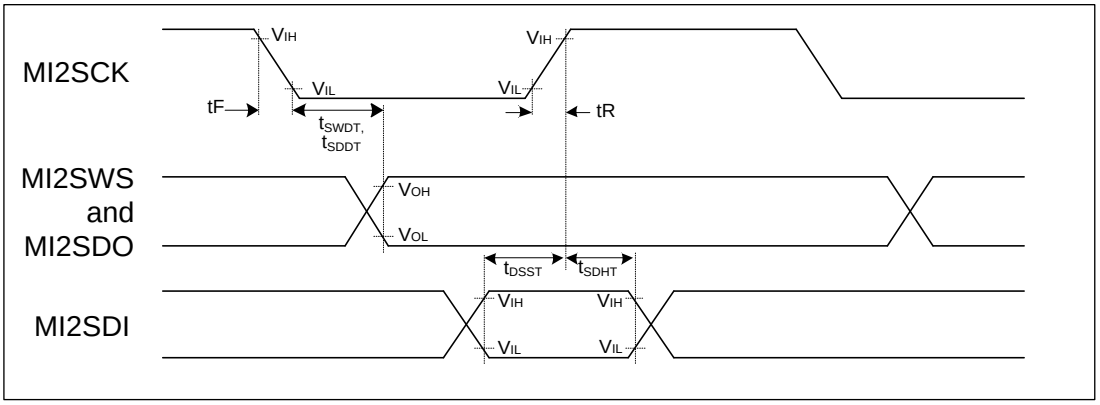
Slave mode

11.4.12 I²S Timing

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
				Min	Max	Min	Max	
MI2SCK max frequency (*1)	F_{MI2SCK}	MI2SCKx	C_L=30 pF	-	6.144	-	6.144	MHz
I²S clock cycle time (*1)	t_{ICYC}	MI2SCKx		4 t_{CYCP}	-	4 t_{CYCP}	-	ns
I²S clock Duty cycle	Δ	MI2SCKx		45%	55%	45%	55%	
MI2SCK ↓ → MI2SWS delay time	t_{SWDT}	MI2SCKx, MI2SWSx		-30	+30	-20	+20	ns
MI2SCK ↓ → MI2SDO delay time	t_{SDDT}	MI2SCKx, MI2SDOx		-30	+30	-20	+20	ns
MI2SDI → MI2SCK ↑ setup time	t_{DSST}	MI2SCKx, MI2SDIx		50	-	36	-	ns
MI2SCK ↑ → MI2SDI hold time	t_{SDHT}	MI2SCKx, MI2SDIx		0	-	0	-	ns
MI2SCK falling time	tF	MI2SCKx		-	5	-	5	ns
MI2SCK rising time	tR	MI2SCKx		-	5	-	5	ns

*1: I²S clock should meet the multiple of PCLK(t_{ICYC}) and the frequency less than F_{MI2SCK} meantime. The detail information please refer to Chapter I²S of Communication Macro Part of Peripheral Manual.



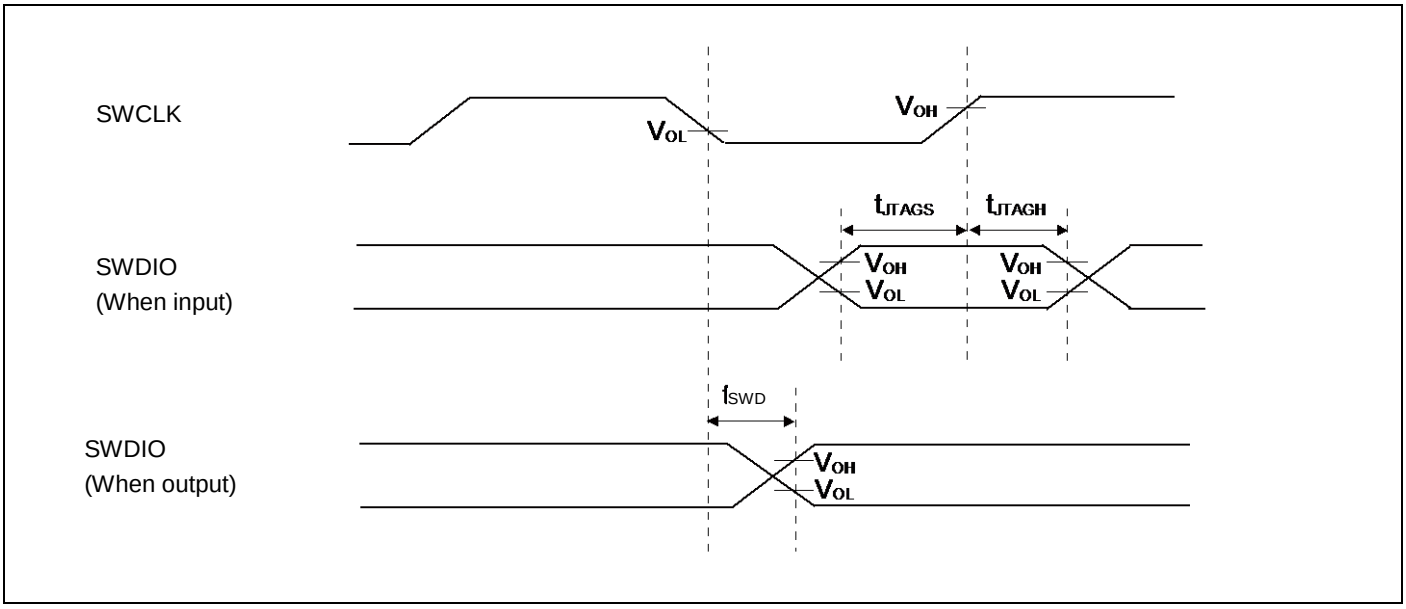
11.4.14 SW-DP Timing

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SWDIO setup time	t_{SWS}	SWCLK, SWDIO	-	15	-	ns	
SWDIO hold time	t_{SWH}	SWCLK, SWDIO	-	15	-	ns	
SWDIO delay time	t_{SWD}	SWCLK, SWDIO	-	-	45	ns	

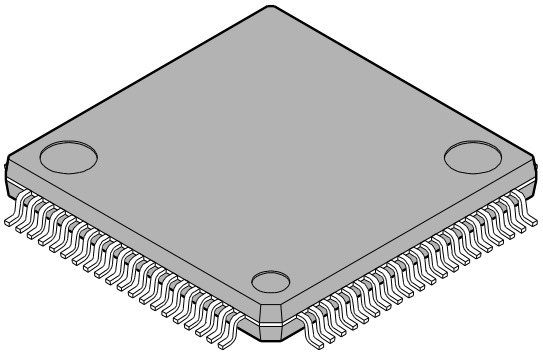
Note:

- *External load capacitance C_L=30 pF*



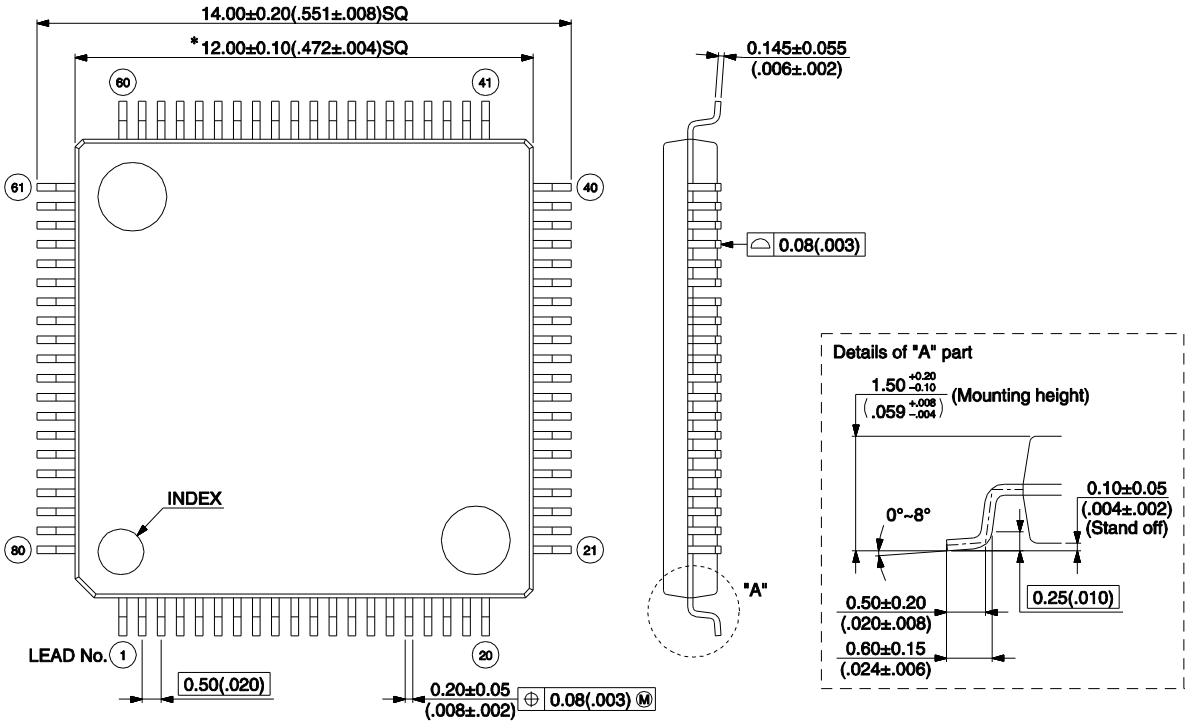
12. Ordering Information

Part Number	On-Chip Flash Memory	On-Chip SRAM	Package	Packing
S6E1B34E0AGV20000	304	32	Plastic • LQFP (0.50 mm pitch), 80 pins (FPT-80P-M21)	Tray
S6E1B36E0AGV20000	560	64		
S6E1B34F0AGV20000	304	32	Plastic • LQFP (0.50 mm pitch), 100 pins (FPT-100P-M20)	Tray
S6E1B36F0AGV20000	560	64		
S6E1B34G0AGV20000	304	32	Plastic • LQFP (0.50 mm pitch), 120 pins (FPT-120P-M21)	Tray
S6E1B36G0AGV20000	560	64		

80-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	12 mm × 12 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.47 g
(FPT-80P-M21)	Code (Reference)	P-LFQFP80-12×12-0.50

80-pin plastic LQFP
(FPT-80P-M21)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values