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What is "[Embedded - Microcontrollers](#)"?

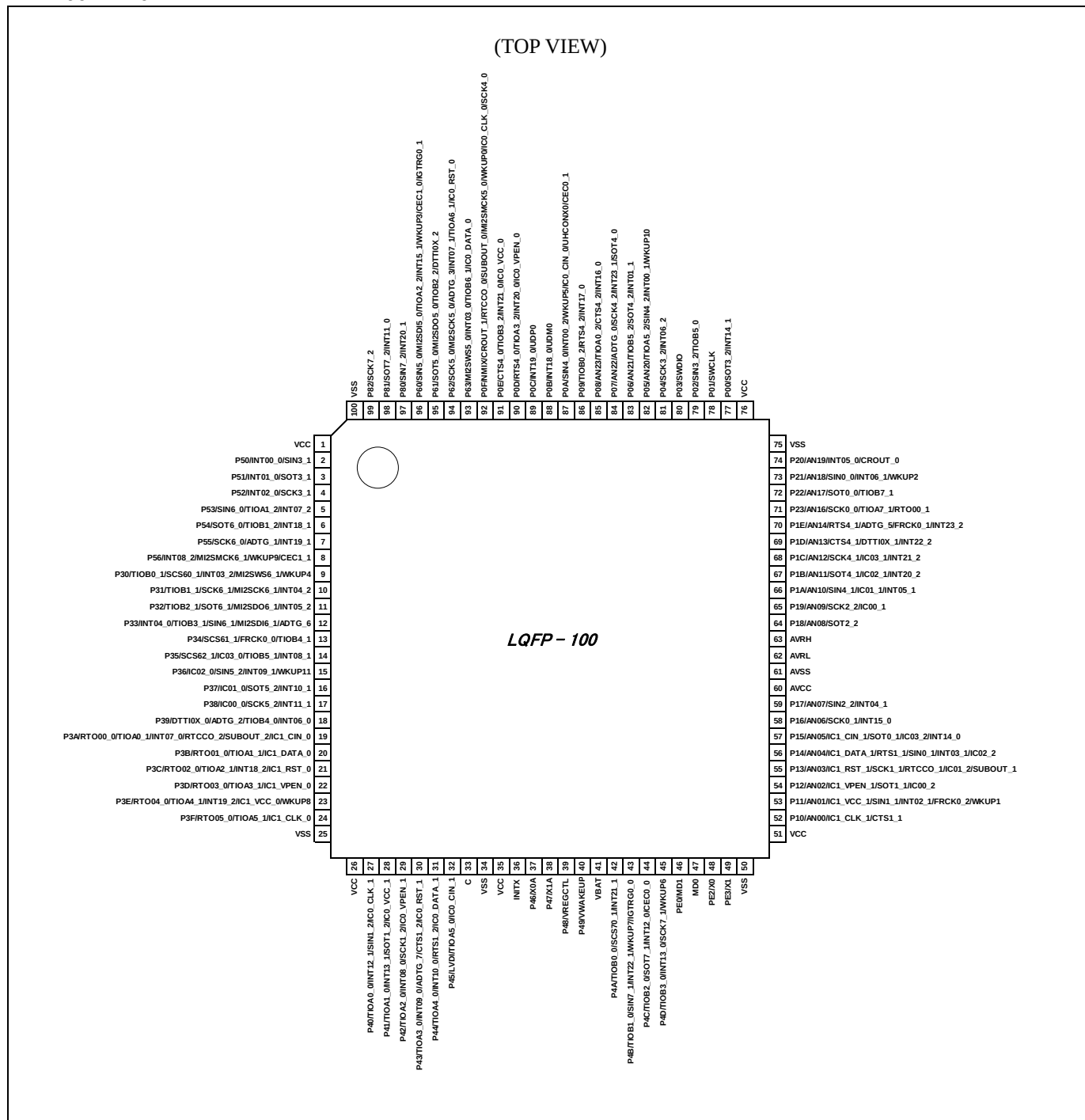
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

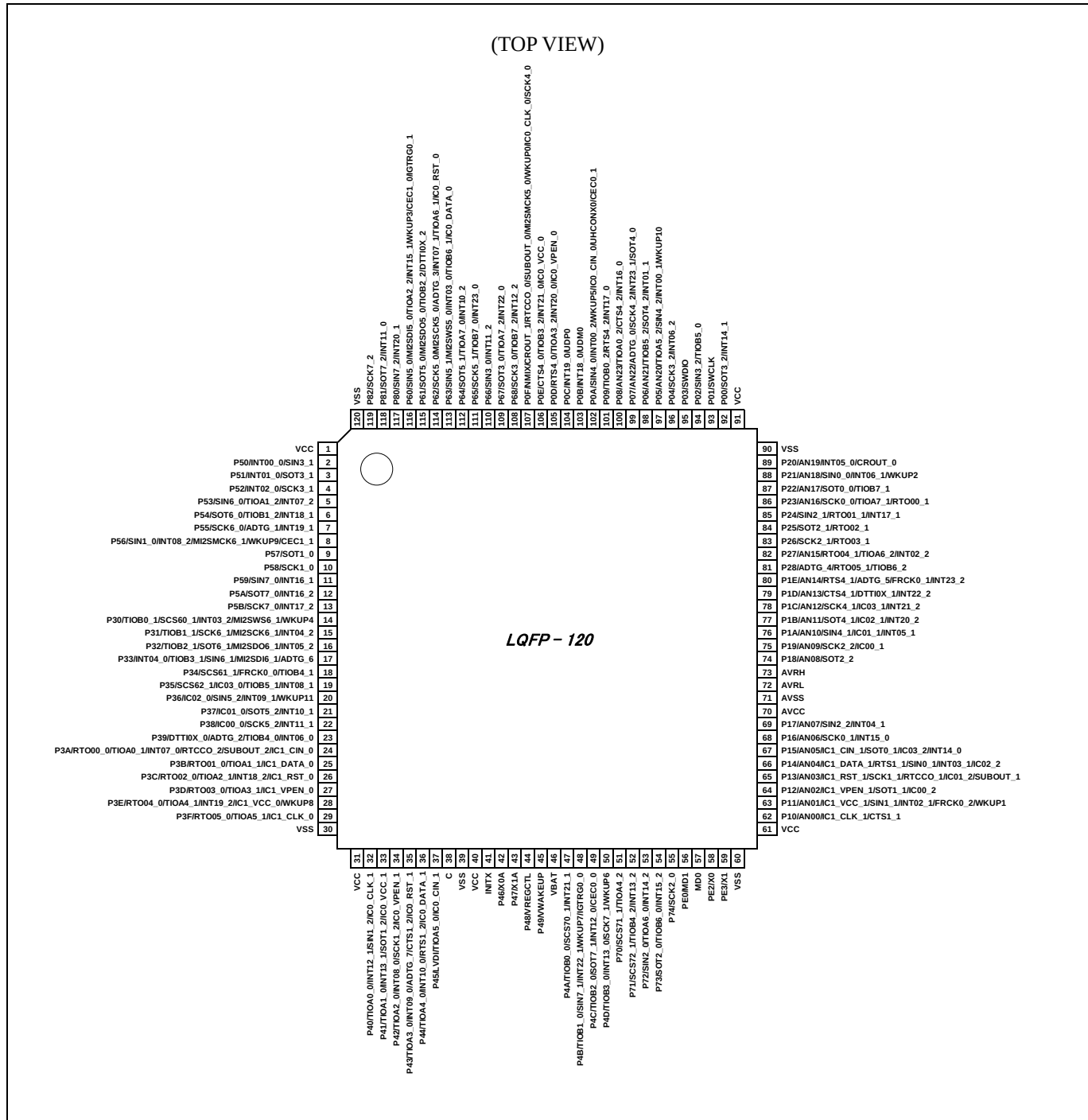
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I ² C, LINbus, SmartCard, UART/USART, USB
Peripherals	I ² S, LVD, POR, PWM, WDT
Number of I/O	102
Program Memory Size	560KB (560K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e1b36g0agv20000

FPT-100P-M20



Note:

- The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.

FPT-120P-M21

Note:

- The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.

Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
34	29	-	P42	F	J
			TIOA2_0		
			SCK1_2		
			IC0_VPEN_1		
			INT08_0		
35	30	-	P43	F	J
			TIOA3_0		
			CTS1_2		
			ADTG_7		
			IC0_RST_1		
36	31	21	INT09_0	I	J
			P44		
			TIOA4_0		
			IC0_DATA_1		
			INT10_0		
37	32	22	RTS1_2	I	I
			P45		
			TIOA5_0		
			IC0_CIN_1		
38	33	23	LVDI	-	-
39	34	24	C	-	-
40	35	25	VSS	-	-
41	36	26	VCC	-	-
42	37	27	INITX	B	C
42	37	27	P46	D	E
			X0A		
43	38	28	P47	E	F
			X1A		
44	39	29	P48	I	I
			VREGCTL		
45	40	30	P49	I	I
			VWAKEUP		
46	41	31	VBAT	-	-
47	42	32	P4A	I	J
			TIOB0_0		
			SCS70_1		
			INT21_1		
48	43	33	P4B	I	N
			TIOB1_0		
			SIN7_1		
			INT22_1		
			WKUP7		
			IGTRG0_0		
49	44	34	P4C	I	R
			TIOB2_0		
			SOT7_1		
			CEC0_0		
			INT12_0		
50	45	35	P4D	I	N
			TIOB3_0		
			SCK7_1		
			INT13_0		
			WKUP6		

Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
51	-	-	P70	F	I
			TIOA4_2		
			SCS71_1		
52	-	-	P71	F	J
			TIOB4_2		
			SCS72_1		
			INT13_2		
53	-	-	P72	F	J
			SIN2_0		
			TIOA6_0		
			INT14_2		
54	-	-	P73	F	J
			SOT2_0		
			TIOB6_0		
			INT15_2		
55	-	-	P74	F	I
			SCK2_0		
56	46	36	PE0	C	D
			MD1		
57	47	37	MD0	J	M
58	48	38	PE2	A	A
			X0		
59	49	39	PE3	A	B
			X1		
60	50	40	VSS	-	-
61	51	41	VCC	-	-
62	52	42	P10	H	K
			IC1_CLK_1		
			CTS1_1		
			AN00		
63	53	43	P11	H	P
			IC1_VCC_1		
			SIN1_1		
			FRCK0_2		
			INT02_1		
			WKUP1		
			AN01		
64	54	44	P12	H	K
			IC1_VPEN_1		
			SOT1_1		
			IC00_2		
			AN02		
65	55	45	P13	H	K
			IC1_RST_1		
			SCK1_1		
			RTCCO_1		
			IC01_2		
			SUBOUT_1		
			AN03		

List of Pin Functions

The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.

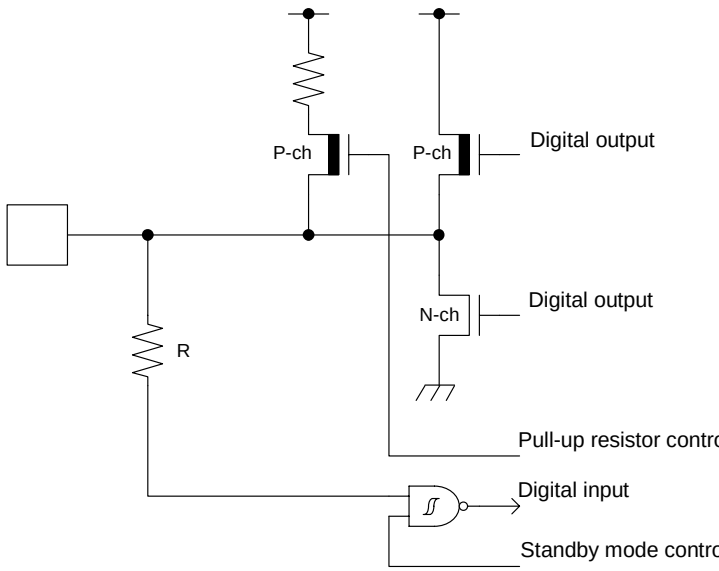
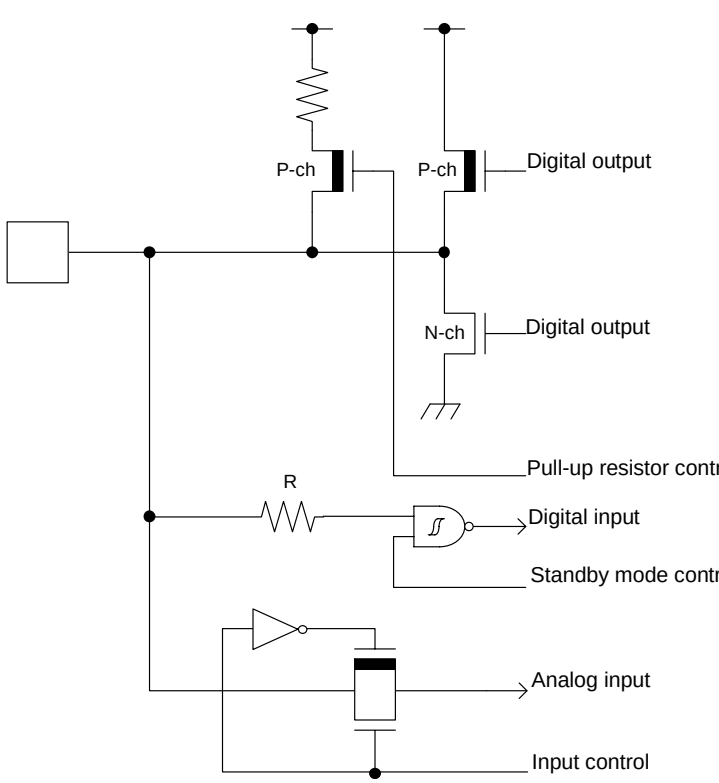
Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
ADC	ADTG_0	A/D converter external trigger input pin	99	84	66
	ADTG_1		7	7	7
	ADTG_2		23	18	13
	ADTG_3		114	94	74
	ADTG_4		81	-	-
	ADTG_5		80	70	-
	ADTG_6		17	12	12
	ADTG_7		35	30	-
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	62	52	42
	AN01		63	53	43
	AN02		64	54	44
	AN03		65	55	45
	AN04		66	56	46
	AN05		67	57	47
	AN06		68	58	48
	AN07		69	59	49
	AN08		74	64	54
	AN09		75	65	55
	AN10		76	66	56
	AN11		77	67	57
	AN12		78	68	-
	AN13		79	69	-
	AN14		80	70	-
	AN15		82	-	-
	AN16		86	71	58
	AN17		87	72	59
	AN18		88	73	60
	AN19		89	74	-
	AN20		97	82	-
	AN21		98	83	-
	AN22		99	84	66
	AN23		100	85	-
Base Timer 0	TIOA0_0	Base timer ch.0 TIOA pin	32	27	-
	TIOA0_1		24	19	14
	TIOA0_2		100	85	-
	TIOB0_0	Base timer ch.0 TIOB pin	47	42	32
	TIOB0_1		14	9	9
	TIOB0_2		101	86	-

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
Base Timer 1	TIOA1_0	Base timer ch.1 TIOA pin	33	28	-
	TIOA1_1		25	20	15
	TIOA1_2		5	5	5
	TIOB1_0	Base timer ch.1 TIOB pin	48	43	33
	TIOB1_1		15	10	10
	TIOB1_2		6	6	6
Base Timer 2	TIOA2_0	Base timer ch.2 TIOA pin	34	29	-
	TIOA2_1		26	21	16
	TIOA2_2		116	96	76
	TIOB2_0	Base timer ch.2 TIOB pin	49	44	34
	TIOB2_1		16	11	11
	TIOB2_2		115	95	75
Base Timer 3	TIOA3_0	Base timer ch.3 TIOA pin	35	30	-
	TIOA3_1		27	22	17
	TIOA3_2		105	90	70
	TIOB3_0	Base timer ch.3 TIOB pin	50	45	35
	TIOB3_1		17	12	12
	TIOB3_2		106	91	71
Base Timer 4	TIOA4_0	Base timer ch.4 TIOA pin	36	31	21
	TIOA4_1		28	23	18
	TIOA4_2		51	-	-
	TIOB4_0	Base timer ch.4 TIOB pin	23	18	13
	TIOB4_1		18	13	-
	TIOB4_2		52	-	-
Base Timer 5	TIOA5_0	Base timer ch.5 TIOA pin	37	32	22
	TIOA5_1		29	24	19
	TIOA5_2		97	82	-
	TIOB5_0	Base timer ch.5 TIOB pin	94	79	63
	TIOB5_1		19	14	-
	TIOB5_2		98	83	-
Base Timer 6	TIOA6_0	Base timer ch.6 TIOA pin	53	-	-
	TIOA6_1		114	94	74
	TIOA6_2		82	-	-
	TIOB6_0	Base timer ch.6 TIOB pin	54	-	-
	TIOB6_1		113	93	73
	TIOB6_2		81	-	-
Base Timer 7	TIOA7_0	Base timer ch.7 TIOA pin	112	-	-
	TIOA7_1		86	71	58
	TIOA7_2		109	-	-
	TIOB7_0	Base timer ch.7 TIOB pin	111	-	-
	TIOB7_1		87	72	59
	TIOB7_2		108	-	-
Debugger	SWCLK	Serial wire debug interface clock input pin	93	78	62
	SWDIO	Serial wire debug interface data input / output pin	95	80	64

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
External Interrupt	INT00_0	External interrupt request 00 input pin	2	2	2
	INT00_1		97	82	-
	INT00_2		102	87	67
	INT01_0	External interrupt request 01 input pin	3	3	3
	INT01_1		98	83	-
	INT02_0	External interrupt request 02 input pin	4	4	4
	INT02_1		63	53	43
	INT02_2		82	-	-
	INT03_0	External interrupt request 03 input pin	113	93	73
	INT03_1		66	56	46
	INT03_2		14	9	9
	INT04_0	External interrupt request 04 input pin	17	12	12
	INT04_1		69	59	49
	INT04_2		15	10	10
	INT05_0	External interrupt request 05 input pin	89	74	-
	INT05_1		76	66	56
	INT05_2		16	11	11
	INT06_0	External interrupt request 06 input pin	23	18	13
	INT06_1		88	73	60
	INT06_2		96	81	65
	INT07_0	External interrupt request 07 input pin	24	19	14
	INT07_1		114	94	74
	INT07_2		5	5	5
	INT08_0	External interrupt request 08 input pin	34	29	-
	INT08_1		19	14	-
	INT08_2		8	8	8
	INT09_0	External interrupt request 09 input pin	35	30	-
	INT09_1		20	15	-
	INT10_0	External interrupt request 10 input pin	36	31	21
	INT10_1		21	16	-
	INT10_2		112	-	-
	INT11_0	External interrupt request 11 input pin	118	98	78
	INT11_1		22	17	-
	INT11_2		110	-	-
	INT12_0	External interrupt request 12 input pin	49	44	34
	INT12_1		32	27	-
	INT12_2		108	-	-
	INT13_0	External interrupt request 13 input pin	50	45	35
	INT13_1		33	28	-
	INT13_2		52	-	-
	INT14_0	External interrupt request 14 input pin	67	57	47
	INT14_1		92	77	61
	INT14_2		53	-	-

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
GND	VSS	GND pin	30	25	20
			39	34	24
			60	50	40
			90	75	-
			120	100	80
Clock	X0	Main clock (oscillation) input pin	58	48	38
	X0A	Sub clock (oscillation) input pin	42	37	27
	X1	Main clock (oscillation) I/O pin	59	49	39
	X1A	Sub clock (oscillation) I/O pin	43	38	28
	CROUT_0	Built-in high-speed CR oscillation clock output port	89	74	-
	CROUT_1	Built-in high-speed CR oscillation clock output port	107	92	72
Analog Power	AVCC	A/D converter analog power supply pin	70	60	50
	AVRH	A/D converter analog reference voltage input pin	73	63	53
Analog GND	AVSS	A/D converter analog reference voltage input pin	71	61	51
C pin	C	Power supply stabilization capacitance pin	38	33	23

*: PE0 is an open drain pin, cannot output high.

Type	Circuit	Remarks
F		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 33 kΩ • $I_{OH} = -4 \text{ mA}$, $I_{OL} = 4 \text{ mA}$ • When this pin is used as an I²C pin, the digital output P-ch transistor is always off
G		• CMOS level output • CMOS level hysteresis input • With input control • Analog input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 33 kΩ • $I_{OH} = -4 \text{ mA}$, $I_{OL} = 4 \text{ mA}$ • When this pin is used as an I²C pin, the digital output P-ch transistor is always off

Latch-Up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNP junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

- (1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
- (2) Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Spanion semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

6.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Spanion's recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Spanion recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

List of Pin Status

Pin Status Type	Function Group	State Upon Power-on Reset or Low-Voltage Detection	State at INITX Input	State Upon Device Internal Reset	State in Run Mode or Sleep Mode	State in Timer Mode, RTC Mode, or Stop Mode		State in Deep Standby RTC Mode or Deep Standby Stop Mode State		State when Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable	Power Supply Stable	Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
A	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Main crystal oscillator input pin/ External main clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
B	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	External main clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	Maintain previous state	Hi-Z / Internal input fixed at 0	Maintain previous state
	Main crystal oscillator output pin	Hi-Z / Internal input fixed at 0/ Input enabled	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Maintain previous state/When oscillation stops* ¹ , Hi-Z / Internal input fixed at 0	Maintain previous state/When oscillation stops* ¹ , Hi-Z / Internal input fixed at 0	Maintain previous state/When oscillation stops* ¹ , Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops* ¹ , Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops* ¹ , Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops* ¹ , Hi-Z / Internal input fixed at 0
C	INITX input pin	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled

Pin Status Type	Function Group	State Upon Power-on Reset or Low-Voltage Detection	State at INITX Input	State Upon Device Internal Reset	State in Run Mode or Sleep Mode	State in Timer Mode, RTC Mode, or Stop Mode		State in Deep Standby RTC Mode or Deep Standby Stop Mode State		State when Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable	Power Supply Stable	Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
E	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	Input enabled	Input enabled	Input enabled
	Sub crystal oscillator input pin / External sub clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	GPIO selected	Hi-Z / Input enabled	GPIO selected
F	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	External sub clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	Maintain previous state	Hi-Z / Internal input fixed at 0	Maintain previous state
	Sub crystal oscillator output pin	Hi-Z / Internal input fixed at 0/ Input enabled	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Maintain previous state	Maintain previous state/When oscillation stops*2, Hi-Z / Internal input fixed at 0	Maintain previous state/When oscillation stops*2, Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops*2, Hi-Z/ Internal input fixed at 0	Maintain previous state / When oscillation stops*2, Hi-Z/ Internal input fixed at 0	Maintain previous state / When oscillation stops*2, Hi-Z/ Internal input fixed at 0
G	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	Resource other than the above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected									

LVD Current

 (V_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Typ	Max		
Low-Voltage detection circuit (LVD) power supply current	I _{CC} LVD	VCC	At operation	0.13	TBD	μA	For occurrence of reset
				0.13	TBD	μA	For occurrence of interrupt

Flash Memory Current

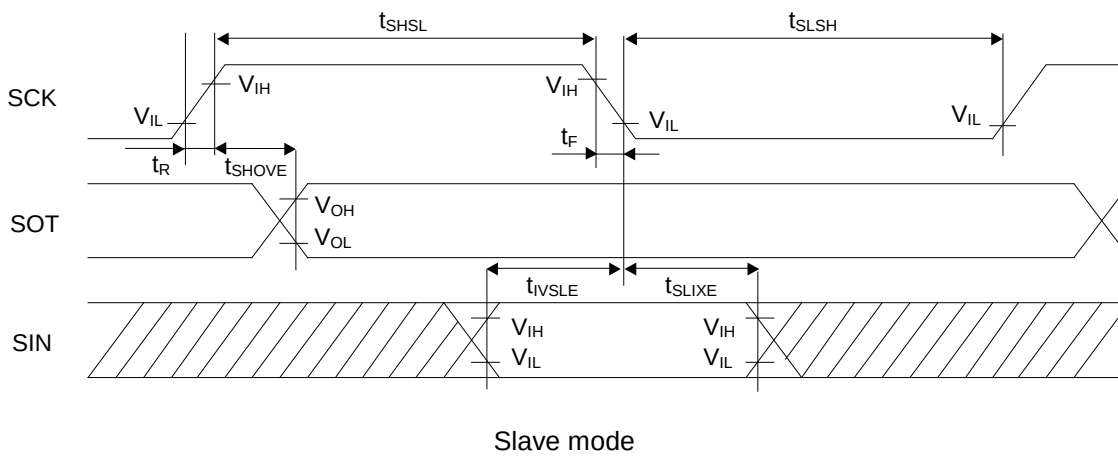
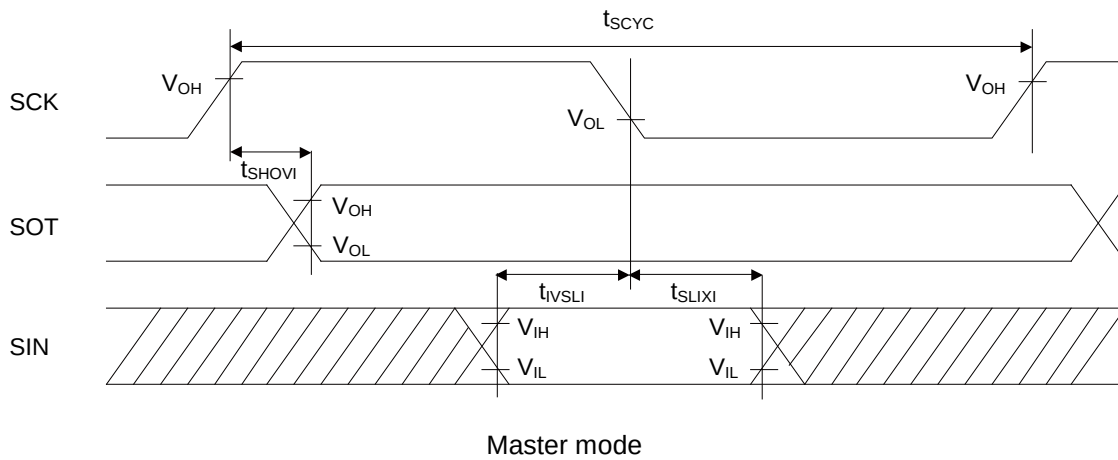
 (V_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

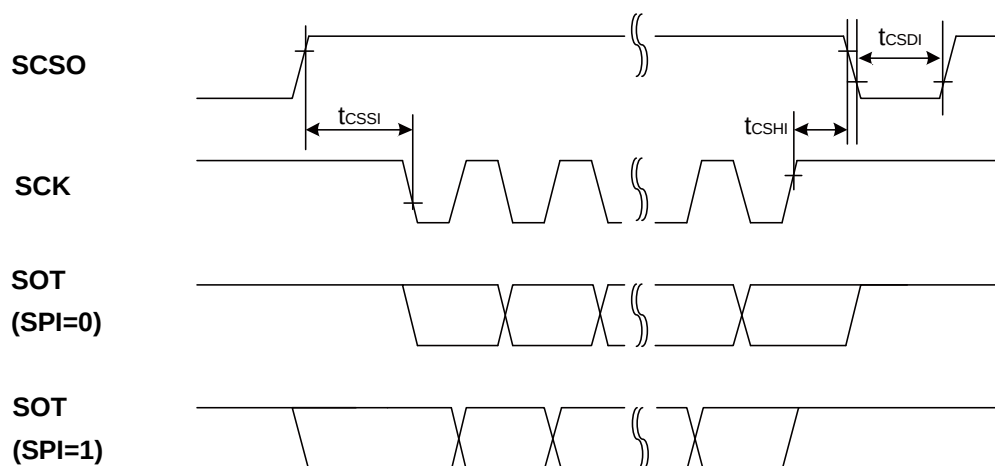
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Typ	Max		
Flash memory write/erase current	I _{CC} FLASH	VCC	At Write/Erase	9.5	TBD	mA	

A/D converter Current

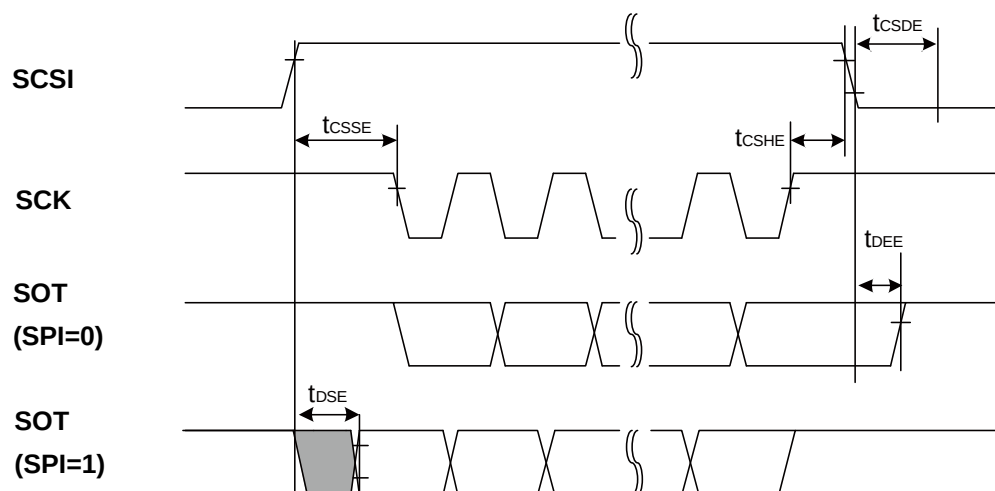
 (V_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Typ	Max		
Power supply current	I _{CC} AD	AVCC	At operation	0.7	TBD	mA	
			At stop	0.13	TBD	μA	
Reference power supply current (AVRH)	I _{CC} AVRH	AVRH	At operation	1.1	TBD	mA	AVRH=3.6 V
			At stop	0.1	TBD	μA	





Master mode

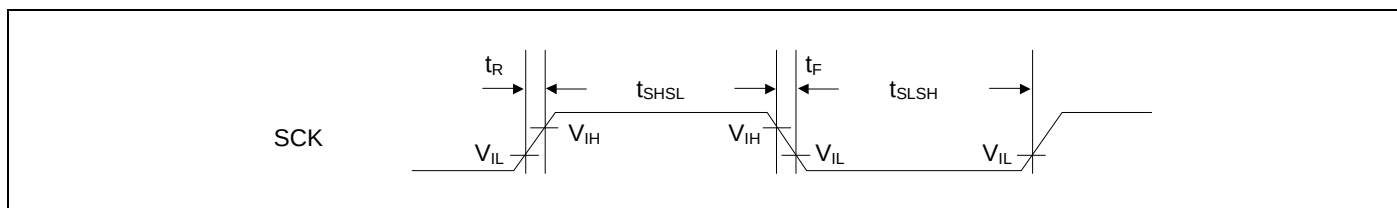


Slave mode

UART external clock input (EXT=1)

 ($V_{CC}=AV_{CC}=1.65\text{ V to }3.6\text{ V}$, $V_{SS}=AV_{SS}=0\text{ V}$, $T_A=-40^{\circ}\text{C to }+105^{\circ}\text{C}$)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Serial clock L pulse width	t_{SLSH}	$C_L=30\text{ pF}$	$t_{CYCP} +10$	-	ns	
Serial clock H pulse width	t_{SHSL}		$t_{CYCP} +10$	-	ns	
SCK falling time	t_F		-	5	ns	
SCK rising time	t_R		-	5	ns	

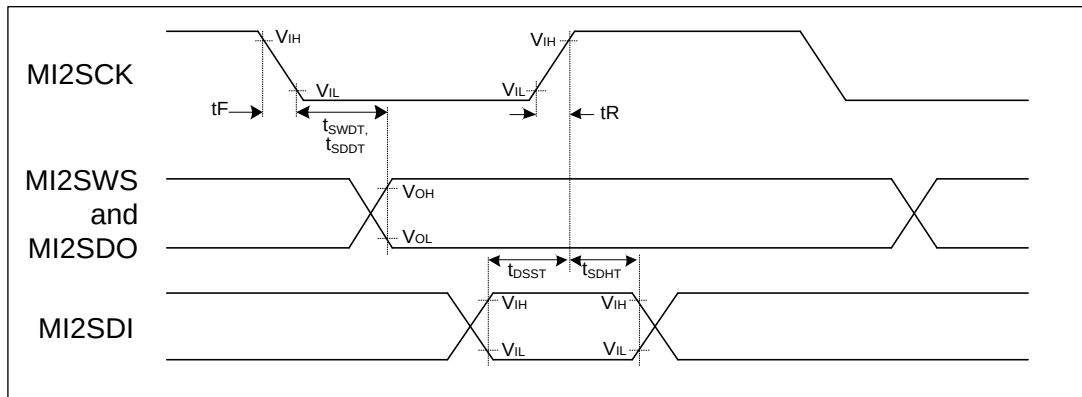


11.4.12 I²S Timing

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	V _{CC} < 2.7 V		V _{CC} ≥ 2.7 V		Unit
				Min	Max	Min	Max	
MI2SCK max frequency (*1)	F _{MI2SCK}	MI2SCKx	C _L =30 pF	-	6.144	-	6.144	MHz
I ² S clock cycle time (*1)	t _{ICYC}	MI2SCKx		4 t _{CYCP}	-	4 t _{CYCP}	-	ns
I ² S clock Duty cycle	Δ	MI2SCKx		45%	55%	45%	55%	
MI2SCK ↓ → MI2SWS delay time	t _{SWDT}	MI2SCKx, MI2SWSx		-30	+30	-20	+20	ns
MI2SCK ↓ → MI2SDO delay time	t _{SDDT}	MI2SCKx, MI2SDOx		-30	+30	-20	+20	ns
MI2SDI → MI2SCK ↑ setup time	t _{DSST}	MI2SCKx, MI2SDIx		50	-	36	-	ns
MI2SCK ↑ → MI2SDI hold time	t _{SDHT}	MI2SCKx, MI2SDIx		0	-	0	-	ns
MI2SCK falling time	t _F	MI2SCKx		-	5	-	5	ns
MI2SCK rising time	t _R	MI2SCKx		-	5	-	5	ns

*1: I²S clock should meet the multiple of PCLK(t_{ICYC}) and the frequency less than F_{MI2SCK} meantime. The detail information please refer to Chapter I²S of Communication Macro Part of Peripheral Manual.



11.8 Flash Memory Write/Erase Characteristics

 (V_{CC}=1.65 V to 3.6 V, T_A=- 40°C to +105°C)

Parameter		Value			Unit	Remarks
		Min	Typ*	Max*		
Sector erase time	Large sector	-	1.1	2.7	s	The sector erase time includes the time of writing prior to internal erase.
	Small sector	-	0.3	0.9		
Halfword (16-bit) write time		-	30	528	μs	The halfword (16-bit) write time excludes the system-level overhead.
Chip erase time		-	11.2	28.8	s	The chip erase time includes the time of writing prior to internal erase.

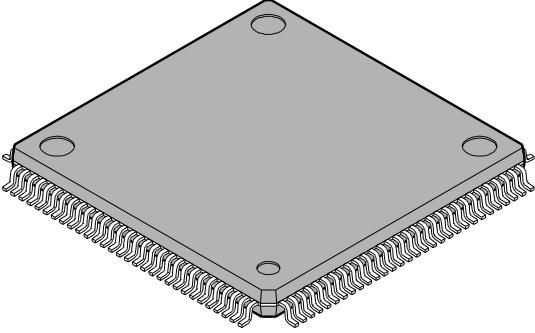
*: The typical value is immediately after shipment, the maximum value is guarantee value under 10,000 cycle of erase/write.

Write/Erase Cycle and Data Hold Time (Target Value)

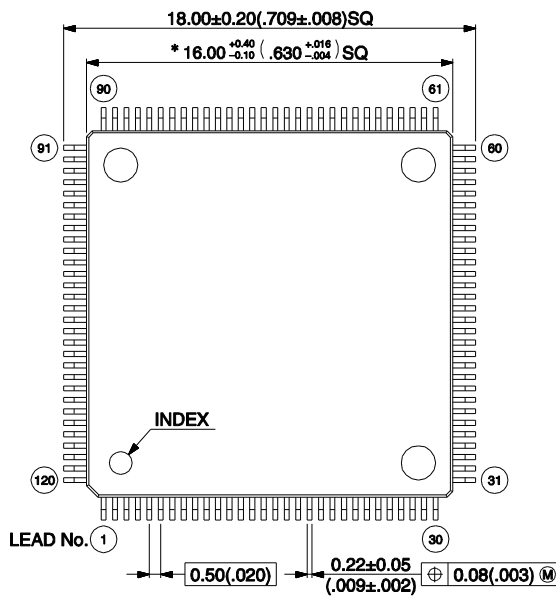
Write/Erase Cycle	Data Hold Time (Year)	Remarks
1,000	20*	
10,000	10*	

*: At average + 85°C

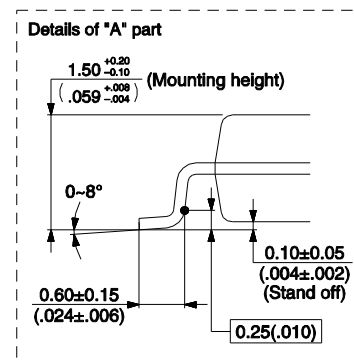
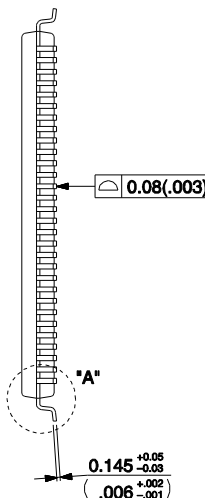
13. Package Dimensions

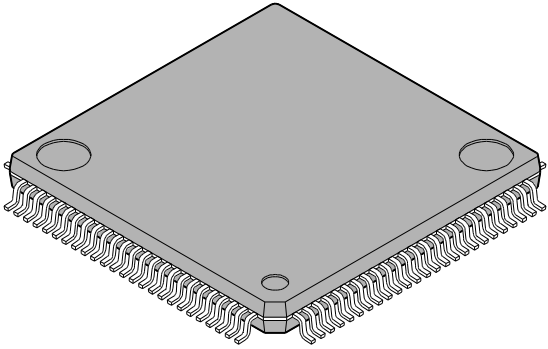
 120-pin plastic LQFP (FPT-120P-M21)	Lead pitch	0.50 mm
	Package width × package length	16.0 × 16.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.88 g
	Code (Reference)	P-LFQFP120-16×16-0.50

120-pin plastic LQFP
(FPT-120P-M21)



- Note 1) * : These dimensions do not include resin protrusion.
Resin protrusion is +0.25(.010) MAX(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



100-pin plastic LQFP  (FPT-100P-M20)	Lead pitch	0.50 mm
	Package width × package length	14.0 mm × 14.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.65 g
	Code (Reference)	P-LFQFP100-14×14-0.50

