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Details

Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	48 MIPS
Connectivity	I ² C, SPI, UART/USART, USB
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	25
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.25V
Data Converters	A/D 21x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051t320-gq

C8051T620/1/6/7 & C8051T320/1/2/3

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C8051T620/1/6/7 & C8051T320/1/2/3

1. System Overview

C8051T620/1/6/7 & C8051T320/1/2/3 devices are fully integrated mixed-signal System-on-a-Chip MCUs. Highlighted features are listed below. Refer to Table 2.1 for specific product feature selection and part ordering numbers.

- High-speed pipelined 8051-compatible microcontroller core (up to 48 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- C8051F34A ISP Flash device is available for quick in-system code development
- Universal Serial Bus (USB) Function Controller with eight flexible endpoint pipes, integrated transceiver, and 1 kB FIFO RAM
- Supply Voltage Regulator
- 10-bit 500 ksp/s Single-ended ADC with analog multiplexer and integrated temperature sensor
- Precision calibrated 48 MHz internal oscillator
- Internal low-frequency oscillator for additional power savings
- 64, 32, or 16 kB of on-chip byte-programmable EPROM—(512 bytes are reserved)
- 1280 or 3328 bytes of on-chip RAM (256 + 1 kB or 3 kB)
- SMBus/I²C, 2 UARTs, and Enhanced SPI serial interfaces implemented in hardware
- Four general-purpose 16-bit timers
- Programmable Counter/Timer Array (PCA) with five capture/compare modules and Watchdog Timer function
- On-chip Power-On Reset, V_{DD} Monitor, and Temperature Sensor
- On-chip Voltage Comparators (2)
- Up to 25 Port I/O

With on-chip Power-On Reset, V_{DD} monitor, Watchdog Timer, and clock oscillator, the C8051T620/1/6/7 & C8051T320/1/2/3 devices are truly stand-alone System-on-a-Chip solutions. User software has complete control of all peripherals, and may individually shut down any or all peripherals for power savings.

Code written for the C8051T620/1/6/7 & C8051T320/1/2/3 family of processors will run on the C8051F34A Mixed-signal ISP Flash microcontroller, providing a quick, cost-effective way to develop code without requiring special emulator circuitry. The C8051T620/1/6/7 & C8051T320/1/2/3 processors include Silicon Laboratories' 2-Wire C2 Debug and Programming interface, which allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection of memory, viewing and modification of special function registers, setting breakpoints, single stepping, run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system debugging without occupying package pins.

Each device is specified for 1.8-to-5.25 V operation over the industrial temperature range (–40 to +85 °C). For voltages above 3.6 V, the on-chip Voltage Regulator must be used. A minimum of 3.0 V is required for USB communication. An additional internal LDO is used to supply the processor core voltage at 1.8 V. The Port I/O and $\overline{\text{RST}}$ pins are tolerant of input signals up to 5 V. The C8051T620/1/6/7 are available in 32-pin QFN packaging, the C8051T320/2 are available in 32-pin LQFP packaging, and the C8051T321/3 are available in 28-pin QFN packaging. See Table 2.1 for ordering information. A block diagram is shown in Figure 1.1.

C8051T620/1/6/7 & C8051T320/1/2/3

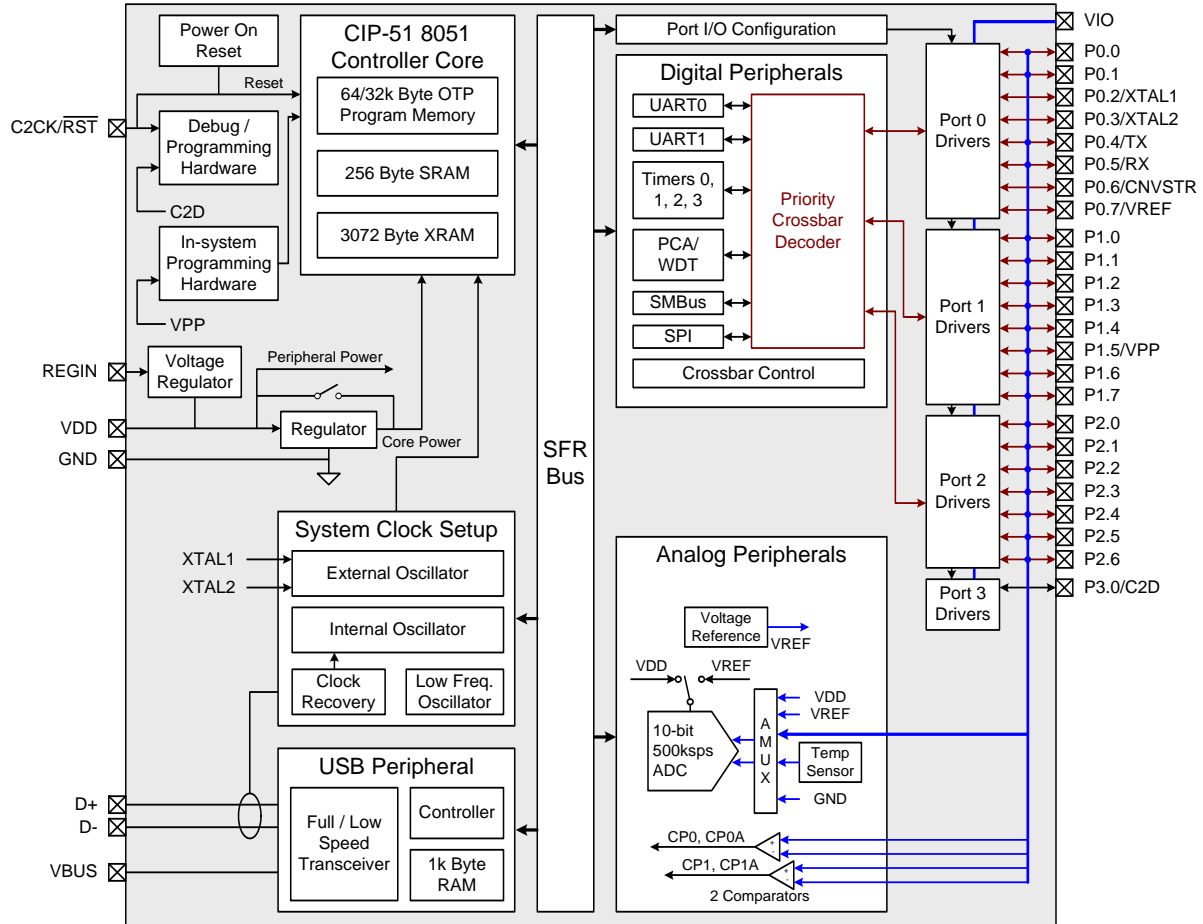


Figure 1.2. C8051T626/7 Block Diagram

C8051T620/1/6/7 & C8051T320/1/2/3

7.2. Electrical Characteristics

Table 7.2. Global Electrical Characteristics

–40 to +85 °C, 25 MHz system clock unless otherwise specified.

Parameters	Test Condition	Min	Typ	Max	Unit
Supply Voltage (Note 1)	Regulator1 in Normal Mode Regulator1 in Bypass Mode	1.8 1.75	3.0 —	3.6 1.9	V V
Digital Supply Current with CPU Active	$V_{DD} = 1.8$ V, Clock = 48 MHz	—	9.4	11.4	mA
	$V_{DD} = 1.8$ V, Clock = 1 MHz	—	1.6	—	mA
	$V_{DD} = 3.3$ V, Clock = 48 MHz	—	11.0	13.7	mA
	$V_{DD} = 3.3$ V, Clock = 1 MHz	—	1.7	—	mA
	$V_{DD} = 3.6$ V, Clock = 48 MHz	—	11.1	13.8	mA
	$V_{DD} = 3.6$ V, Clock = 1 MHz	—	1.8	—	mA
Digital Supply Current with CPU Inactive (not accessing EPROM)	$V_{DD} = 1.8$ V, Clock = 48 MHz	—	4.6	5.5	mA
	$V_{DD} = 1.8$ V, Clock = 1 MHz	—	0.4	—	mA
	$V_{DD} = 3.3$ V, Clock = 48 MHz	—	5.1	5.9	mA
	$V_{DD} = 3.3$ V, Clock = 1 MHz	—	0.45	—	mA
	$V_{DD} = 3.6$ V, Clock = 48 MHz	—	5.1	6.0	mA
	$V_{DD} = 3.6$ V, Clock = 1 MHz	—	0.5	—	mA
Digital Supply Current (shutdown)	Oscillator not running (stop mode), Internal Regulator Off	—	.1	—	μA
	Oscillator not running (stop or suspend mode), Internal Regulator On	—	375	—	μA
Digital Supply Current for USB Module (USB Active Mode)	$V_{DD} = 3.6$ V, USB Clock = 48 MHz	—	11.8	—	mA
	$V_{DD} = 3.3$ V, USB Clock = 48 MHz	—	11.4	—	mA
Digital Supply Current for USB Module (USB Suspend Mode)	Oscillator not running; V_{DD} monitor disabled. C8051T620/1/T320/1/2/3 C8051T626/7	—	60	—	μA
		—	90	—	μA
		—	—	—	—
Digital Supply RAM Data Retention Voltage		—	1.5	—	V
Specified Operating Temperature Range		–40	—	+85	°C
SYSCLK (System Clock) (Note 2)		0	—	48	MHz
Tsysl (SYSCLK low time)		9.75	—	—	ns
Tsysh (SYSCLK high time)		9.75	—	—	ns
Notes: 1. Analog performance is not guaranteed when V_{DD} is below 1.8 V. 2. SYSCLK must be at least 32 kHz to enable debugging.					

C8051T620/1/6/7 & C8051T320/1/2/3

7.3. Typical Performance Curves

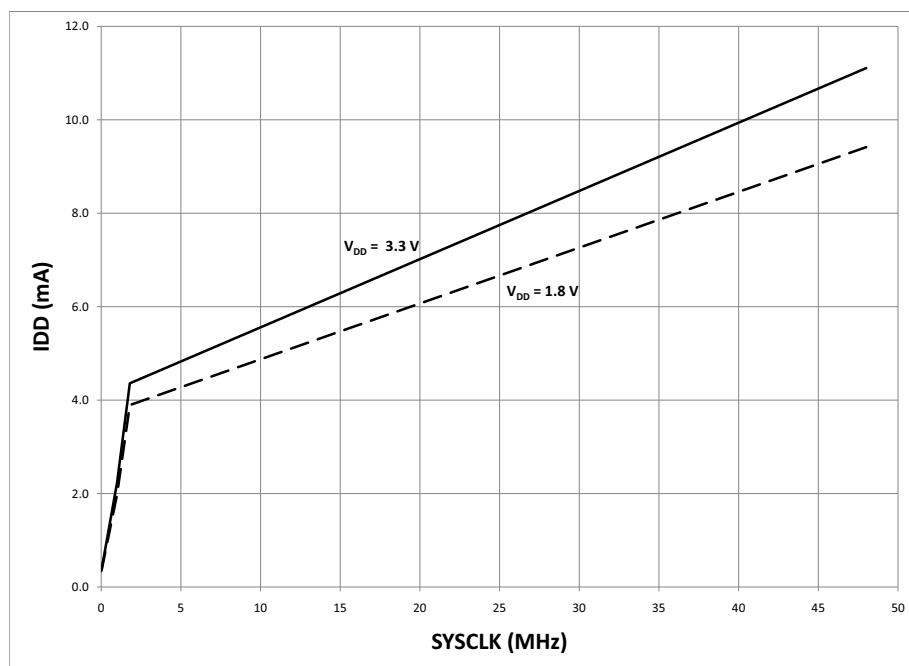


Figure 7.1. Normal Mode Digital Supply Current vs. Frequency (MPCE = 1)

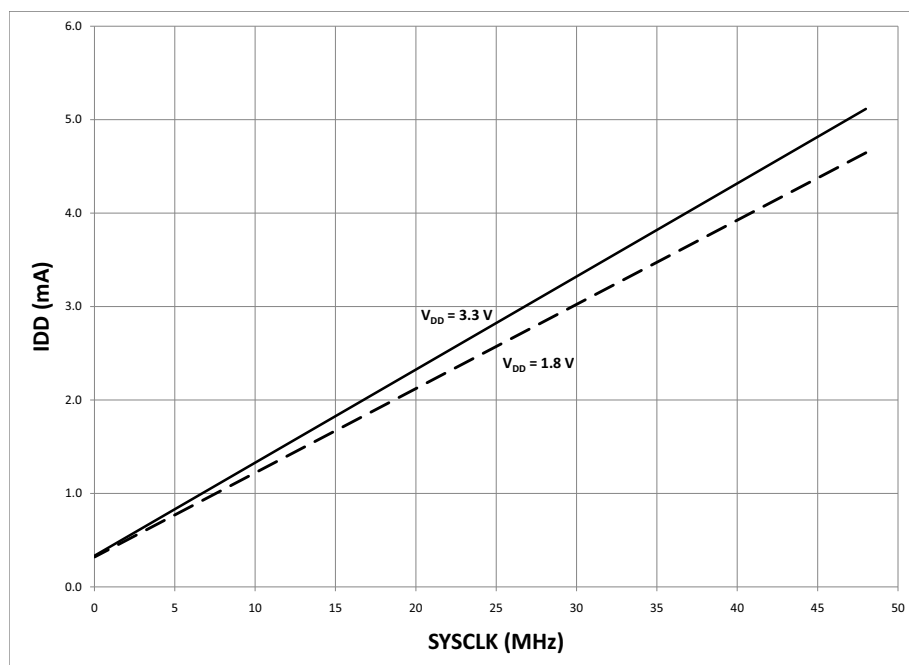


Figure 7.2. Idle Mode Digital Supply Current vs. Frequency (MPCE = 1)

C8051T620/1/6/7 & C8051T320/1/2/3

SFR Definition 8.1. ADC0CF: ADC0 Configuration

Bit	7	6	5	4	3	2	1	0
Name	AD0SC[4:0]					AD0LJST	AD08BE	AMP0GN0
Type	R/W					R/W	R/W	R/W
Reset	1	1	1	1	1	0	0	1

SFR Address = 0xBC

Bit	Name	Function
7:3	AD0SC[4:0]	ADC0 SAR Conversion Clock Period Bits. SAR Conversion clock is derived from system clock by the following equation, where <i>AD0SC</i> refers to the 5-bit value held in bits AD0SC4–0. SAR Conversion clock requirements are given in the ADC specification table. $AD0SC = \frac{SYSCLK}{CLK_{SAR}} - 1$ Note: If the Memory Power Controller is enabled (MPCE = '1'), AD0SC must be set to at least "00001" for proper ADC operation.
2	AD0LJST	ADC0 Left Justify Select. 0: Data in ADC0H:ADC0L registers are right-justified. 1: Data in ADC0H:ADC0L registers are left-justified. Note: The AD0LJST bit is only valid for 10-bit mode (AD08BE = 0).
1	AD08BE	8-Bit Mode Enable. 0: ADC operates in 10-bit mode (normal). 1: ADC operates in 8-bit mode. Note: When AD08BE is set to 1, the AD0LJST bit is ignored.
0	AMP0GN0	ADC Gain Control Bit. 0: Gain = 0.5 1: Gain = 1

11. Voltage Regulators (REG0 and REG1)

C8051T620/1/6/7 & C8051T320/1/2/3 devices include two internal voltage regulators: one regulates a voltage source on RGIN to 3.45 V (REG0), and the other regulates the internal core supply to 1.8 V from a V_{DD} supply of 1.8 to 3.6 V (REG1). When enabled, the REG0 output appears on the V_{DD} pin and can be used to power external devices. REG0 can be enabled/disabled by software using bit REG0DIS in register REG01CN (SFR Definition 11.1). REG1 has two power-saving modes built into the regulator to help reduce current consumption in low-power applications. These modes are accessed through the REG01CN register. Electrical characteristics for the on-chip regulators are specified in Table 7.5 on page 37.

Note that the VBUS signal must be connected to the VBUS pin when using the device in a USB network. The VBUS signal should only be connected to the RGIN pin when operating the device as a bus-powered function. REG0 configuration options are shown in Figure 11.1–Figure 11.4.

11.1. Voltage Regulator (REG0)

11.1.1. Regulator Mode Selection

REG0 offers a low power mode intended for use when the device is in suspend mode. In this low power mode, the REG0 output remains as specified; however the REG0 dynamic performance (response time) is degraded. See Table 7.5 for normal and low power mode supply current specifications. The REG0 mode selection is controlled via the REG0MD bit in register REG01CN.

11.1.2. VBUS Detection

When the USB Function Controller is used (see section Section “23. Universal Serial Bus Controller (USB0)” on page 160), the VBUS signal should be connected to the VBUS pin. The VBSTAT bit (register REG01CN) indicates the current logic level of the VBUS signal. If enabled, a VBUS interrupt will be generated when the VBUS signal has either a falling or rising edge. The VBUS interrupt is edge-sensitive, and has no associated interrupt pending flag. See Table 7.5 for VBUS input parameters.

Important Note: When USB is selected as a reset source, a system reset will be generated when a falling or rising edge occurs on the VBUS pin. See Section “20. Reset Sources” on page 121 for details on selecting USB as a reset source.

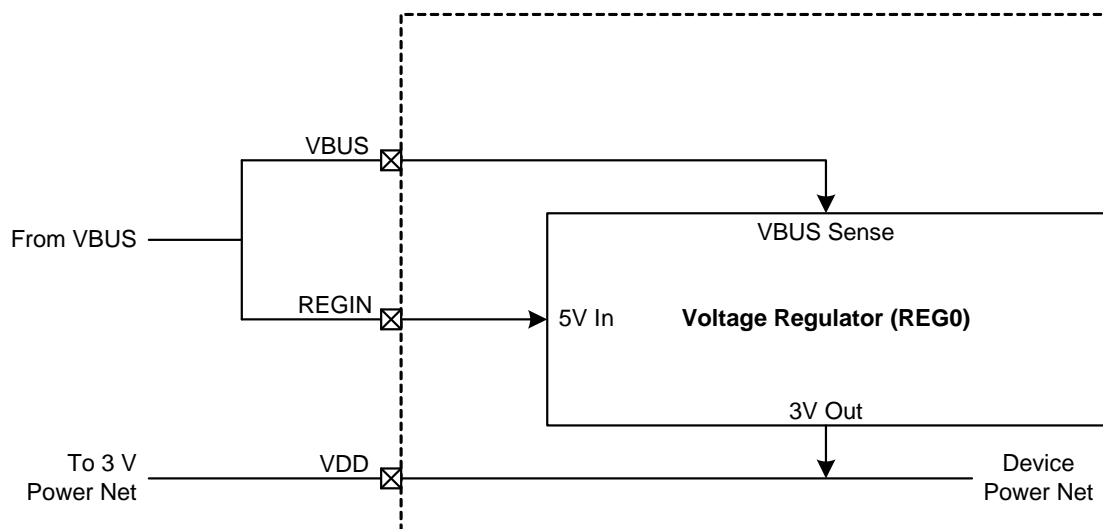


Figure 11.1. REG0 Configuration: USB Bus-Powered

19. Power Management Modes

The C8051T620/1/6/7 & C8051T320/1/2/3 devices have three software programmable power management modes: Idle, Stop, and Suspend. Idle mode and stop mode are part of the standard 8051 architecture, while suspend mode is an enhanced power-saving mode implemented by the high-speed oscillator peripheral.

Idle mode halts the CPU while leaving the peripherals and clocks active. In stop mode, the CPU is halted, all interrupts and timers (except the Missing Clock Detector) are inactive, and the internal oscillator is stopped (analog peripherals remain in their selected states; the external oscillator is not affected). Suspend mode is similar to stop mode in that the internal oscillator is halted, but the device can wake on events such as a Port Mismatch, Timer 3 overflow, or activity with the USB transceiver. Additionally, the CPU is not halted in suspend mode, so it can run on another oscillator, if desired. Since clocks are running in Idle mode, power consumption is dependent upon the system clock frequency and the number of peripherals left in active mode before entering Idle. Stop mode and suspend mode consume the least power because the majority of the device is shut down with no clocks active. SFR Definition 19.1 describes the Power Control Register (PCON) used to control the C8051T620/1/6/7 & C8051T320/1/2/3's Stop and Idle power management modes. Suspend mode is controlled by the SUSPEND bit in the OSCICN register (SFR Definition 21.3).

Although the C8051T620/1/6/7 & C8051T320/1/2/3 has Idle, Stop, and suspend modes available, more control over the device power can be achieved by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers or serial buses, draw little power when they are not in use. Turning off oscillators lowers power consumption considerably, at the expense of reduced functionality.

19.1. Idle Mode

Setting the Idle Mode Select bit (PCON.0) causes the hardware to halt the CPU and enter Idle mode as soon as the instruction that sets the bit completes execution. All internal registers and memory maintain their original data. All analog and digital peripherals can remain active during idle mode.

Idle mode is terminated when an enabled interrupt is asserted or a reset occurs. The assertion of an enabled interrupt will cause the Idle Mode Selection bit (PCON.0) to be cleared and the CPU to resume operation. The pending interrupt will be serviced and the next instruction to be executed after the return from interrupt (RETI) will be the instruction immediately following the one that set the Idle Mode Select bit. If Idle mode is terminated by an internal or external reset, the CIP-51 performs a normal reset sequence and begins program execution at address 0x0000.

Note: If the instruction following the write of the IDLE bit is a single-byte instruction and an interrupt occurs during the execution phase of the instruction that sets the IDLE bit, the CPU may not wake from Idle mode when a future interrupt occurs. Therefore, instructions that set the IDLE bit should be followed by an instruction that has two or more opcode bytes, for example:

```
// in 'C':
PCON |= 0x01;           // set IDLE bit
PCON = PCON;           // ... followed by a 3-cycle dummy instruction

; in assembly:
ORL PCON, #01h          ; set IDLE bit
MOV PCON, PCON          ; ... followed by a 3-cycle dummy instruction
```

If enabled, the Watchdog Timer (WDT) will eventually cause an internal watchdog reset and thereby terminate the Idle mode. This feature protects the system from an unintended permanent shutdown in the event of an inadvertent write to the PCON register. If this behavior is not desired, the WDT may be disabled by software prior to entering the Idle mode if the WDT was initially configured to allow this operation. This pro-

C8051T620/1/6/7 & C8051T320/1/2/3

SFR Definition 19.1. PCON: Power Control

Bit	7	6	5	4	3	2	1	0
Name	GF[5:0]						STOP	IDLE
Type	R/W						R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x87

Bit	Name	Function
7:2	GF[5:0]	General Purpose Flags 5–0. These are general purpose flags for use under software control.
1	STOP	Stop Mode Select. Setting this bit will place the CIP-51 in stop mode. This bit will always be read as 0. 1: CPU goes into stop mode (internal oscillator stopped).
0	IDLE	IDLE: Idle Mode Select. Setting this bit will place the CIP-51 in Idle mode. This bit will always be read as 0. 1: CPU goes into Idle mode. (Shuts off clock to CPU, but clock to Timers, Interrupts, Serial Ports, and Analog Peripherals are still active.)

C8051T620/1/6/7 & C8051T320/1/2/3

22.1. Port I/O Modes of Operation

Port pins use the Port I/O cell shown in Figure 22.2. Each Port I/O cell can be configured by software for analog I/O or digital I/O using the PnMDIN registers. On reset, all Port I/O cells default to a high impedance state with weak pull-ups enabled until the Crossbar is enabled (XBARE = 1).

22.1.1. Port Pins Configured for Analog I/O

Any pins to be used as Comparator or ADC input, external oscillator input/output, or VREF should be configured for analog I/O (PnMDIN.n = 1). When a pin is configured for analog I/O, its weak pullup, digital driver, and digital receiver are disabled. Port pins configured for analog I/O will always read back a value of 0.

Configuring pins as analog I/O saves power and isolates the Port pin from digital interference. Port pins configured as digital inputs may still be used by analog peripherals; however, this practice is not recommended and may result in measurement errors.

22.1.2. Port Pins Configured For Digital I/O

Any pins to be used by digital peripherals (UART, SPI, SMBus, etc.), external digital event capture functions, or as GPIO should be configured as digital I/O (PnMDIN.n = 1). For digital I/O pins, one of two output modes (push-pull or open-drain) must be selected using the PnMDOUT registers.

Push-pull outputs (PnMDOUT.n = 1) drive the Port pad to the V_{IO} or GND supply rails based on the output logic value of the Port pin. Open-drain outputs have the high side driver disabled; therefore, they only drive the Port pad to GND when the output logic value is 0 and become high impedance inputs (both high and low drivers turned off) when the output logic value is 1.

When a digital I/O cell is placed in the high impedance state, a weak pull-up transistor pulls the Port pad to the V_{DD} supply voltage to ensure the digital input is at a defined logic state. Weak pull-ups are disabled when the I/O cell is driven to GND to minimize power consumption and may be globally disabled by setting WEAKPUD to 1. The user should ensure that digital I/O are always internally or externally pulled or driven to a valid logic state to minimize power consumption. Port pins configured for digital I/O always read back the logic state of the Port pad, regardless of the output logic value of the Port pin.

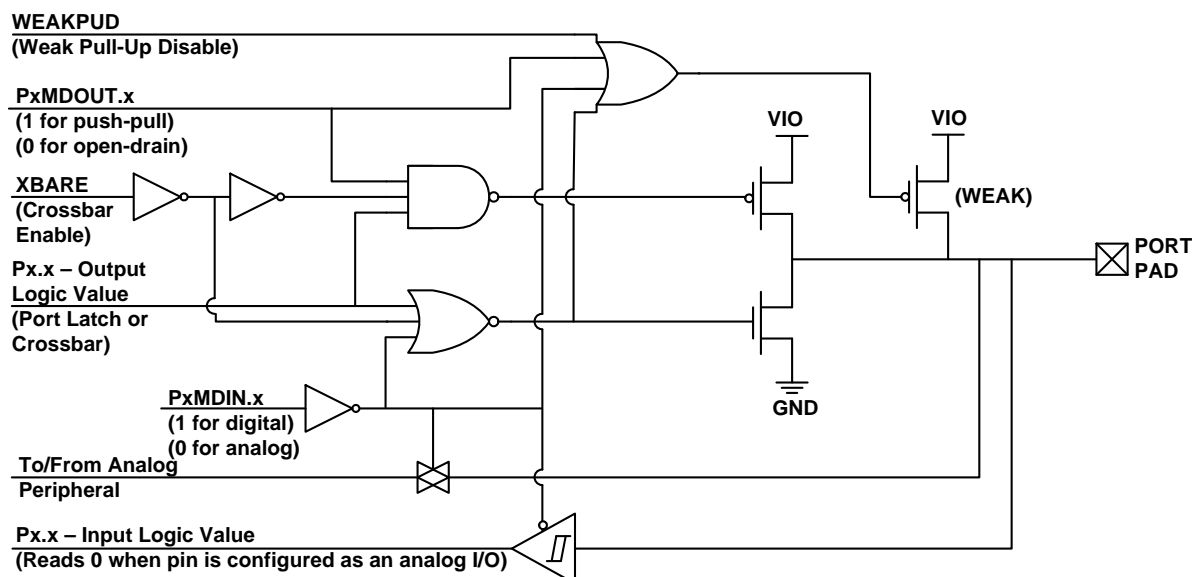


Figure 22.2. Port I/O Cell Block Diagram

C8051T620/1/6/7 & C8051T320/1/2/3

Table 23.2. USB0 Controller Registers

USB Register Name	USB Register Address	Description	Page Number
Interrupt Registers			
IN1INT	0x02	Endpoint0 and Endpoints1-3 IN Interrupt Flags	176
OUT1INT	0x04	Endpoints1-3 OUT Interrupt Flags	177
CMINT	0x06	Common USB Interrupt Flags	178
IN1IE	0x07	Endpoint0 and Endpoints1-3 IN Interrupt Enables	179
OUT1IE	0x09	Endpoints1-3 OUT Interrupt Enables	180
CMIE	0x0B	Common USB Interrupt Enables	181
Common Registers			
FADDR	0x00	Function Address	172
POWER	0x01	Power Management	174
FRAMEL	0x0C	Frame Number Low Byte	175
FRAMEH	0x0D	Frame Number High Byte	175
INDEX	0x0E	Endpoint Index Selection	167
CLKREC	0x0F	Clock Recovery Control	168
EENABLE	0x1E	Endpoint Enable	186
FIFOn	0x20-0x23	Endpoints0-3 FIFOs	171
Indexed Registers			
E0CSR	0x11	Endpoint0 Control / Status	184
EINCSRL		Endpoint IN Control / Status Low Byte	188
EINCSRH	0x12	Endpoint IN Control / Status High Byte	189
EOUTCSRL	0x14	Endpoint OUT Control / Status Low Byte	191
EOUTCSRH	0x15	Endpoint OUT Control / Status High Byte	192
E0CNT	0x16	Number of Received Bytes in Endpoint0 FIFO	185
EOUTCNTL		Endpoint OUT Packet Count Low Byte	192
EOUTCNTH	0x17	Endpoint OUT Packet Count High Byte	193

C8051T620/1/6/7 & C8051T320/1/2/3

23.4. USB Clock Configuration

USB0 is capable of communication as a Full or Low Speed USB function. Communication speed is selected via the SPEED bit in SFR USB0XCN. When operating as a Low Speed function, the USB0 clock must be 6 MHz. When operating as a Full Speed function, the USB0 clock must be 48 MHz. Clock options are described in Section “21. Oscillators and Clock Selection” on page 127. The USB0 clock is selected via SFR CLKSEL (see SFR Definition 21.1).

Clock Recovery circuitry uses the incoming USB data stream to adjust the internal oscillator; this allows the internal oscillator to meet the requirements for USB clock tolerance. Clock Recovery should be used in the following configurations:

Communication Speed	USB Clock
Full Speed	Internal Oscillator
Low Speed	Internal Oscillator / 8

When operating USB0 as a Low Speed function with Clock Recovery, software must write 1 to the CRLOW bit to enable Low Speed Clock Recovery. Clock Recovery is typically not necessary in Low Speed mode.

Single Step Mode can be used to help the Clock Recovery circuitry to lock when high noise levels are present on the USB network. This mode is not required (or recommended) in typical USB environments.

USB Register Definition 23.5. CLKREC: Clock Recovery Control

Bit	7	6	5	4	3	2	1	0
Name	CRE	CRSSEN	CRLOW	Reserved	Reserved	Reserved	Reserved	Reserved
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	1	1	1	1

USB Register Address = 0x0F

Bit	Name	Function
7	CRE	Clock Recovery Enable Bit. This bit enables/disables the USB clock recovery feature. 0: Clock recovery disabled. 1: Clock recovery enabled.
6	CRSSEN	Clock Recovery Single Step. This bit forces the oscillator calibration into ‘single-step’ mode during clock recovery. 0: Normal calibration mode. 1: Single step mode.
5	CRLOW	Low Speed Clock Recovery Mode. This bit must be set to 1 if clock recovery is used when operating as a Low Speed USB device. 0: Full Speed Mode. 1: Low Speed Mode.
4:0	Reserved	Read = Variable. Must Write = 01111b.

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23.6. Function Addressing

The FADDR register holds the current USB0 function address. Software should write the host-assigned 7-bit function address to the FADDR register when received as part of a SET_ADDRESS command. A new address written to FADDR will not take effect (USB0 will not respond to the new address) until the end of the current transfer (typically following the status phase of the SET_ADDRESS command transfer). The UPDATE bit (FADDR.7) is set to 1 by hardware when software writes a new address to the FADDR register. Hardware clears the UPDATE bit when the new address takes effect as described above.

USB Register Definition 23.7. FADDR: USB0 Function Address

Bit	7	6	5	4	3	2	1	0
Name	UPDATE	FADDR[6:0]						
Type	R	R/W						
Reset	0	0	0	0	0	0	0	0

USB Register Address = 0x00

Bit	Name	Function
7	UPDATE	Function Address Update Bit. Set to 1 when software writes the FADDR register. USB0 clears this bit to 0 when the new address takes effect. 0: The last address written to FADDR is in effect. 1: The last address written to FADDR is not yet in effect.
6:0	FADDR[6:0]	Function Address Bits. Holds the 7-bit function address for USB0. This address should be written by software when the SET_ADDRESS standard device request is received on Endpoint0. The new address takes effect when the device request completes.

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USB Register Definition 23.16. CMIE: USB0 Common Interrupt Enable

Bit	7	6	5	4	3	2	1	0
Name					SOFE	RSTINTE	RSUINTE	SUSINTE
Type	R	R	R	R	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	1	1	0

USB Register Address = 0x0B

Bit	Name	Function
7:4	Unused	Read = 0000b. Write = don't care.
3	SOFE	Start of Frame Interrupt Enable. 0: SOF interrupt disabled. 1: SOF interrupt enabled.
2	RSTINTE	Reset Interrupt Enable. 0: Reset interrupt disabled. 1: Reset interrupt enabled.
1	RSUINTE	Resume Interrupt Enable. 0: Resume interrupt disabled. 1: Resume interrupt enabled.
0	SUSINTE	Suspend Interrupt Enable. 0: Suspend interrupt disabled. 1: Suspend interrupt enabled.

23.9. The Serial Interface Engine

The Serial Interface Engine (SIE) performs all low level USB protocol tasks, interrupting the processor when data has successfully been transmitted or received. When receiving data, the SIE will interrupt the processor when a complete data packet has been received; appropriate handshaking signals are automatically generated by the SIE. When transmitting data, the SIE will interrupt the processor when a complete data packet has been transmitted and the appropriate handshake signal has been received.

The SIE will not interrupt the processor when corrupted/erroneous packets are received.

23.10. Endpoint0

Endpoint0 is managed through the USB register E0CSR (USB Register Definition 23.18). The INDEX register must be loaded with 0x00 to access the E0CSR register.

An Endpoint0 interrupt is generated when:

1. A data packet (OUT or SETUP) has been received and loaded into the Endpoint0 FIFO. The OPRDY bit (E0CSR.0) is set to 1 by hardware.
2. An IN data packet has successfully been unloaded from the Endpoint0 FIFO and transmitted to the host; INPRDY is reset to 0 by hardware.
3. An IN transaction is completed (this interrupt generated during the status stage of the transaction).
4. Hardware sets the STSTL bit (E0CSR.2) after a control transaction ended due to a protocol violation.

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24.4.4. Data Register

The SMBus Data register SMB0DAT holds a byte of serial data to be transmitted or one that has just been received. Software may safely read or write to the data register when the SI flag is set. Software should not attempt to access the SMB0DAT register when the SMBus is enabled and the SI flag is cleared to logic 0, as the interface may be in the process of shifting a byte of data into or out of the register.

Data in SMB0DAT is always shifted out MSB first. After a byte has been received, the first bit of received data is located at the MSB of SMB0DAT. While data is being shifted out, data on the bus is simultaneously being shifted in. SMB0DAT always contains the last data byte present on the bus. In the event of lost arbitration, the transition from master transmitter to slave receiver is made with the correct data or address in SMB0DAT.

SFR Definition 24.5. SMB0DAT: SMBus Data

Bit	7	6	5	4	3	2	1	0
Name	SMB0DAT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xC2

Bit	Name	Function
7:0	SMB0DAT[7:0]	SMBus Data. The SMB0DAT register contains a byte of data to be transmitted on the SMBus serial interface or a byte that has just been received on the SMBus serial interface. The CPU can read from or write to this register whenever the SI serial interrupt flag (SMB0CN.0) is set to logic 1. The serial data in the register remains stable as long as the SI flag is set. When the SI flag is not set, the system may be in the process of shifting data in/out and the CPU should not attempt to access this register.

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24.5. SMBus Transfer Modes

The SMBus interface may be configured to operate as master and/or slave. At any particular time, it will be operating in one of the following four modes: Master Transmitter, Master Receiver, Slave Transmitter, or Slave Receiver. The SMBus interface enters Master Mode any time a START is generated, and remains in Master Mode until it loses an arbitration or generates a STOP. An SMBus interrupt is generated at the end of all SMBus byte frames. Note that the position of the ACK interrupt when operating as a receiver depends on whether hardware ACK generation is enabled. As a receiver, the interrupt for an ACK occurs **before** the ACK with hardware ACK generation disabled, and **after** the ACK when hardware ACK generation is enabled. As a transmitter, interrupts occur **after** the ACK, regardless of whether hardware ACK generation is enabled or not.

24.5.1. Write Sequence (Master)

During a write sequence, an SMBus master writes data to a slave device. The master in this transfer will be a transmitter during the address byte, and a transmitter during all data bytes. The SMBus interface generates the START condition and transmits the first byte containing the address of the target slave and the data direction bit. In this case the data direction bit (R/W) will be logic 0 (WRITE). The master then transmits one or more bytes of serial data. After each byte is transmitted, an acknowledge bit is generated by the slave. The transfer is ended when the STO bit is set and a STOP is generated. Note that the interface will switch to Master Receiver Mode if SMB0DAT is not written following a Master Transmitter interrupt. Figure 24.5 shows a typical master write sequence. Two transmit data bytes are shown, though any number of bytes may be transmitted. Notice that all of the “data byte transferred” interrupts occur **after** the ACK cycle in this mode, regardless of whether hardware ACK generation is enabled.

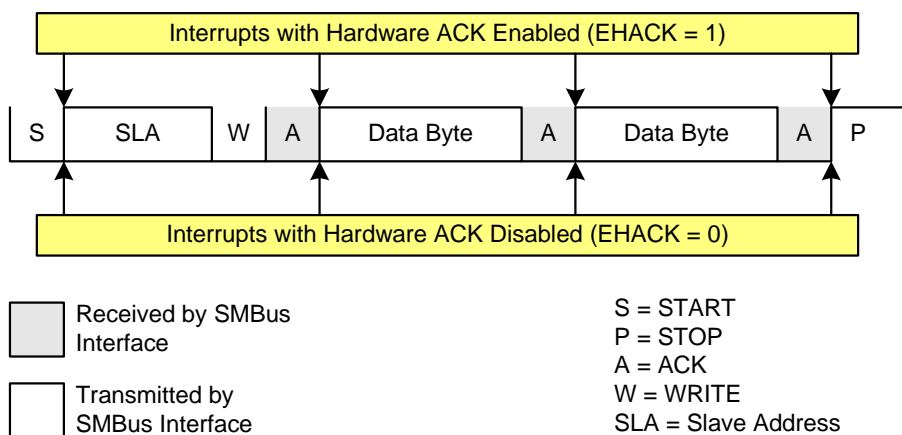


Figure 24.5. Typical Master Write Sequence

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SFR Definition 26.3. SBUF1: UART1 Data Buffer

Bit	7	6	5	4	3	2	1	0
Name	SBUF1[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xD3

Bit	Name	Description	Write	Read
7:0	SBUF1[7:0]]	Serial Data Buffer Bits. This SFR is used to both send data from the UART and to read received data from the UART1 receive FIFO.	Writing a byte to SBUF1 initiates the transmission. When data is written to SBUF1, it first goes to the Transmit Holding Register, where it is held for serial transmission. When the transmit shift register is available, data is transferred into the shift register, and SBUF1 may be written again.	Reading SBUF1 retrieves data from the receive FIFO. When read, the oldest byte in the receive FIFO is returned, and removed from the FIFO. Up to three bytes may be held in the FIFO. If there are additional bytes available in the FIFO, the RI1 bit will remain at logic 1, even after being cleared by software.

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SFR Definition 27.2. SPI0CN: SPI0 Control

Bit	7	6	5	4	3	2	1	0
Name	SPIF	WCOL	MODF	RXOVRN	NSSMD[1:0]		TXBMT	SPIEN
Type	R/W	R/W	R/W	R/W	R/W		R	R/W
Reset	0	0	0	0	0	1	1	0

SFR Address = 0xF8; Bit-Addressable

Bit	Name	Function
7	SPIF	SPI0 Interrupt Flag. This bit is set to logic 1 by hardware at the end of a data transfer. If SPI interrupts are enabled, an interrupt will be generated. This bit is not automatically cleared by hardware, and must be cleared by software.
6	WCOL	Write Collision Flag. This bit is set to logic 1 if a write to SPI0DAT is attempted when TXBMT is 0. When this occurs, the write to SPI0DAT will be ignored, and the transmit buffer will not be written. If SPI interrupts are enabled, an interrupt will be generated. This bit is not automatically cleared by hardware, and must be cleared by software.
5	MODF	Mode Fault Flag. This bit is set to logic 1 by hardware when a master mode collision is detected (NSS is low, MSTEN = 1, and NSSMD[1:0] = 01). If SPI interrupts are enabled, an interrupt will be generated. This bit is not automatically cleared by hardware, and must be cleared by software.
4	RXOVRN	Receive Overrun Flag (valid in slave mode only). This bit is set to logic 1 by hardware when the receive buffer still holds unread data from a previous transfer and the last bit of the current transfer is shifted into the SPI0 shift register. If SPI interrupts are enabled, an interrupt will be generated. This bit is not automatically cleared by hardware, and must be cleared by software.
3:2	NSSMD[1:0]	Slave Select Mode. Selects between the following NSS operation modes: (See Section 27.2 and Section 27.3). 00: 3-Wire Slave or 3-Wire Master Mode. NSS signal is not routed to a port pin. 01: 4-Wire Slave or Multi-Master Mode (Default). NSS is an input to the device. 1x: 4-Wire Single-Master Mode. NSS signal is mapped as an output from the device and will assume the value of NSSMD0.
1	TXBMT	Transmit Buffer Empty. This bit will be set to logic 0 when new data has been written to the transmit buffer. When data in the transmit buffer is transferred to the SPI shift register, this bit will be set to logic 1, indicating that it is safe to write a new byte to the transmit buffer.
0	SPIEN	SPI0 Enable. 0: SPI disabled. 1: SPI enabled.

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SFR Definition 28.3. TMOD: Timer Mode

Bit	7	6	5	4	3	2	1	0
Name	GATE1	C/T1	T1M[1:0]		GATE0	C/T0	T0M[1:0]	
Type	R/W	R/W	R/W		R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x89

Bit	Name	Function
7	GATE1	Timer 1 Gate Control. 0: Timer 1 enabled when TR1 = 1 irrespective of $\overline{\text{INT1}}$ logic level. 1: Timer 1 enabled only when TR1 = 1 AND $\overline{\text{INT1}}$ is active as defined by bit IN1PL in register IT01CF (see SFR Definition 17.7).
6	C/T1	Counter/Timer 1 Select. 0: Timer: Timer 1 incremented by clock defined by T1M bit in register CKCON. 1: Counter: Timer 1 incremented by high-to-low transitions on external pin (T1).
5:4	T1M[1:0]	Timer 1 Mode Select. These bits select the Timer 1 operation mode. 00: Mode 0, 13-bit Counter/Timer 01: Mode 1, 16-bit Counter/Timer 10: Mode 2, 8-bit Counter/Timer with Auto-Reload 11: Mode 3, Timer 1 Inactive
3	GATE0	Timer 0 Gate Control. 0: Timer 0 enabled when TR0 = 1 irrespective of $\overline{\text{INT0}}$ logic level. 1: Timer 0 enabled only when TR0 = 1 AND $\overline{\text{INT0}}$ is active as defined by bit IN0PL in register IT01CF (see SFR Definition 17.7).
2	C/T0	Counter/Timer 0 Select. 0: Timer: Timer 0 incremented by clock defined by T0M bit in register CKCON. 1: Counter: Timer 0 incremented by high-to-low transitions on external pin (T0).
1:0	T0M[1:0]	Timer 0 Mode Select. These bits select the Timer 0 operation mode. 00: Mode 0, 13-bit Counter/Timer 01: Mode 1, 16-bit Counter/Timer 10: Mode 2, 8-bit Counter/Timer with Auto-Reload 11: Mode 3, Two 8-bit Counter/Timers

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SFR Definition 29.4. PCA0CPMn: PCA Capture/Compare Mode

Bit	7	6	5	4	3	2	1	0
Name	PWM16n	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Addresses: 0xDA (n = 0), 0xDB (n = 1), 0xDC (n = 2), 0xDD (n = 3), 0xDE (n = 4)

Bit	Name	Function
7	PWM16n	16-bit Pulse Width Modulation Enable. This bit enables 16-bit mode when Pulse Width Modulation mode is enabled. 0: 8 to 11-bit PWM selected. 1: 16-bit PWM selected.
6	ECOMn	Comparator Function Enable. This bit enables the comparator function for PCA module n when set to 1.
5	CAPPn	Capture Positive Function Enable. This bit enables the positive edge capture for PCA module n when set to 1.
4	CAPNn	Capture Negative Function Enable. This bit enables the negative edge capture for PCA module n when set to 1.
3	MATn	Match Function Enable. This bit enables the match function for PCA module n when set to 1. When enabled, matches of the PCA counter with a module's capture/compare register cause the CCFn bit in PCA0MD register to be set to logic 1.
2	TOGn	Toggle Function Enable. This bit enables the toggle function for PCA module n when set to 1. When enabled, matches of the PCA counter with a module's capture/compare register cause the logic level on the CEXn pin to toggle. If the PWMn bit is also set to logic 1, the module operates in Frequency Output Mode.
1	PWMn	Pulse Width Modulation Mode Enable. This bit enables the PWM function for PCA module n when set to 1. When enabled, a pulse width modulated signal is output on the CEXn pin. 8 to 11-bit PWM is used if PWM16n is cleared; 16-bit mode is used if PWM16n is set to logic 1. If the TOGn bit is also set, the module operates in Frequency Output Mode.
0	ECCFn	Capture/Compare Flag Interrupt Enable. This bit sets the masking of the Capture/Compare Flag (CCFn) interrupt. 0: Disable CCFn interrupts. 1: Enable a Capture/Compare Flag interrupt request when CCFn is set.
Note: When the WDTE bit is set to 1, the PCA0CPM4 register cannot be modified, and module 4 acts as the watchdog timer. To change the contents of the PCA0CPM4 register or the function of module 4, the Watchdog Timer must be disabled.		